M50744-XXXSP/FP
M50746-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50744-XXXSP and the M50746-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. Both are housed in a 64-pin shrink plastic molded DIP (flat package type also available). These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50744-XXXSP and the M50746-XXXSP are noted below. The following explanations apply to the M50744-XXXSP. Specification variations for other chips are noted accordingly.

Type name	ROM size
M50744-XXXSP	4096bytes
M50746-XXXSP	6144bytes

The differences between the M50744-XXXSP and the M50744-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

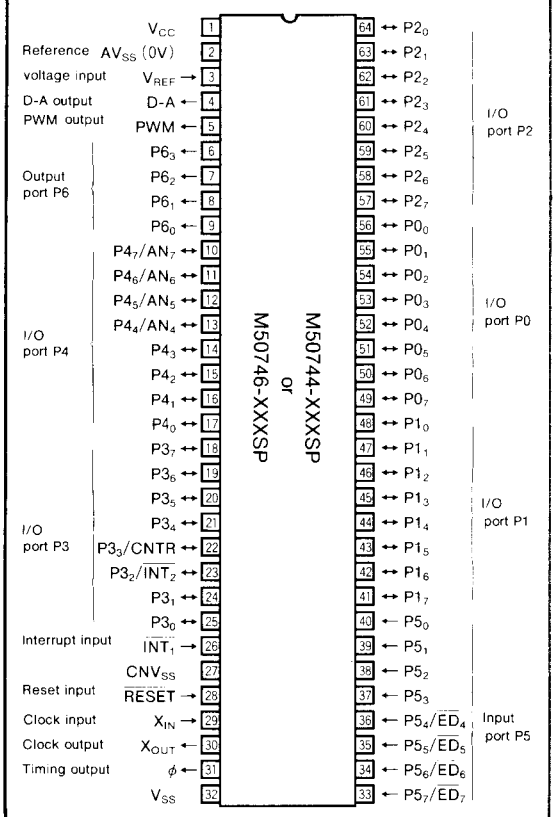
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 4096 bytes (M50744-XXXSP)
  6144 bytes (M50746-XXXSP)
  RAM 144bytes
- Instruction execution time
  ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply f(X_{IN})=4MHz ..... 5V±10%
- Power dissipation
  normal operation mode (at 4MHz frequency) 15mW
- Subroutine nesting ..... 72 levels (Max.)
- Interrupt ..... 6 types, 5 vecters
- 8-bit timer 3
- Programmable I/O (Ports P0, P1, P2, P3, P4) 40
- Input ports (Port P5) 8
- Output ports (Port P6) 4
- A-D converter ..... 8-bit successive approximation
- D-A converter
- 8-bit PWM function
- Watchdog timer

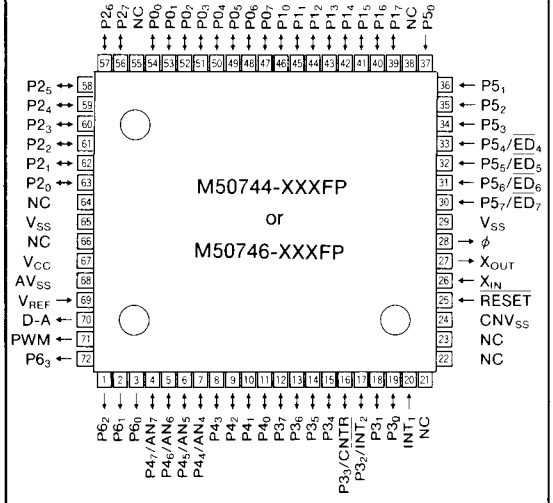
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B



Outline 72P6

NC : No connection

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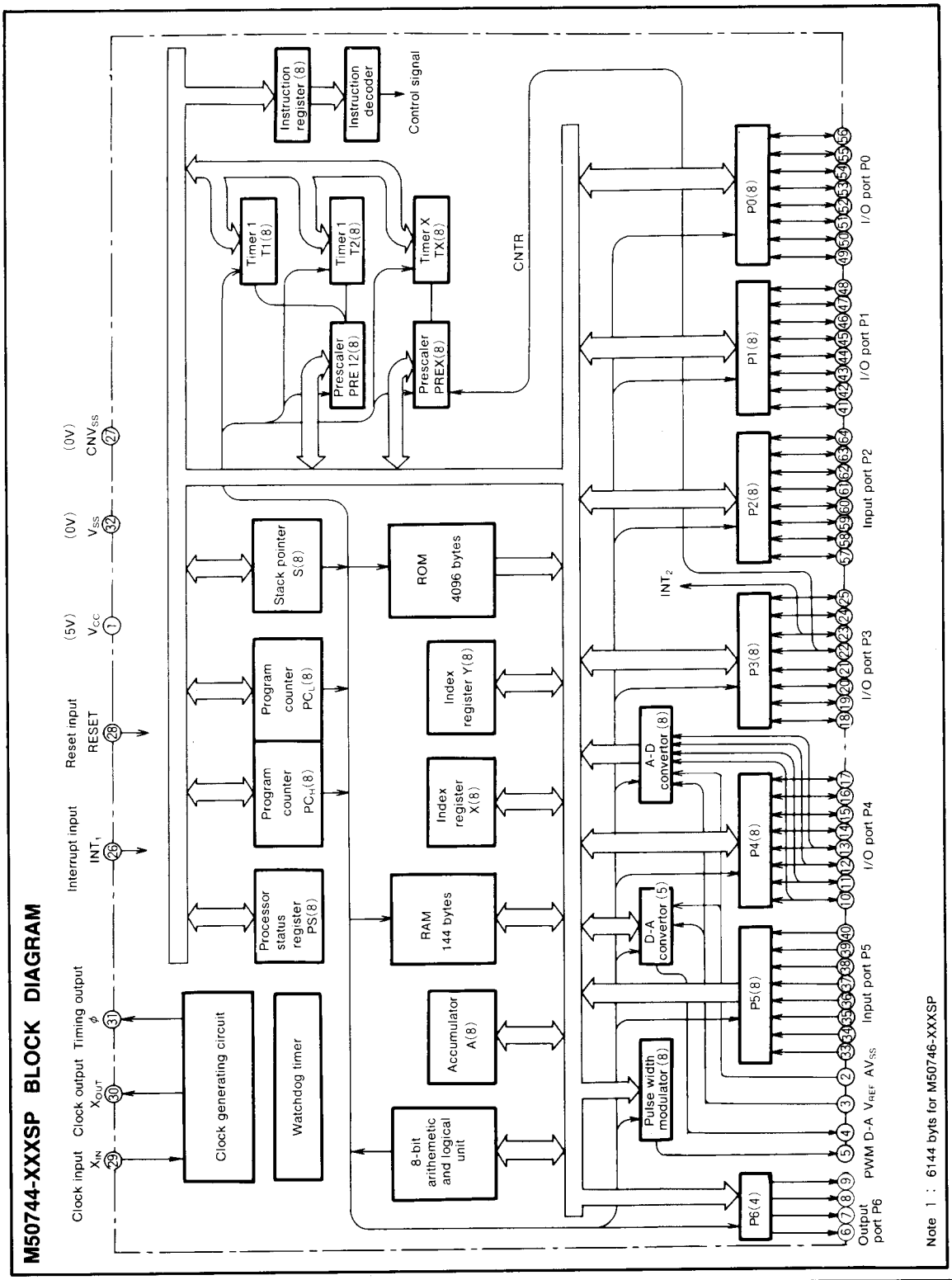
M50744-XXXSP BLOCK DIAGRAM



FUNCTIONS OF M50744-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction excution time			2μs (minimum instructions at 4MHz frequency)
Memory size	ROM		4096bytes (6144bytes for M50746-XXXSP)
	RAM		144bytes
I/O ports	$\overline{INT_1}$	Input	1-bit×1
	P0, P1, P2, P3, P4	I/O	8-bit×5 (Part of P3 used with timer I/O and interrupt input)
	P5	Input	8-bit×1
	P6	Output	4-bit×1
Timers			8-bit prescaler×2+8-bit timer×3
A-D converter			8-bit× 1 (4 channels)
D-A converter			5-bit×1
Pulse width modulator			8-bit×1
Watchdog timer			15-bit×1
Subroutine nesting			72 levels (max.)
Interrupt			2 external interrupts, 3 internal timer interrupts
Clock generating circuit			Built-in (externally connected ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	High-speed operation		15mW (at 4MHz frequency)
I/O characteristics	I/O voltage		12V (Ports P0, P1, P3, P4, P5, P6, $\overline{INT_1}$)
	Output current		5mA (Ports P0, P1, P2, P3, P4)
Memory expansion			Possibe
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package	M50744-XXXSP, M50746-XXXSP		64-pin shrink plastic molded DIP
	M50744-XXXFP, M50746-XXXFP		72-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
AV_{SS}	Voltage input for A-D and D-A		This is GND input pin for the A-D and D-A converters.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D and D-A converters.
D-A	D-A output	Output	This is output pin from the D-A converter.
PWM	PWM output	Output	This is output pin from the pulse width modulator. The output structure is N-channel open drain.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is CMOS output.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. $P3_3$ and $P3_2$ work as CNTR pin and the lowest interrupt input pin ($\overline{INT_2}$), respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0. $P4_4$~$P4_7$ work as analog input port AN_4~AN_7.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port. $P5_4$~$P5_7$ can be used as the edge sense inputs.
$P6_0$~$P6_3$	Output port P6	Output	Port P6 is a 4-bit output port. The output structure is N-channel open drain.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50744-XXXSP is shown in Figure 1. Addresses $F000_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 4096 bytes.

Addresses $E800_{16}$ to $FFFF_{16}$ are the ROM address area assigned to the M50746-XXXSP.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $008F_{16}$ are assigned to the built-in RAM and consist of 144 bytes of static RAM. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

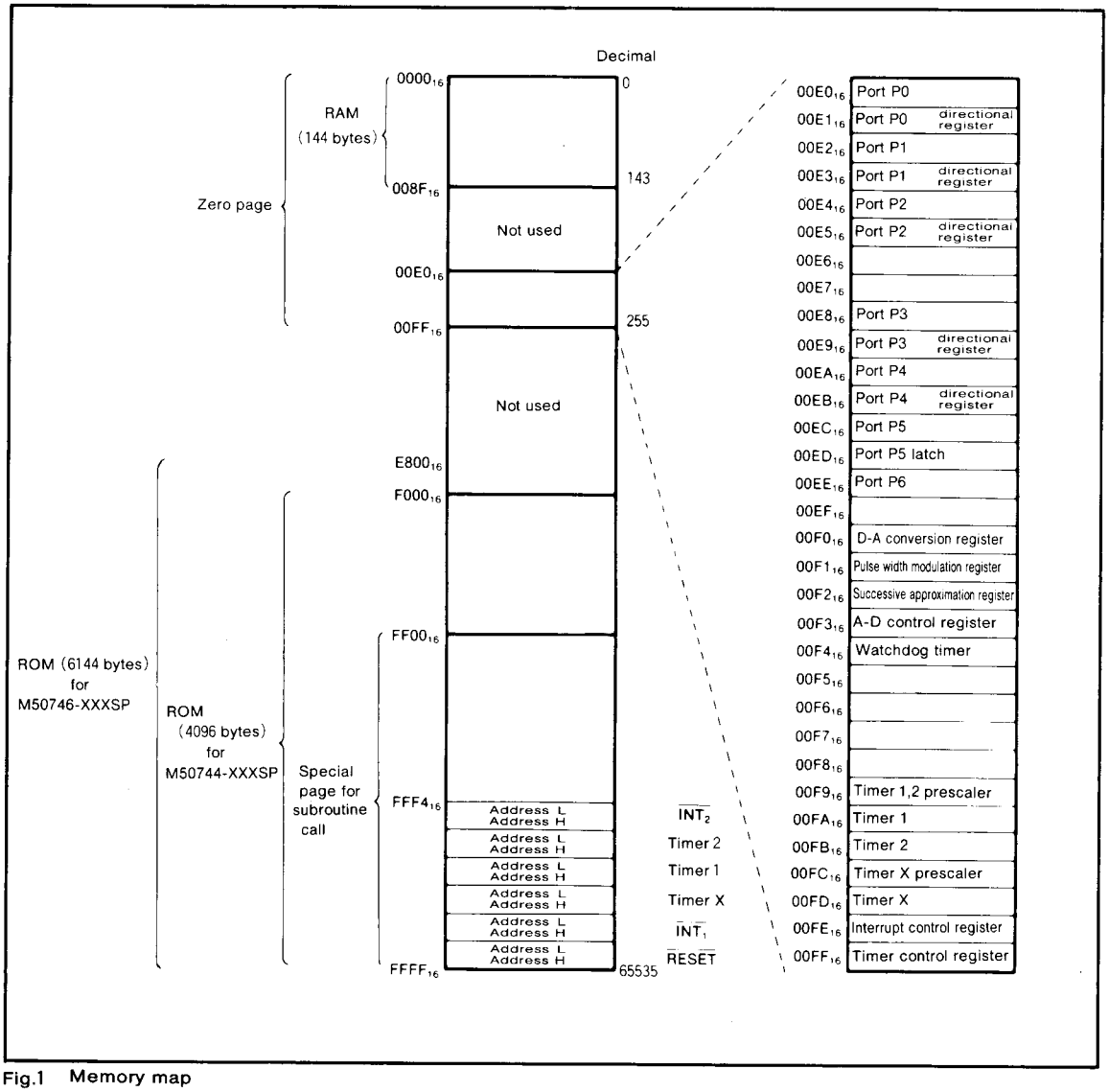


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

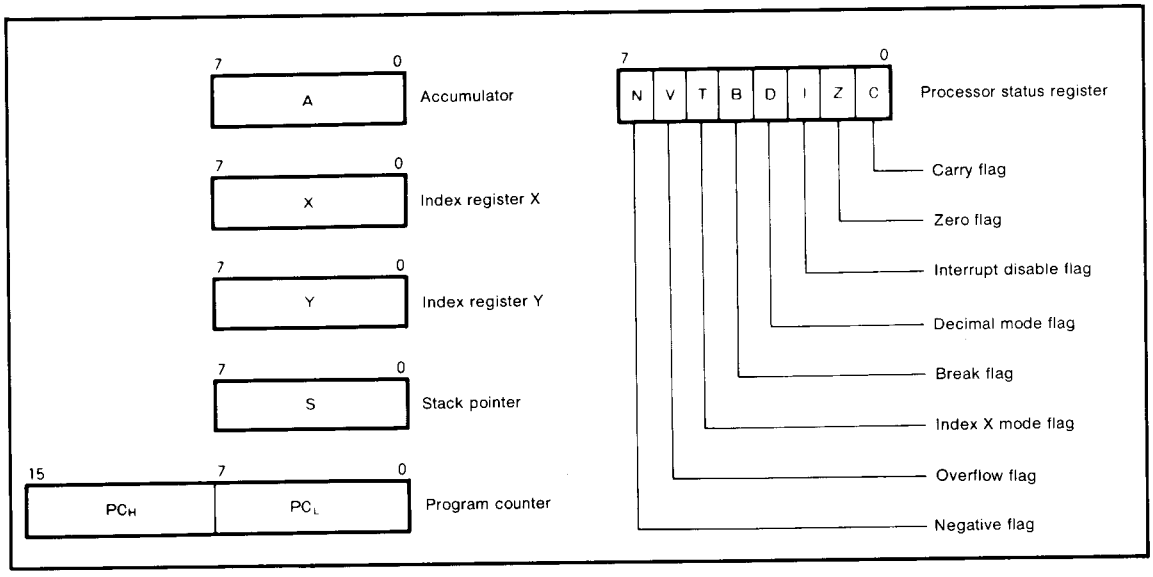


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The location of the stack can be determined by the stack page bit (bit 4 at address $00FF_{16}$). When bit 4 is "0" and the contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When bit 4 is "1", the stack address is set to $01XX_{16}$. When using this microcomputer in the single-chip mode, the stack page bit must be "0" and the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
RESET	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{INT_1}$	2	$FFFD_{16}$, $FFFC_{16}$
Timer X	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1	4	$FFF9_{16}$, $FFF8_{16}$
Timer 2	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{INT_2}$(BRK)	6	$FFF5_{16}$, $FFF4_{16}$

INTERRUPT

The M50744-XXXSP can be interrupted from seven souces; $\overline{INT_1}$, timer X, timer 1, timer 2, or $\overline{INT_2}$/BRK instruction.

However, the $\overline{INT_2}$ pin is used with port $P3_2$ and the corresponding directional register bit should be set to "0" when $P3_2$ is used as an interrupt input pin.

These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins go from "H" to "L"

(2) When the contents of timer X, timer 1, timer 2 go to "0"

These request bits can be reset by the program but can not

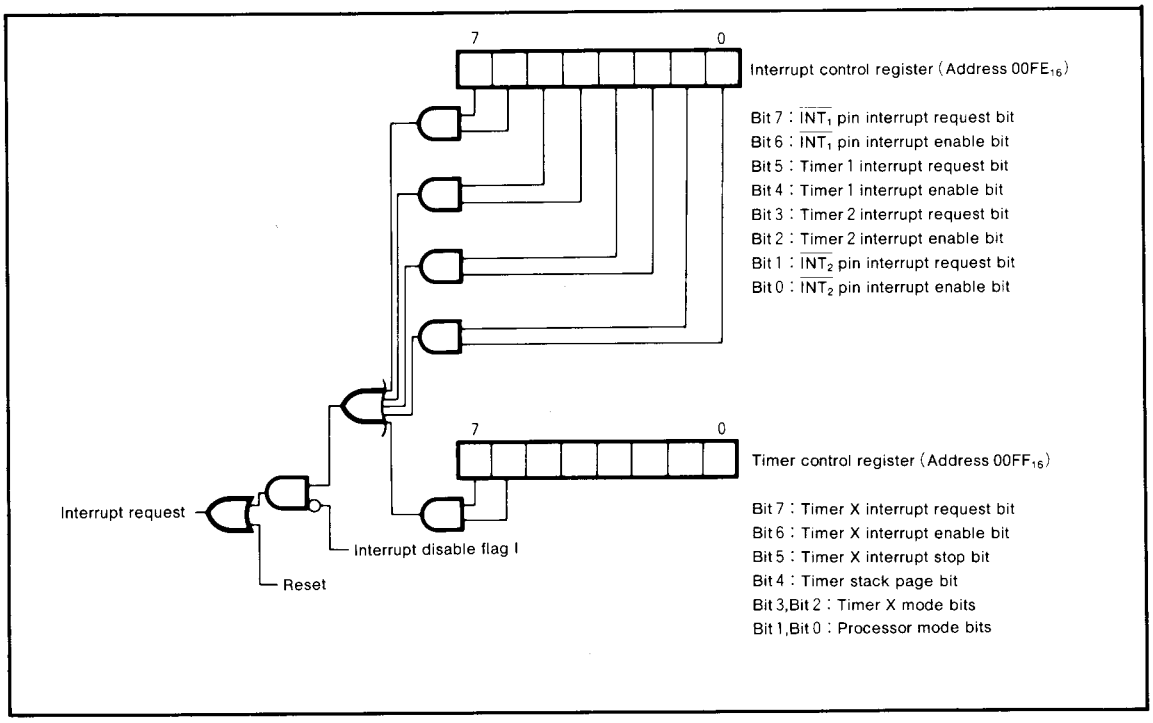


Fig. 3 Interrupt control

be set by the program. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT_2}$ generated the interrupt.

TIMER

The M50744-XXXSP has three timers; timer X, timer 1, and timer 2. Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1 and timer 2 is shown in Figure 4.

The $P3_3$/CNTR pin cannot be used as CNTR when $P3_3$ is being used in the normal I/O mode.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+1)$, where n is the decimal contents of the prescaler latch. All three timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see interrupt section).

The four modes of timer X as follows:

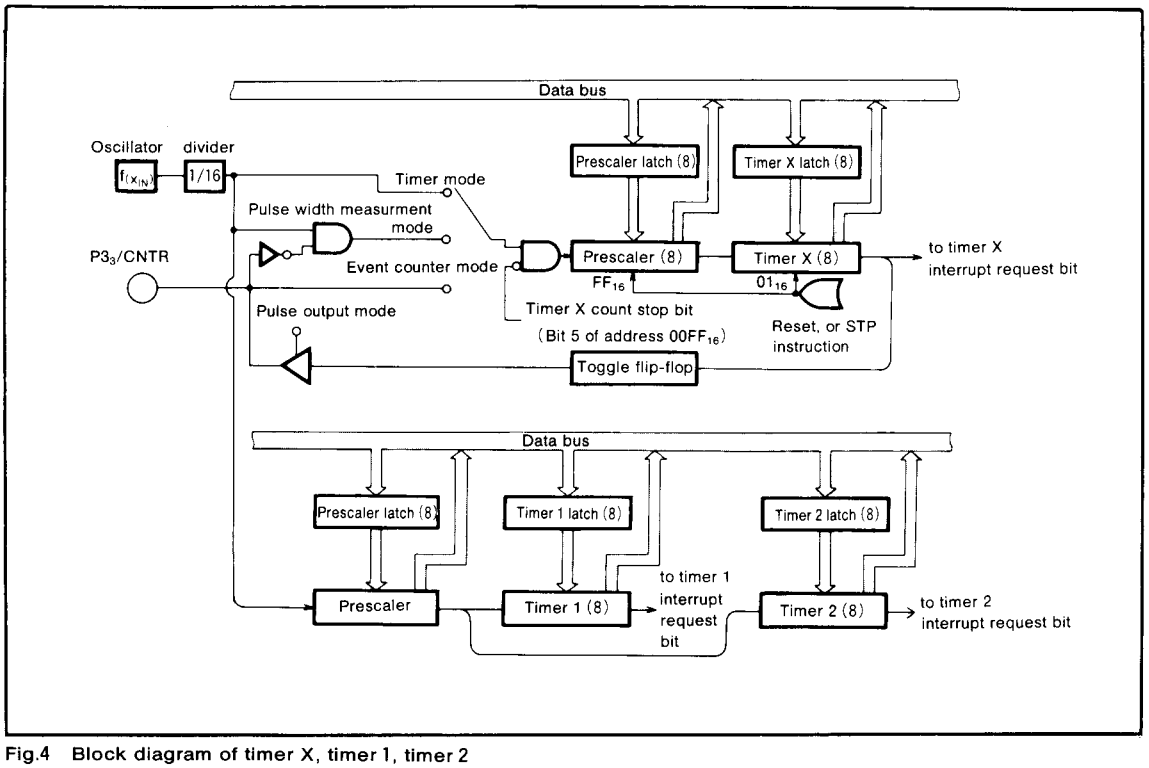


Fig.4 Block diagram of timer X, timer 1, timer 2

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]
This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock sourse.

(4) Pulse width measurement mode [11]
This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 5.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

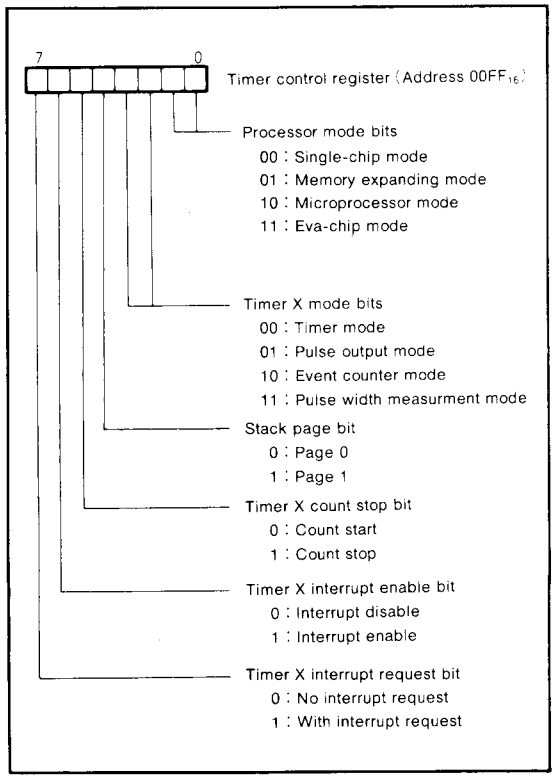


Fig.5 Structure of timer control registe

A-D CONVERTER

An 8-bit successive approximation method of A-D conversion is employed providing a precision of ±3LSB. A block diagram of the A-D convertor is shown in Figure 6. Conversion is automatic once it is started with the program.

The four analog inputs are used in common with pins $P4_7$, $P4_6$, $P4_5$, and $P4_4$ of port 4. Bits 1 and 0 of the A-D control regsiter (address $00F3_{16}$) are used to select which pins are used for A-D conversion. The input condition is accomplished by setting to "0" the bit in the directional register that corresponds to the pin where A-D conversion is to take place. Bit 4 of the A-D control regsiter is the A-D conversion end bit. During A-D conversion, this bit is "0", and upon completion becomes "1". Thus, it can be ascertained whether or not A-D conversion has been completed or not by inspecting this bit. The relation between the contents of the A-D control register and the selection of input pins are shown in Figure 7.

The results of the conversion can be found be reading the contents of the successive approximation register (address $00F2_{16}$) which stores the results of the conversion. The procedure for executing A-D conversion is next explained. Firstly, the pin that is to be used for the A-D conversion is selected by setting bit 1 and bit 0 of the A-D control register. Next, the successive approximation is written to upon which the A-D conversion starts. Since actual data is not written to the successive approximation, any type of may be written. Simultaneous with its being written, the A-D conversion end bit (bit 4 of address $00F3_{16}$) is cleared to "0" signifying that A-D conversion operations are being conducted. A-D conversion completes after 198 clock cycles upon which the A-D conversion end bit is set to "1" and the results of the conversion can be found in the successive approximation. Since the comparator consists of the capacitive coupled configuration, f (X_{IN}) is needed larger than 1MHz during A-D conversion.

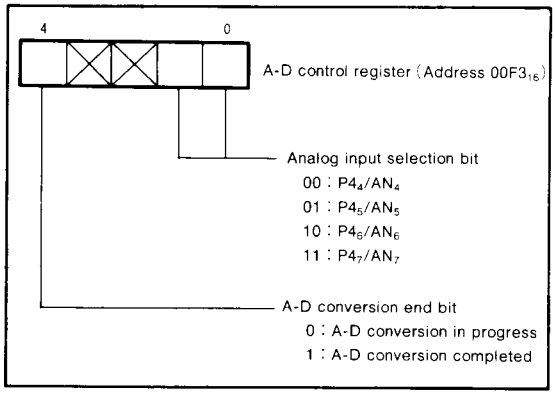


Fig.7 Structure of A-D control register

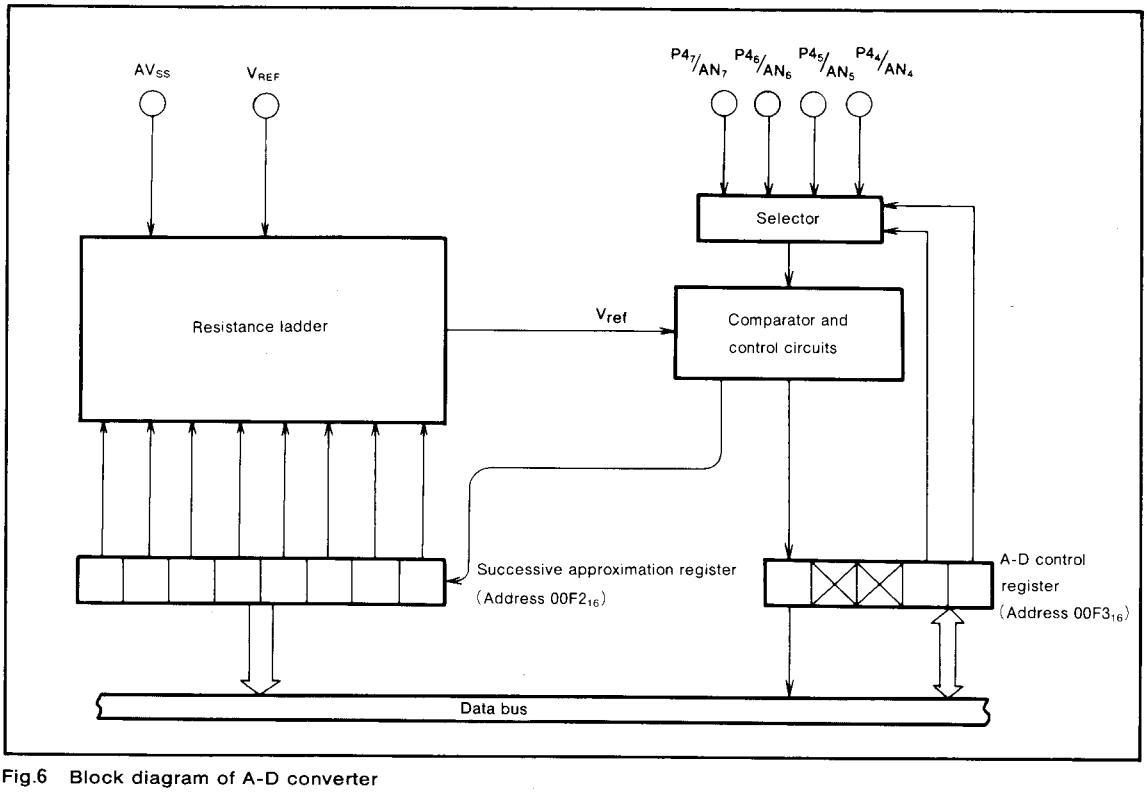


Fig.6 Block diagram of A-D converter

D-A CONVERTER

The R-2R method is used for D-A conversion. The block diagram is shown in Figure 8. An analog voltage is output that corresponds to the contents of the D-A conversion register (address $00F0_{16}$). Ideally, the relation of the analog output voltage V and the content n of the D-A conversion register is $V=V_{REF} \times n/32 (n=0 \sim 31)$.

Reset operation clears the contents (n) of the D-A conversion register to 0_{16}.

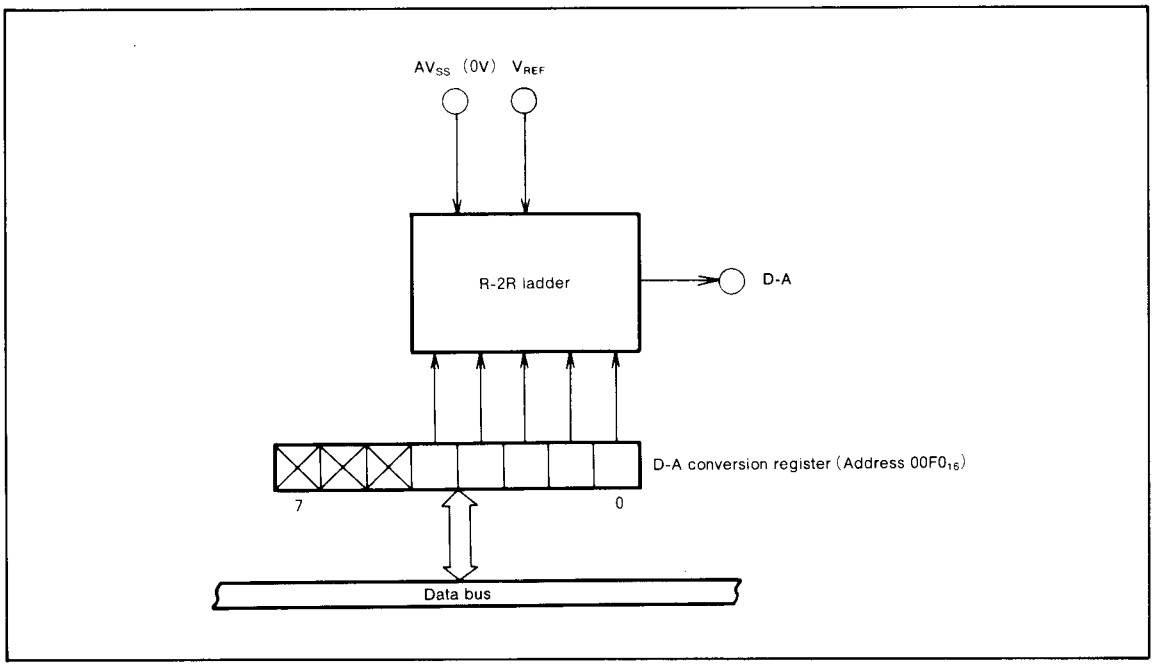


Fig.8 Block diagram of the D-A converter

PULSE WIDTH MODULATOR

The pulse width modulation register (address $00F1_{16}$) is configured of an 8-bit counter. The period of repetition is 4080 clock cycles. With the content of the pulse width modulation register m, the PWM pin becomes high-level for the period of 4080 × m/255 (m=0~255). Figure 9 shows that relationship. An N-channel open drain output is used for the PWM pin.

Reset sets the content m of the pulse width modulation register to 00_{16}.

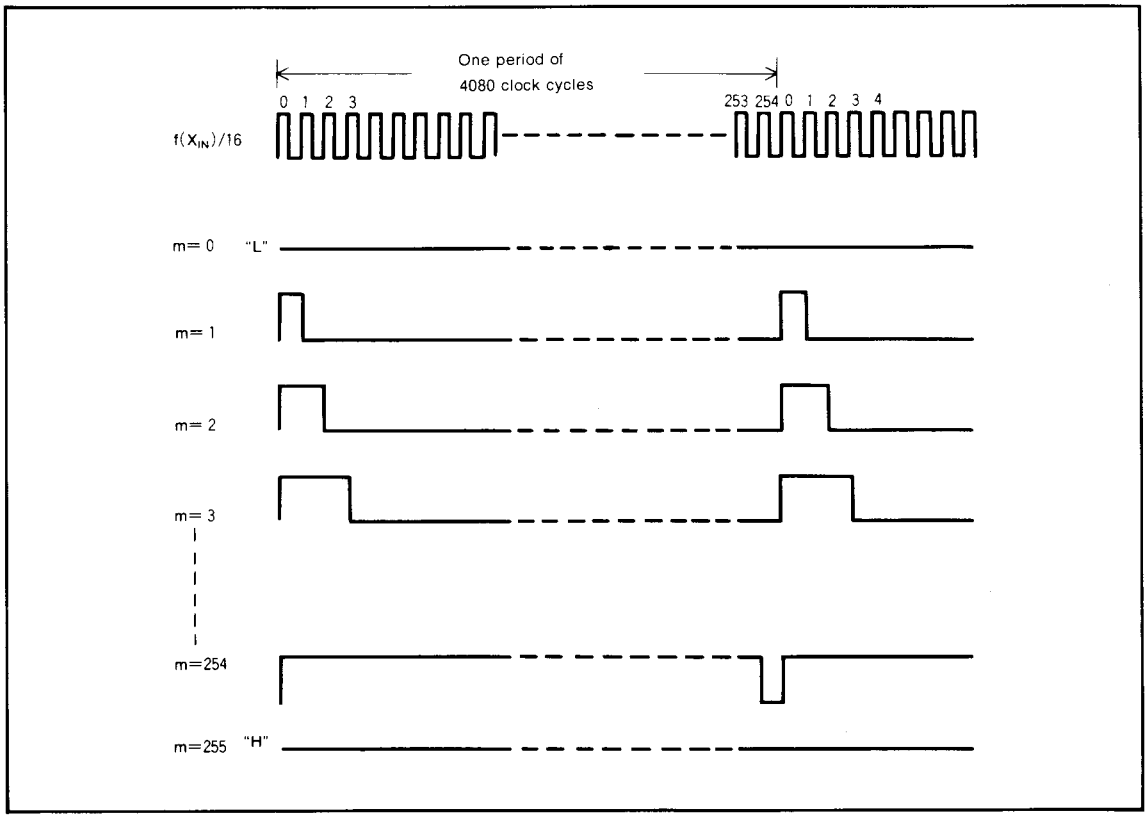


Fig.9 Relation between m and PWM output

WATCHDOG TIMER

The watchdog timer provides the means to return to a reset condition when a program runs wild and the program will not run the normal loops.

The watchdog timer (address $00F4_{16}$) is a 15-bit counter. The watchdog timer counts 1/16th the output frequency of the oscillator. The watchdog timer is set to $7FFF_{16}$ when a reset is accomplished or a write operation has been made to it. As well as any of the instructions that generate a write signal, such as STA, LDM, and CLB, can be used to write data to the watchdog timer. An output of the most significant bits of the watchdog timer is input to the reset circuit. When 262144 clock cycles have been counted, the most significant bit becomes "0" and reset is carried out. When reset is carried out, the watchdog timer is set to $7FFF_{16}$ and reset is released. The program then begins again from reset vector address. Normally, the program is written so that a writing operation is made to the watchdog timer prior to the most significant bit's becoming "0". Application of a + 10V to the $\overline{\text{RESET}}$ pin will disable the watchdog timer function.

Since execution of the STP instruction causes both the clock and the watchdog timer to stop, an option is offered where the STP instruciotn can be disabled.

RESET CIRCUIT

The M50744-XXXSP is reset according to the sequence shown in Figure 10. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 11.

An example of the reset circuit is shown in Figure 12.

When the power on reset is used, the $\overline{\text{RESET}}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

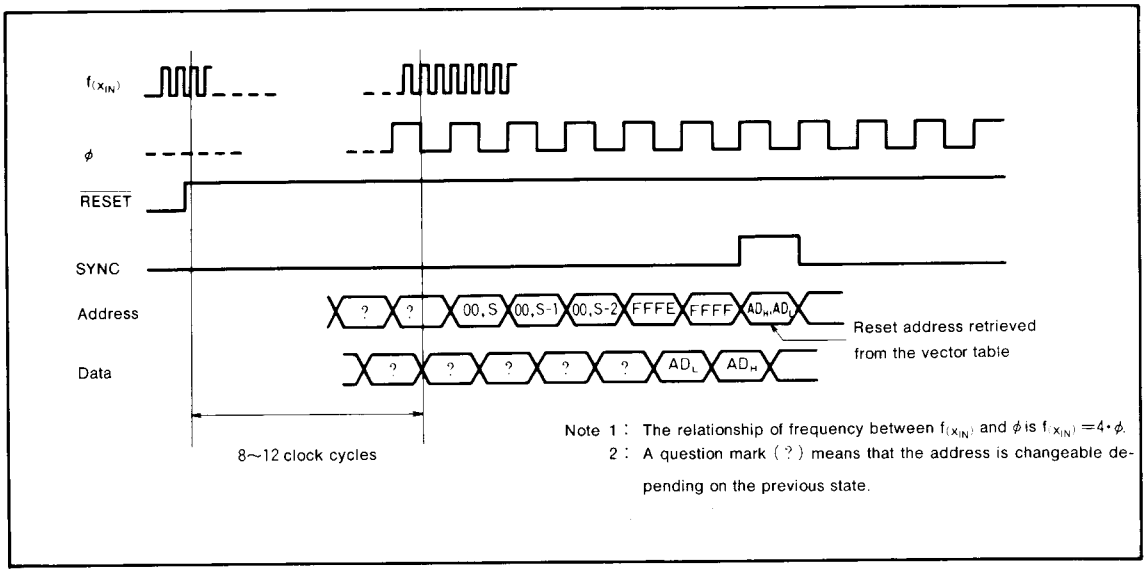


Fig.10 Timing diagram at reset

	Address	
(1) Port P0 directional register	($E1_{16}$) ···	00_{16}
(2) Port P1 directional register	($E3_{16}$) ···	00_{16}
(3) Port P2 directional register	($E5_{16}$) ···	00_{16}
(4) Port P3 directional register	($E9_{16}$) ···	00_{16}
(5) Port P4 directional register	(EB_{16}) ···	00_{16}
(6) Port 6 (Note 1)	(EE_{16}) ···	FF_{16}
(7) D-A conversion register	($F0_{16}$) ···	0 0 0 0 0
(8) Pulse width modulation register	($F1_{16}$) ···	00_{16}
(9) Watchdog timer	($F4_{16}$) ···	$7FFF_{16}$
(10) Prescaler	(FC_{16}) ···	FF_{16}
(11) Timer X	(FD_{16}) ···	01_{16}
(12) Interrupt control register	(FE_{16}) ···	00_{16}
(13) Timer control register	(FF_{16}) ···	00_{16}
(14) Processor status register (only the interrupt disable flag is set.)	(PS) ···	1
(15) Program counter	(PC_H) ···	Contents of address $FFFF_{16}$
	(PC_L) ···	Contents of address $FFFF_{16}$

Note 1 : Port P6 is the high-impedance state during reset.
After return from reset, it is "FF_{16}".

Fig.11 Internal state of microcomputer at reset

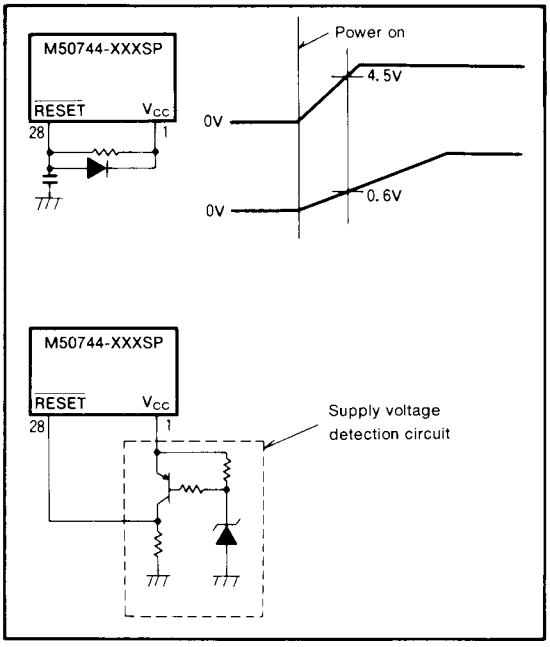


Fig.12 Example of reset circuit

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain output.

As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. In the other modes, P1's functions are slighlty different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0, but it has CMOS output. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

In the single-chip mode, port P3 has the same function as P0. In the other modes, P3's functions are slightly different from P0's. Port P3 can also be used as $\overline{INT_2}$ and I/O pins for timer X. For more details, see the processor mode information.

(5) Port P4

Port P4 has the same function as port P0 in the single-chip mode. But $P4_7$ through $P4_4$ can also be used as analog input pins AN_7 through AN_4.

(6) Port P5

Port P5 is an input port. $P5_4$ through $P5_7$ can also be used as edge sence inputs. In such a case, reading is begun from $00ED_{16}$. $00ED_{16}$ is provided with a latch which is set to "1" when the input changes from high-level to low-level. The input pulse width must be at least 7 clock cycle wide. The latch is reset by using such instructions as LDM and CLB to write a "0" to the latch. When $00ED_{16}$ is read, the lower order 4 bits are always zero.

When port P5 is used as level sence input, read the contents of the address $00EC_{16}$.

(7) Port P6

Port P6 is a 4-bit output port. It has N-channel open drain output. See Figure 13 for more details.

(8) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ.

(9) $\overline{INT_1}$ pin

The $\overline{INT_1}$ pin is an interrupt input pin. The $\overline{INT_1}$ interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

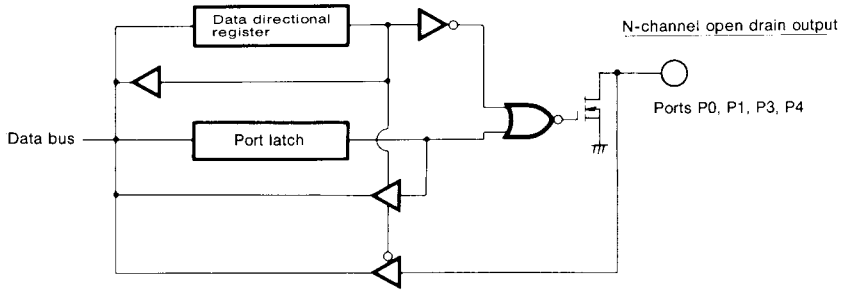
(10) $\overline{INT_2}$ pin ($P3_2/\overline{INT_2}$ pin)

The $\overline{INT_2}$ pin is an interrupt input pin used with $P3_2$. To use this pin as an interrupt pin, set the corresponding bit in the directional register to input ("0"). When this signal level changes from "H" to "L", the interrupt request bit (bit 1 at address $00FE_{16}$) is set to "1".

(11) CNTR pin ($P3_3$/CNTR pin)

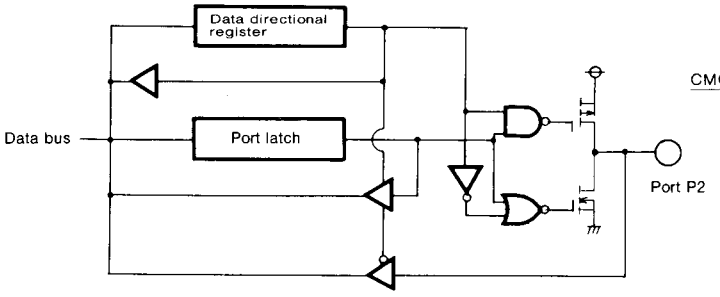
The $P3_3$/CNTR pin is an I/O pin of timer X. To use this pin as the timer X input pin, set the corresponding directional register bit to input ("0"). In the event counter mode, CNTR becomes the input pin of the external pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

Ports P0, P1, P3, P4

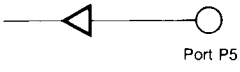


Note : P3 is used both as a timer input/output pin and an interrupt input pin.
P4 is used as an analog input pin.

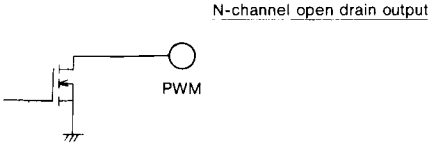
Port P2



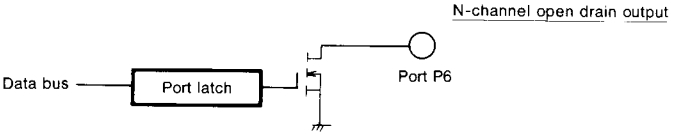
Port P5



PWM



Port P6



ϕ

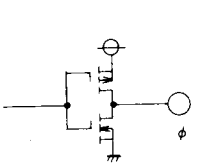


Fig.13 Block diagram of port P0~P6 (single-chip mode) and ϕ output format

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0 ~ P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 15 shows the functions of ports P0~P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 14.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

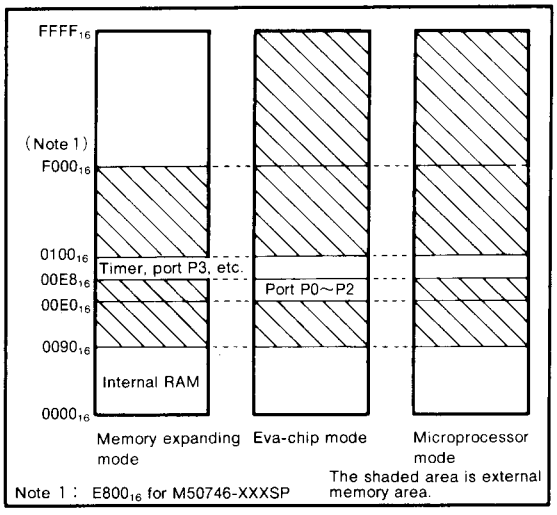


Fig.14 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0 ~ P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost. Port P2 becomes the data bus of $D_7 \sim D_0$ (including instruction code) and loses its normal I/O functions. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively when ϕ enters into the "H" state. Port $P3_2$ functions as an input port during this same transition.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode.

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the databus ($D_7 \sim D_0$) and loses its normal I/O functions. Port $P3_1$ and $P3_0$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

In this mode, the internal ROM is inhibited so the external memory is requierd.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original I/O functions while ϕ is at the "H" state, and works as a data bus of $D_7 \sim D_0$ (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P3_1$ and $P3_0$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

Port \ Mode	Single-chip mode (CM_1=0, CM_0=0)	Eva-chip mode (CM_1=1, CM_0=1)	Memory expanding mode (CM_1=0, CM_0=1)	Microprocessing mode (CM_1=1, CM_0=0)
Port P0	Ports $P0_7$~$P0_0$: I/O port	Ports $P0_7$~$P0_0$: Address A_7~A_0 / I/O port	Ports $P0_7$~$P0_0$: Address A_7~A_0	Same as left
Port P1	Ports $P1_7$~$P1_0$: I/O port	Ports $P1_7$~$P1_0$: Address A_{15}~A_8 / I/O port	Ports $P1_7$~$P1_0$: Address A_{15}~A_8	Same as left
Port P2	Ports $P2_7$~$P2_0$: I/O port	Ports $P2_7$~$P2_0$: Output port / Data D_7~D_0	Ports $P2_7$~$P2_0$: Data D_7~D_0	Same as left
Port P3	Ports $P3_7$~$P3_0$: I/O port	Ports $P3_7$~$P3_2$: I/O port; Port $P3_1$: SYNC / I/O port; Port $P3_0$: R/W / I/O port	Ports $P3_7$~$P3_2$: I/O port; Port $P3_1$: SYNC; Port $P3_0$: R/W	Same as left

Fig.15 Processor mode and functions of Ports P0~P3

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 18.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleard when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 16.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock uasge is shown in Figure 17. X_{IN} is the input, and X_{OUT} is open.

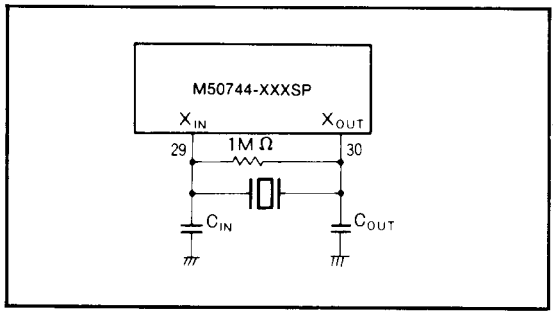


Fig.16 External ceramic resonator circuit

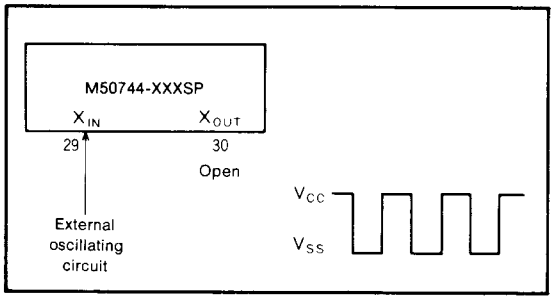


Fig.17 External clock input circuit

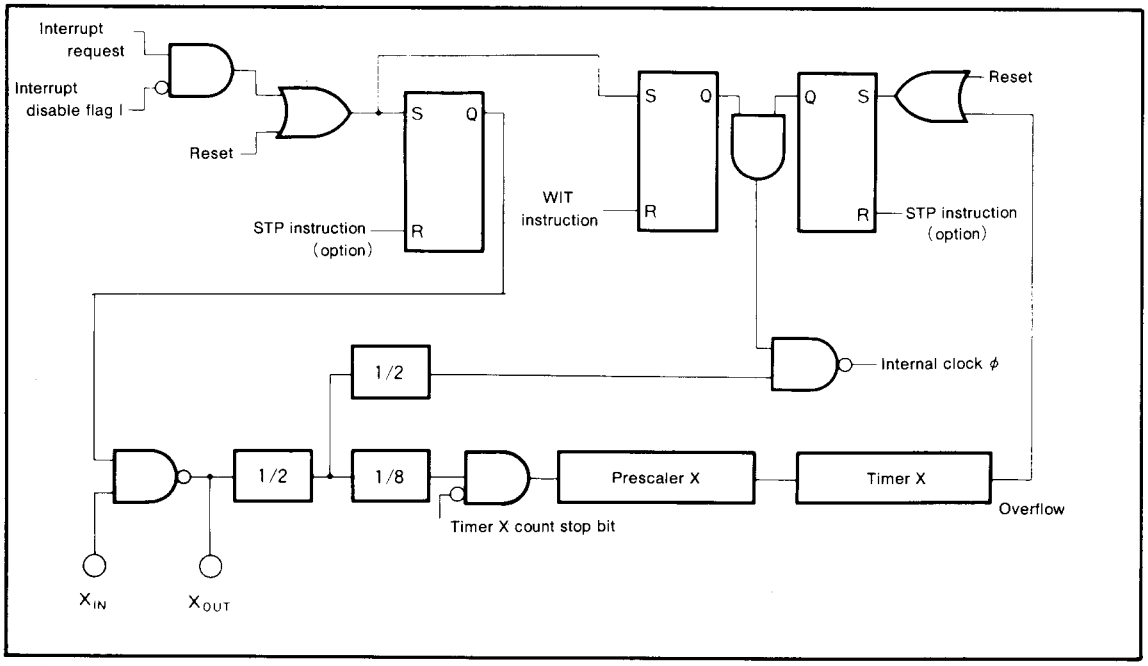


Fig.18 Block diagram of the clock generating circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

(6) Since the comparator consists of the capacitive coupled configuration, f(X_{IN}) is needed lager than 1MHz during A-D conversion. And during A-D conversion, don't use STP or WIT instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mark specification form

(3) ROM data ..... EPROM 3sets

Write the following option on the mask ROM confirmation form

• STP instruction option

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3～7	V
V_I	Input voltage X_{IN}		−0.3～7	V
V_I	Input voltage $P2_0$～$P2_7$, $P4_4$～$P4_7$		−0.3～V_{CC}+0.3	V
V_I	Input voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P3_0$～$P3_7$, $P4_0$～$P4_3$, $P5_0$～$P5_7$, $\overline{INT_1}$	With respect to V_{SS} With the output transistor cut-off	−0.3～13	V
V_I	Input voltage CNV_{SS}, $\overline{RESET}$		−0.3～13	V
V_O	Output voltage $P2_0$～$P2_7$, $P4_4$～$P4_7$, X_{OUT}, ϕ, D-A		−0.3～V_{CC}+0.3	V
V_O	Output voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P3_0$～$P3_7$, $P4_0$～$P4_3$, $P6_0$～$P6_3$, PWM		−0.3～13	V
P_d	Power dissipation	T_a=25℃	1000(Note 1)	mW
T_{opr}	Operating temperature		−10～70	℃
T_{stg}	Storage temperature		−40～125	℃

Note 1 : 300mW for QFP types

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10～70℃, unless otherwise noted)

Symbol	Parameter	Limits Min.	Limits Nom.	Limits Max.	Unit
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, $P5_0$～$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, $P5_0$～$P5_7$, $\overline{INT_1}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, PWM (Note 3)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$～$P6_3$ (Note 3)			15	mA
$I_{OL(avg)}$	"L" average output current $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, PWM (Note 2)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0$～$P6_3$ (Note 2)			7	mA
$I_{OH(peak)}$	"H" peak output current $P2_0$～$P2_7$ (Note 3)			−10	mA
$I_{OH(avg)}$	"H" average output current $P2_0$～$P2_7$ (Note 2)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillator frequency			4	MHz

Note 2 : The average output currents $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.
3 : Do not allow the combined low- level output current of ports P0, P1, P2, P3, P4, P6, and PWM to exceed 80mA.
Do not allow the combined high- level output current of port P2 to exceed 50mA.
4 : "H" input voltage of ports' P0, P1, P3, $P4_0$～$P4_3$, P5 and $\overline{INT_1}$ is available up to +12V.

ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC}=5V, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P2_0$~$P2_7$	I_{OH}=−10mA	3			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA	3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_3$, PWM	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage ϕ	I_{OL}=5mA			2	V
V_{T+}−V_{T-}	Hysteresis $\overline{INT_1}$		0.3		1	V
V_{T+}−V_{T-}	Hysteresis $P3_2$	When used as $\overline{INT_2}$ input	0.3		1	V
V_{T+}−V_{T-}	Hysteresis $P3_3$	When used as CNTR input	0.5	1		V
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$			0.5	0.7	V
V_{T+}−V_{T-}	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=0V			−5	μA
I_{IL}	"L" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I=0V			−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=12V			12	μA
I_{IH}	"H" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, $P2_0$~$P2_7$, $P4_4$~$P4_7$	V_I=5V			5	μA
V_{RAM}	RAM retention voltage	When clock disabled	2			V
I_{CC}	Supply current	ϕ, X_{OUT}, and D-A pins opened, other pins at V_{SS}, and A-D converter in the finished condition. — $f_{X_{IN}}$=4MHz Square wave		3	6	mA
		at clock stop T_a=25°C			1	μA
		at clock stop T_a=75°C			10	μA

A-D CONVERTER CHARACTERISTICS (T_a=25°C, V_{CC}=5V, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute precision	V_{REF}=V_{CC}, with the output transistor cut-off			±3	LSB
R_{LADDER}	Ladder resistance	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS (T_a=25°C, V_{CC}=5V, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF}=V_{CC}			5	Bits
—	Error in full scale range	V_{REF}=V_{CC}, with the output transistor cut-off			±1	%
t_{SU}	Setup time	V_{REF}=V_{CC}			3	μs
R_O	Output resistance	V_{REF}=V_{CC}			3	kΩ
V_{REF}	Reference voltage		4		V_{CC}	V

TIMING REQUIREMENTS

Single-chip mode (T_a=25°C, V_{CC}=5V±10%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time	270			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time	20			ns
t_c	External clock input cycle time	250			ns
t_w	External clock input pulse width	75			ns
t_r	External clock rise-time			25	ns
t_f	External clock fall-time			25	ns

Eva-chip mode (T_a=25°C, V_{CC}=5V±10%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

Memory expanding and microprocessor modes

(T_a=25°C, V_{CC}=5V±10%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	30			ns

SWITCHING CHARACTERISTICS

Single-chip mode (T_a=25°C, V_{CC}=5V±10%, V_{SS}=0V, $f_{X_{IN}}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Typ.	Max.	Unit
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig. 19			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 20			230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time	Fig. 19			230	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				230	ns

Eva-chip mode (T_a=25°C, V_{CC}=5V±10%, V_{SS}=0V, $f_{X_{IN}}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Typ.	Max.	Unit
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 19			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 20			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/W signal output delay time	Fig. 19			250	ns
$t_{d(\phi-R/WF)}$	R/W signal output delay time				250	ns
$t_{d(\phi-P3_0Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				200	ns

Memory expanding and microprocessor modes

(T_a=25°C, V_{CC}=5V±10%, V_{SS}=0V, $f_{X_{IN}}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Typ.	Max.	Unit
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 19			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 20			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/W signal output delay time	Fig. 19			250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

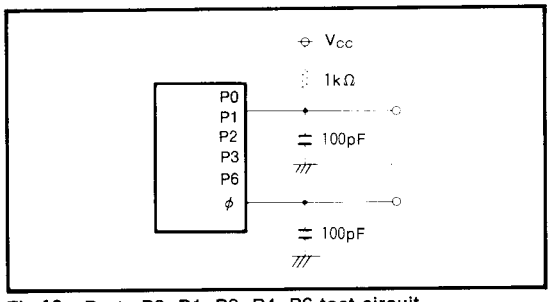


Fig.19 Ports P0, P1, P3, P4, P6 test circuit

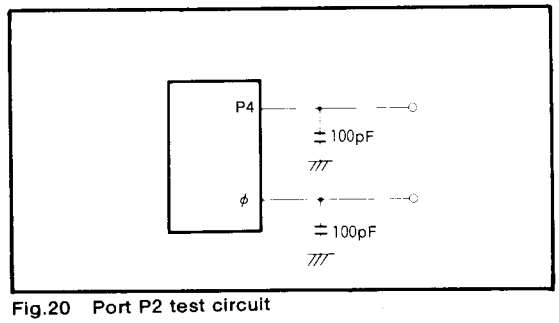
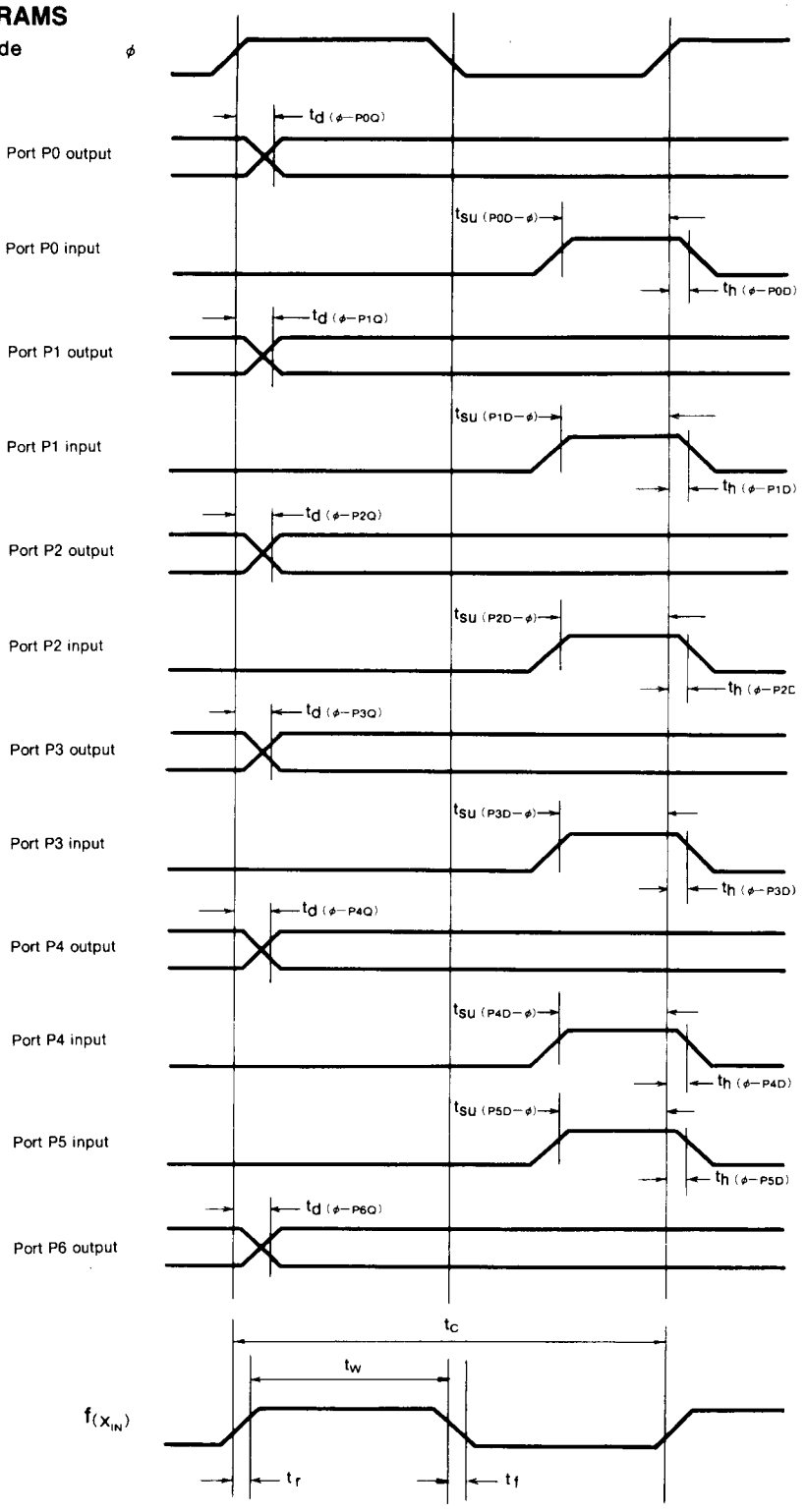


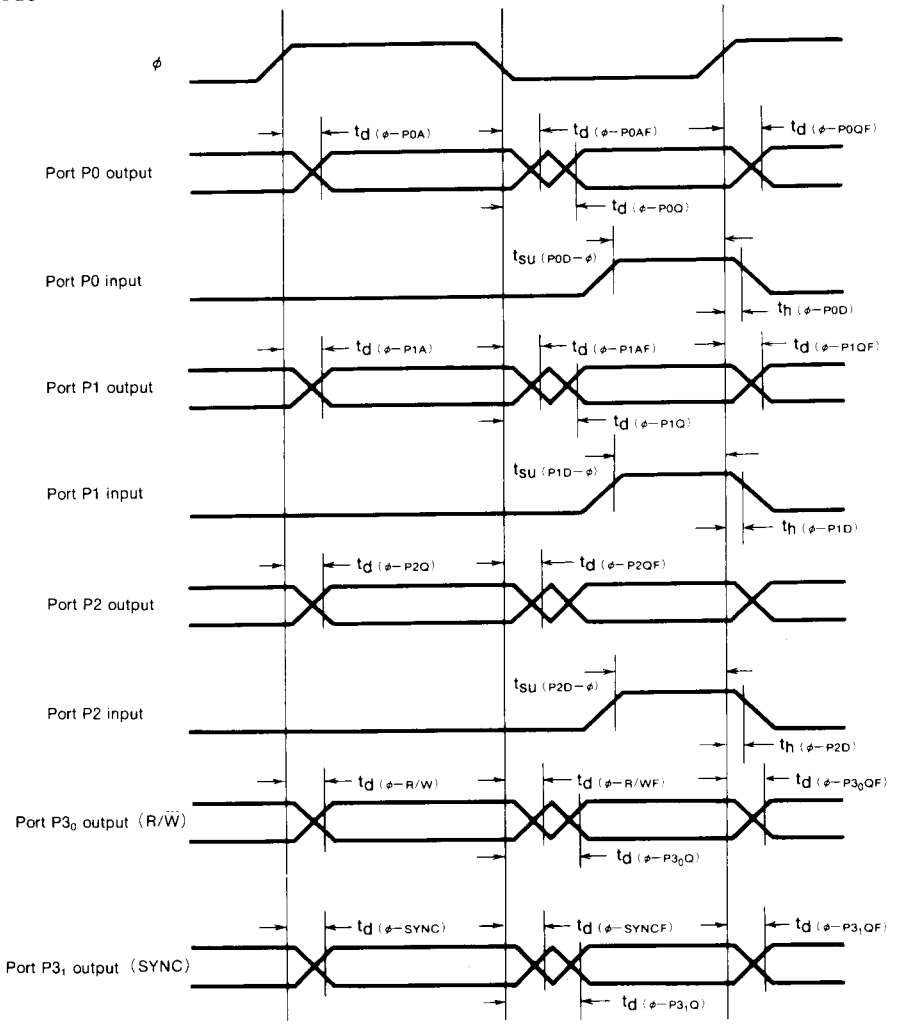
Fig.20 Port P2 test circuit

TIMING DIAGRAMS

In single-chip mode



In eva-chip mode



In memory expanding mode and microprocessor mode