

## CMOS single-chip 8-bit microcontrollers

## 83C51FB/87C51FB

## DESCRIPTION

The 83C51FB/87C51FB (hereafter collectively called 8XC51FB) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC51FB has the same instruction set as the 80C51.

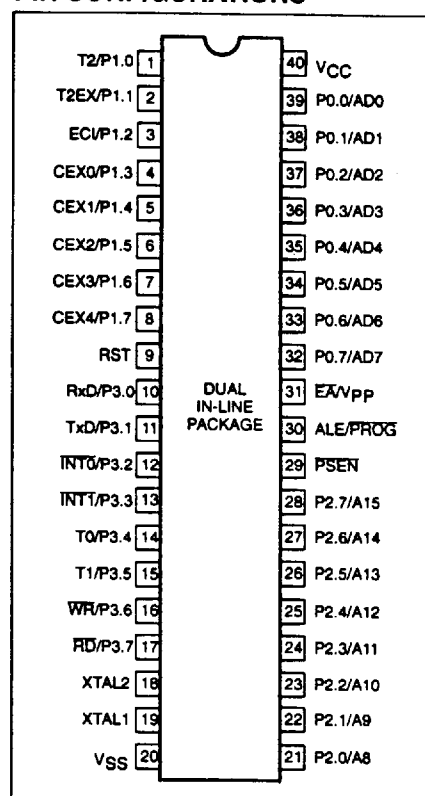
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 87C51FB contains 16k x 8 EPROM memory, the 83C51FB contains 16k x 8 ROM memory, a volatile 256 x 8 read/write data memory, four 8-bit I/O ports, three 16-bit timer/event counters, a Programmable Counter Array (PCA), a multi-source, two-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 87C51FB can be expanded using standard TTL compatible memories and logic.

Its added features make it an even more powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multiprocessor communications.

## FEATURES

- 80C51 central processing unit
- 16k x 8 EPROM expandable externally to 64k bytes (87C51FB)
  - Quick Pulse programming algorithm
  - Two level program security system
- 16k x 8 ROM (83C51FB)
- 256 x 8 RAM, expandable externally to 64k bytes
- Three 16-bit timer/counters
  - T2 is an up/down counter
- Programmable Counter Array (PCA)
  - High speed output
  - Capture/compare
  - Pulse Width Modulator
  - Watchdog Timer
- Four 8-bit I/O ports
- Full-duplex enhanced UART
  - Framing error detection
  - Automatic address recognition
- Power control modes
  - Idle mode
  - Power-down mode
- Once (On Circuit Emulation) Mode
- Five package styles
- OTP package available

## PIN CONFIGURATIONS



## ORDERING INFORMATION

ROM	EPROM		TEMPERATURE RANGE °C AND PACKAGE <sup>1</sup>	FREQ. (MHz)	DRAWING NUMBER
S83C51FB-4N40	S87C51FB-4N40	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	3.5 to 16	0415C
	S87C51FB-4F40	UV	0 to +70, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 16	0590B
S83C51FB-4A44	S87C51FB-4A44	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	3.5 to 16	0403G
	S87C51FB-4K44	UV	0 to +70, 44-Pin Ceramic Leaded Chip Carrier w/Window	3.5 to 16	1472A
S83C51FB-4B44	S87C51FB-4B44	OTP	0 to +70, 44-Pin Plastic Quad Flat Pack	3.5 to 16	1118D
S83C51FB-5N40	S87C51FB-5N40	OTP	-40 to +85, 40-Pin Plastic Dual In-line Package	3.5 to 16	0415C
	S87C51FB-5F40	UV	-40 to +85, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 16	0590B
S83C51FB-5A44	S87C51FB-5A44	OTP	-40 to +85, 44-Pin Plastic Leaded Chip Carrier	3.5 to 16	0403G
	S87C51FB-5K44	UV	-40 to +85, 44-Pin Ceramic Leaded Chip Carrier w/Window	3.5 to 16	1472A
S83C51FB-5B44	S87C51FB-5B44	OTP	-40 to +85, 44-Pin Plastic Quad Flat Pack	3.5 to 16	1118D
S83C51FB-AN40	S87C51FB-AN40	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	3.5 to 24	0415C
	S87C51FB-AF40	UV	0 to +70, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 24	0590B
S83C51FB-AA44	S87C51FB-AA44	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	3.5 to 24	0403G
	S87C51FB-AK44	UV	0 to +70, 44-Pin Ceramic Leaded Chip Carrier w/Window	3.5 to 24	1472A
S83C51FB-BN40	S87C51FB-BN40	OTP	-40 to +85, 40-Pin Plastic Dual In-line Package	3.5 to 24	0415C
	S87C51FB-BF40	UV	-40 to +85, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 24	0590B
S83C51FB-BA44	S87C51FB-BA44	OTP	-40 to +85, 44-Pin Plastic Leaded Chip Carrier	3.5 to 24	0403G
	S87C51FB-BK44	UV	-40 to +85, 44-Pin Ceramic Leaded Chip Carrier w/Window	3.5 to 24	1472A

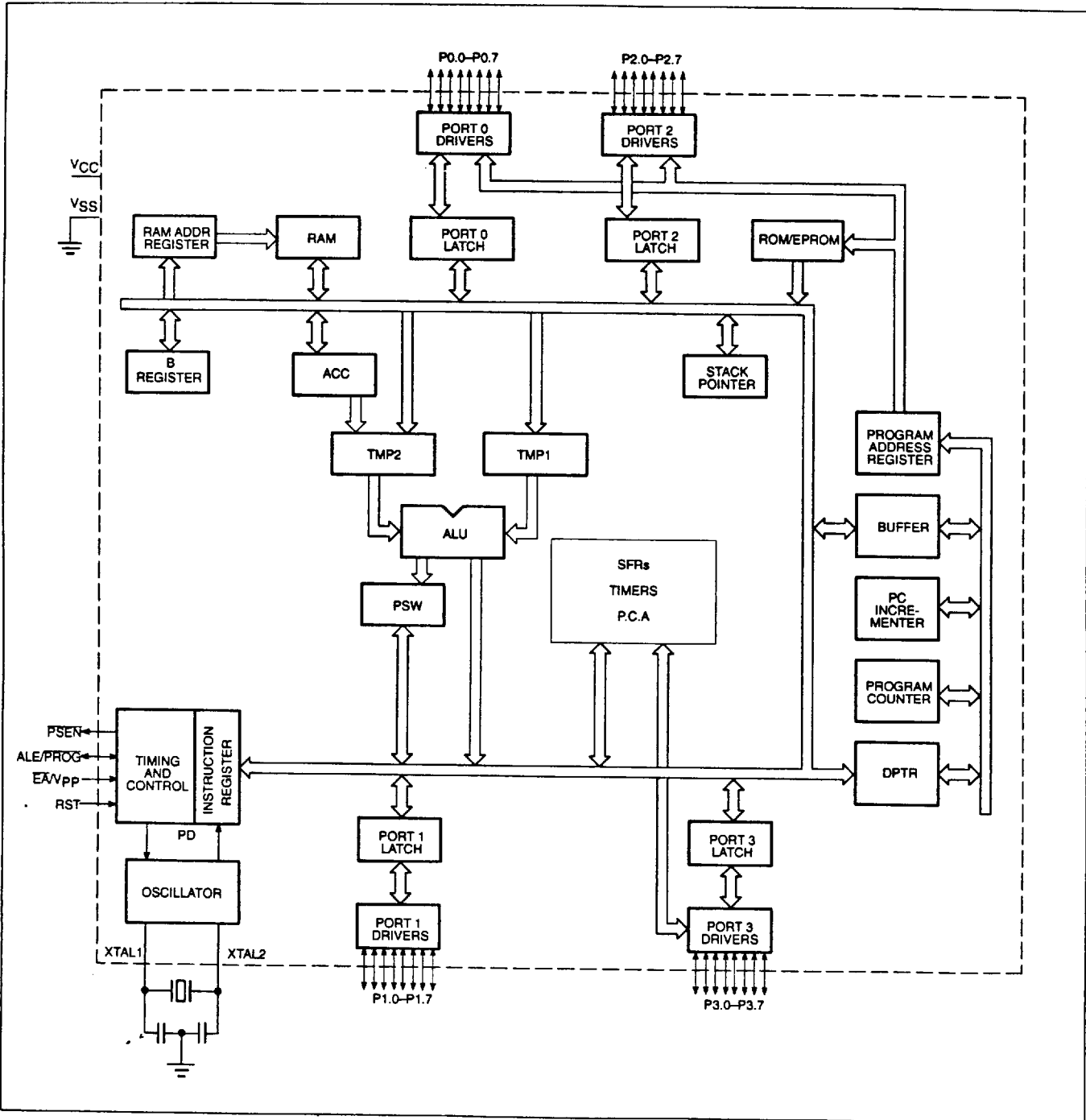
## NOTE:

1. OTP = One Time Programmable EPROM. UV = Erasable EPROM.

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## BLOCK DIAGRAM



CMOS single-chip 8-bit microcontrollers

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Table 1. 8XC51FB Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB							LSB	
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	-	-	-	-	-	-	-	AO	xxxxxx0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
CCAP0H#	Module 0 Capture High	FAH									xxxxxxxxB
CCAP1H#	Module 1 Capture High	FBH									xxxxxxxxB
CCAP2H#	Module 2 Capture High	FCH									xxxxxxxxB
CCAP3H#	Module 3 Capture High	FDH									xxxxxxxxB
CCAP4H#	Module 4 Capture High	FEH									xxxxxxxxB
CCAP0L#	Module 0 Capture Low	EAH									xxxxxxxxB
CCAP1L#	Module 1 Capture Low	EBH									xxxxxxxxB
CCAP2L#	Module 2 Capture Low	ECH									xxxxxxxxB
CCAP3L#	Module 3 Capture Low	EDH									xxxxxxxxB
CCAP4L#	Module 4 Capture Low	EEH									xxxxxxxxB
CCAPM0#	Module 0 Mode	DAH	-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x000000B
CCAPM1#	Module 1 Mode	DBH	-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x000000B
CCAPM2#	Module 2 Mode	DCH	-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x000000B
CCAPM3#	Module 3 Mode	DDH	-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x000000B
CCAPM4#	Module 4 Mode	DEH	-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x000000B
CCON*#	PCA Counter Control	D8H	DF	DE	DD	DC	DB	DA	D9	D8	00x00000B
CH#	PCA Counter High	F9H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	
CL#	PCA Counter Low	E9H									
CMOD#	PCA Counter Mode	D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00xx000B
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
IE*	Interrupt Enable	A8H	AF	AE	AD	AC	AB	AA	A9	A8	00H
			EA	EC	ET2	ES	ET1	EX1	ET0	EX0	
IP*	Interrupt Priority	B8H	BF	BE	BD	BC	BB	BA	B9	B8	x0000000B
			-	PPC	PT2	PS	PT1	PX1	PT0	PX0	
P0*	Port 0	80H	87	86	85	84	83	82	81	80	FFH
			AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
P1*	Port 1	90H	97	96	95	94	93	92	91	90	FFH
			CEX4	CEX3	CEX2	CEX1	CEX0	EX1	T2EX	T2	
P2*	Port 2	A0H	A7	A6	A5	A4	A3	A2	A1	A0	FFH
			AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	
P3*	Port 3	B0H	B7	B6	B5	B4	B3	B2	B1	B0	FFH
			RD	WR	T1	T0	INT1	INT0	TxD	RxD	
PCON	Power Control	87H	SMOD1	SMOD0	-	POF1	GF1	GF0	PD	IDL	00xxxx00B

\* SFRs are bit addressable.

# SFRs are modified from or added to the 80C51 SFRs.

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Table 1. 8XC51FB Special Function Registers (Continued)

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE								
			MSB				LSB												
			D7	D6	D5	D4	D3	D2	D1	D0									
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	-	P	00H								
RACAP2H#	Timer 2 Capture High	CBH									00H								
RACAP2L#	Timer 2 Capture Low	CAH									00H								
SADDR#	Slave Address	A9H									00H								
SADEN#	Slave Address Mask	B9H									00H								
SBUF	Serial Data Buffer	99H									xxxxxxx0B								
SCON*	Serial Control	98H									9F	9E	9D	9C	9B	9A	99	98	
SP	Stack Pointer	81H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H								
TCON*	Timer Control	88H									07H								
											8F	8E	8D	8C	8B	8A	89	88	
T2CON*	Timer 2 Control	C8H									00H								
											TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
T2MOD#	Timer 2 Mode Control	C9H									00H								
											CF	CE	CD	CC	CB	CA	C9	C8	
TH0	Timer High 0	8CH	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00H								
TH1	Timer High 1	8DH	-	-	-	-	-	-	-	DCEN	xxxxxxx0B								
TH2#	Timer High 2	CDH									00H								
TL0	Timer Low 0	8AH									00H								
TL1	Timer Low 1	8BH									00H								
TL2#	Timer Low 2	CCH									00H								
TMOD	Timer Mode	89H									GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
											C7	C6	C5	C4	C3	C2	C1	C0	

\* SFRs are bit addressable.

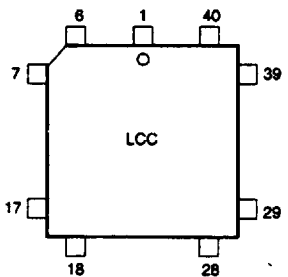
# SFRs are modified from or added to the 80C51 SFRs.

1. Reset value depends on reset source.

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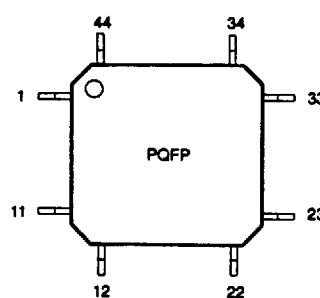
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CERAMIC AND PLASTIC LEADED CHIP CARRIER  
PIN FUNCTIONS



Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0/T2	24	P2.0/A8
3	P1.1/T2EX	25	P2.1/A9
4	P1.2/ECI	26	P2.2/A10
5	P1.3/CEX0	27	P2.3/A11
6	P1.4/CEX1	28	P2.4/A12
7	P1.5/CEX2	29	P2.5/A13
8	P1.6/CEX3	30	P2.6/A14
9	P1.7/CEX4	31	P2.7/A15
10	RST	32	PSEN
11	P3.0/RxD	33	ALE/PROG
12	NC	34	NC
13	P3.1/TxD	35	EA/Vpp
14	P3.2/INT0	36	P0.7/AD7
15	P3.3/INT1	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/WR	40	P0.3/AD3
19	P3.7/RD	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	VSS	44	VCC

PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function
1	NC	23	P2.5/A13
2	P1.5/CEX2	24	P2.6/A14
3	P1.6/CEX3	25	P2.7/A15
4	P1.7/CEX4	26	PSEN
5	RST	27	ALE/PROG
6	P3.0/RxD	28	NC
7	NC	29	EA/Vpp
8	P3.1/TxD	30	P0.7/AD7
9	P3.2/INT0	31	P0.6/AD6
10	P3.3/INT1	32	P0.5/AD5
11	P3.4/T0	33	P0.4/AD4
12	P3.5/T1	34	P0.3/AD3
13	P3.6/WR	35	P0.2/AD2
14	P3.7/RD	36	P0.1/AD1
15	XTAL2	37	P0.0/AD0
16	XTAL1	38	VCC
17	VSS	39	NC
18	NC	40	P1.0/T2
19	P2.0/A8	41	P1.1/T2EX
20	P2.1/A9	42	P1.2/ECI
21	P2.2/A10	43	P1.3/CEX0
22	P2.3/A11	44	P1.4/CEX1

PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIP	LCC	QFP		
Vss	20	22	16	I	Ground: 0V reference.
Vcc	40	44	38	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
P0.0-0.7	39-32	43-36	37-30	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification and receives code bytes during EPROM programming. External pull-ups are required during program verification.
P1.0-P1.7	1-8	2-9	40-44, 1-3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Port 1 also receives the low-order address byte during program memory verification. Alternate functions include:
	1	2	40	I	T2 (P1.0): Timer/Counter 2 external count input/Clockout
	2	3	41	I	T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control
	3	4	42	I	ECI (P1.2): External Clock Input to the PCA
	4	5	43	I/O	CEX0 (P1.3): Capture/Compare External I/O for PCA module 0
	5	6	44	I/O	CEX1 (P1.4): Capture/Compare External I/O for PCA module 1
	6	7	1	I/O	CEX2 (P1.5): Capture/Compare External I/O for PCA module 2
	7	8	2	I/O	CEX3 (P1.6): Capture/Compare External I/O for PCA module 3
	8	9	3	I/O	CEX4 (P1.7): Capture/Compare External I/O for PCA module 4

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## PIN DESCRIPTIONS (Continued)

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIP	LCC	QFP		
P2.0-P2.7	21-28	24-31	18-25	I/O	<b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: $I_{IL}$ ). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. Some Port 2 pins receive the high order address bits during EPROM programming and verification.
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	<b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: $I_{IL}$ ). Port 3 also serves the special features of the 80C51 family, as listed below: <b>RxD (P3.0):</b> Serial input port <b>TxD (P3.1):</b> Serial output port <b>INT0 (P3.2):</b> External interrupt <b>INT1 (P3.3):</b> External interrupt <b>T0 (P3.4):</b> Timer 0 external input <b>T1 (P3.5):</b> Timer 1 external input <b>WR (P3.6):</b> External data memory write strobe <b>RD (P3.7):</b> External data memory read strobe
RST	9	10	4	I	<b>Reset:</b> A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to $V_{SS}$ permits a power-on reset using only an external capacitor to $V_{CC}$ .
ALE/PROG	30	33	27	I/O	<b>Address Latch Enable/Program Pulse:</b> Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming.
PSEN	29	32	26	O	<b>Program Store Enable:</b> The read strobe to external program memory. When the 87C51FB is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
EA/ $V_{PP}$	31	35	29	I	<b>External Access Enable/Programming Supply Voltage:</b> EA must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH. This pin also receives the 12.75V programming supply voltage ( $V_{PP}$ ) during EPROM programming. If security bit 1 is programmed, EA will be internally latched on Reset.
XTAL1	19	21	15	I	<b>Crystal 1:</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	<b>Crystal 2:</b> Output from the inverting oscillator amplifier.

## NOTE:

To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than  $V_{CC} + 0.5V$  or  $V_{SS} - 0.5V$ , respectively.

## TIMER 2

This is a 16-bit up or down counter, which can be operated as either a timer or event counter. It can be operated in one of three different modes (autoreload, capture or as the baud rate generator for the UART).

In the autoreload mode the Timer can be set to count up or down by setting or clearing the bit DCEN in the T2CON Special Function Register. The SFR's RCAP2H and RCAP2L are used to reload the Timer upon overflow or a 1-to-0 transition on the T2EX input (P1.1).

In the Capture mode Timer 2 can either set TF2 and generate an interrupt or capture its value. To capture Timer 2 in response to a 1-to-0 transition on the T2EX input, the EXEN2 bit in the T2CON must be set. Timer 2 is then captured in SFR's RCAP2H and RCAP2L.

As the baud rate generator, Timer 2 is selected by setting TCLK and/or RCLK in T2CON. As the baud rate generator Timer 2 is incremented at  $1/2$  the oscillator frequency.

## POWER OFF FLAG

The Power Off Flag (POF) is set by on-chip circuitry when the  $V_{CC}$  level on the 87C51FB rises from 0 to 5V. The POF bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after powerdown. The  $V_{CC}$  level must remain above 3V for the POF to remain unaffected by the  $V_{CC}$  level.

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**OSCILLATOR CHARACTERISTICS**

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

**Reset**

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V<sub>CC</sub> and RST must come up at the same time for a proper start-up.

**Idle Mode**

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle

mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

**Power-Down Mode**

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 87C51FB either a hardware reset or external interrupt can use an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V<sub>CC</sub> is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the

instruction that put the device into Power Down.

**Design Consideration**

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

**ONCE™ Mode**

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 87C51FB without the 87C51FB having to be removed from the circuit. The ONCE Mode is invoked by:

- Pull ALE low while the device is in reset and PSEN is high;
- Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and PSEN are weakly pulled high. The oscillator circuit remains active. While the 87C51FB is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

**Table 2. External Pin Status During Idle and Power-Down Mode**

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

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**Programmable Counter Array (PCA)**

The Programmable Counter Array is a special Timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3(CEX0), module 1 to P1.4(CEX1), etc. The basic PCA configuration is shown in Figure 1.

The PCA timer is a common time base for all five modules and can be programmed to run at: 1/12 the oscillator frequency, 1/4 the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P1.2). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see Figure 4):

CPS1	CPS0	PCA Timer Count Source
0	0	1/12 oscillator frequency
0	1	1/4 oscillator frequency
1	0	Timer 0 overflow
1	1	External Input at ECI pin

In the CMOD SFR are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during idle mode, WDTE which enables or disables the watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to

be set when the PCA timer overflows. These functions are shown in Figure 2.

The watchdog timer function is implemented in module 4 as implemented in other parts that have a PCA that are available on the market. However, if a watchdog timer is required in the target application, it is recommended to use the hardware watchdog timer that is implemented on the 8XC51FB separately from the PCA (see Figure 12).

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (refer to Figure 5). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software. The PCA interrupt system shown in Figure 3.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (see Figure 6). The registers contain the bits that control the mode that each module will operate in. The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or

4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function. Figure 7 shows the CCAPMn settings for the various PCA functions.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

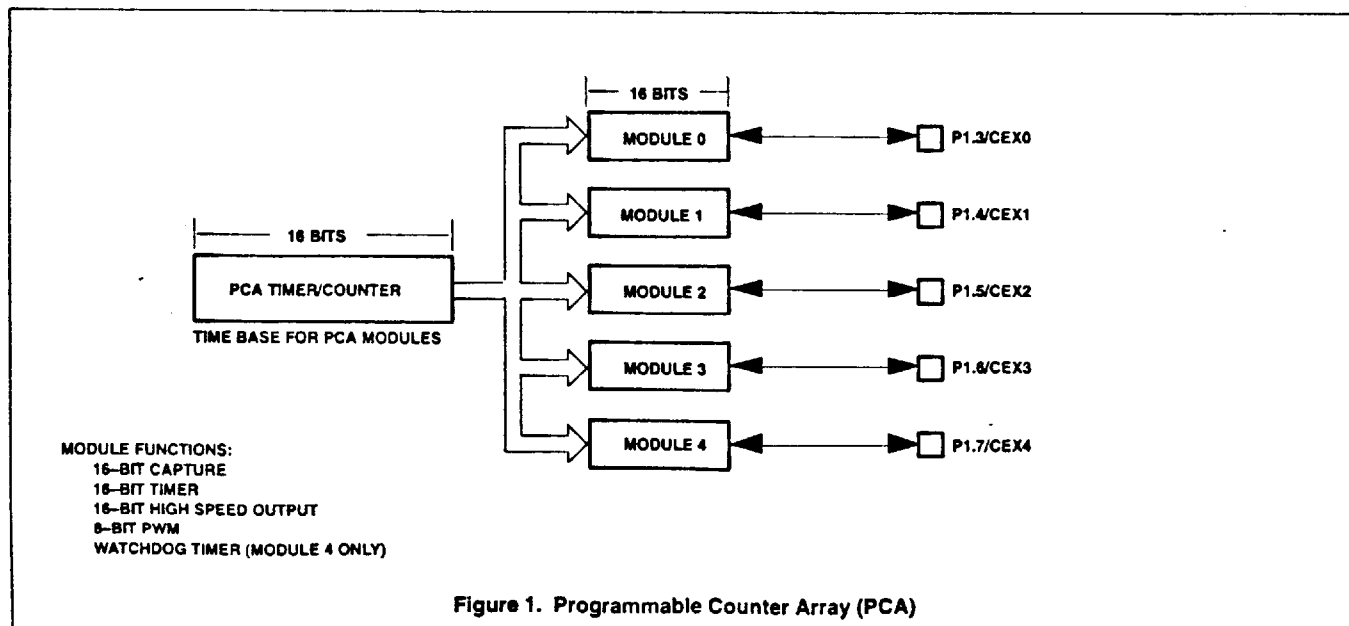


Figure 1. Programmable Counter Array (PCA)

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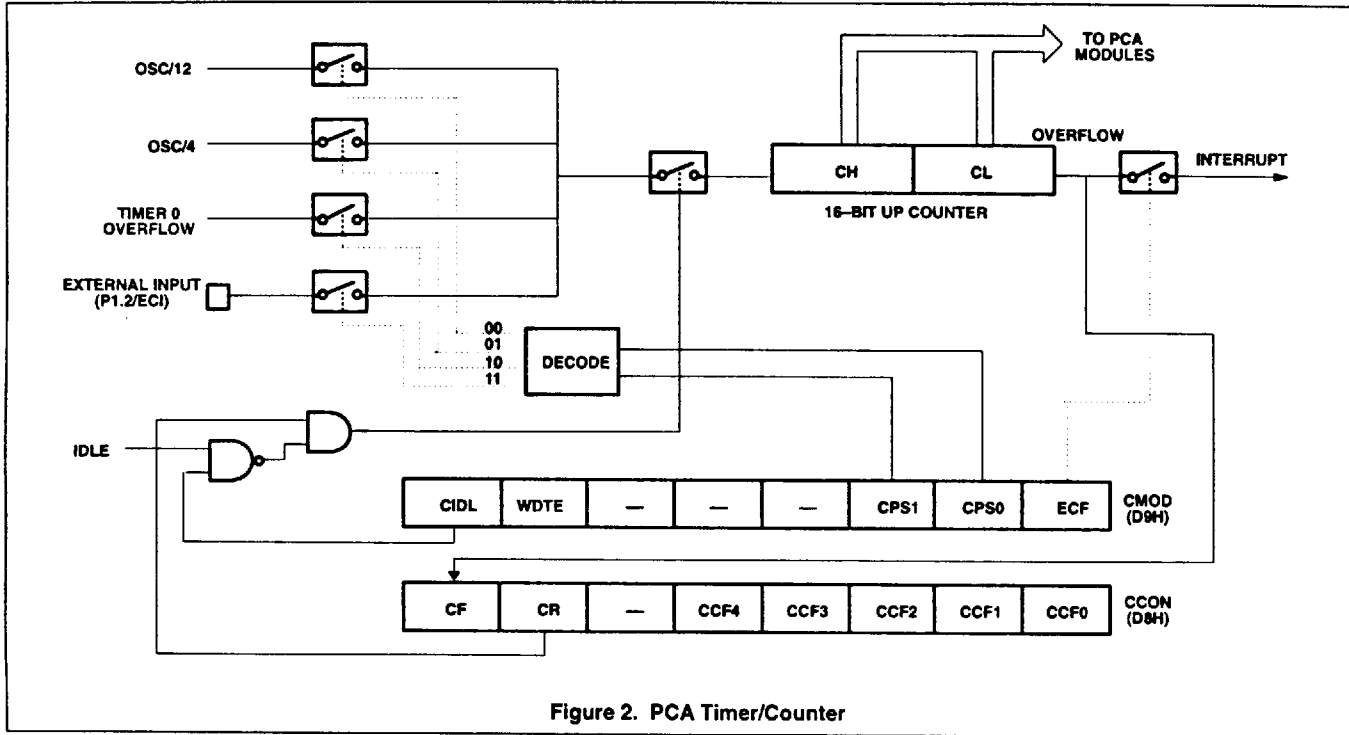


Figure 2. PCA Timer/Counter

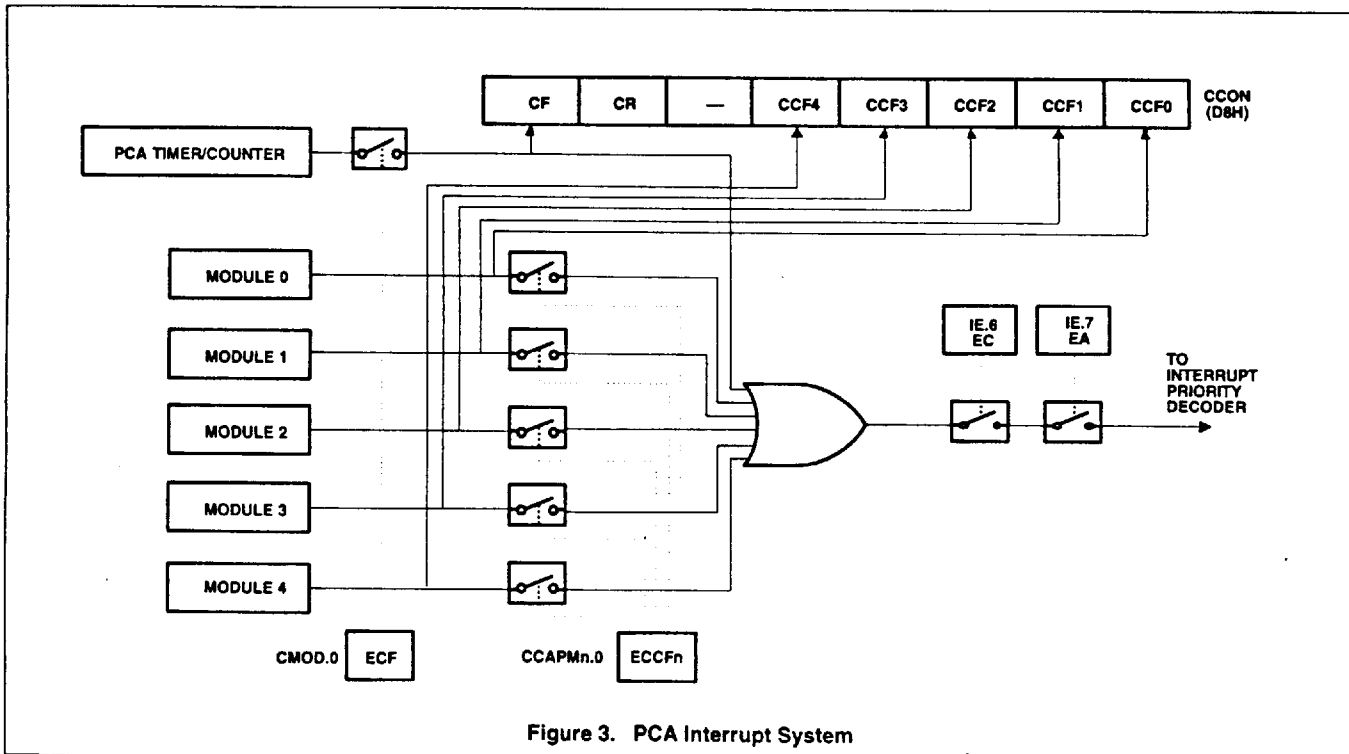
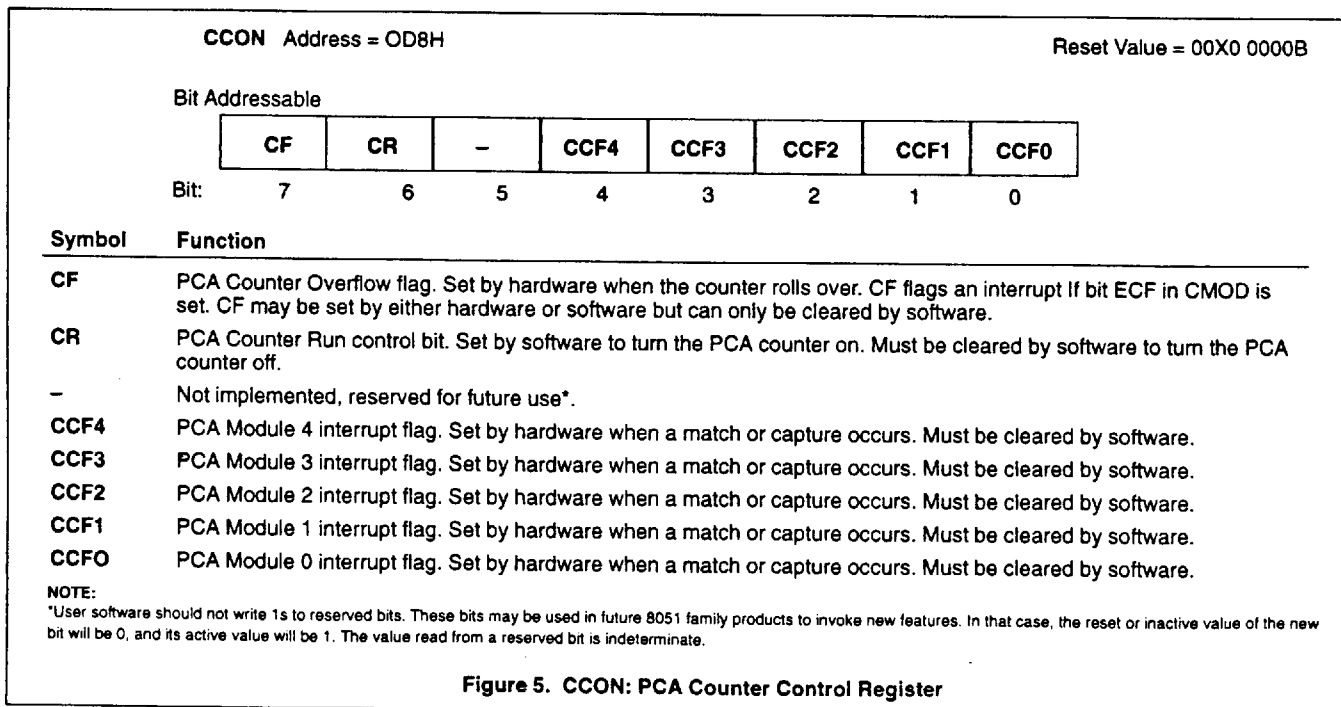
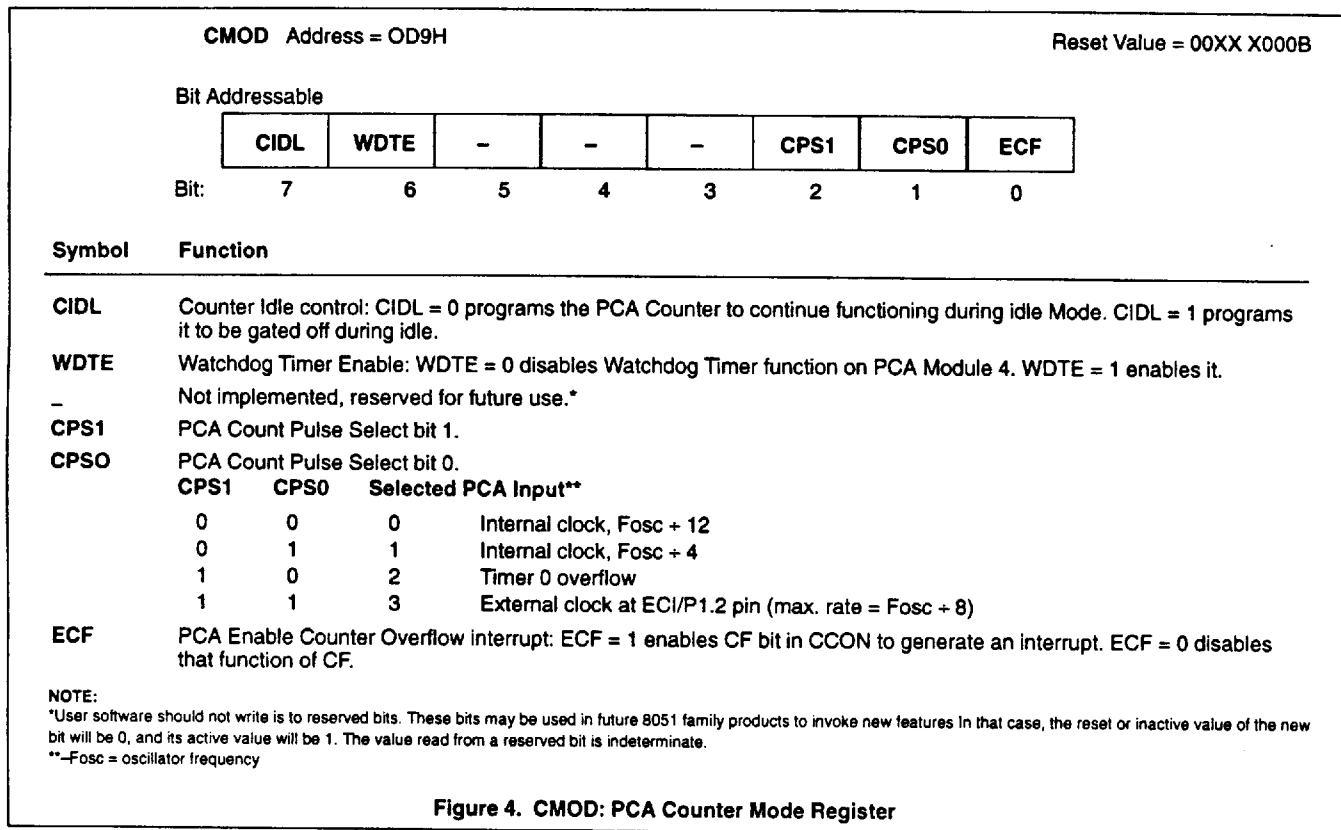


Figure 3. PCA Interrupt System

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—	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	MODULE FUNCTION
X	0	0	0	0	0	0	0	No operation
X	X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
X	1	0	0	1	0	0	X	16-bit Software Timer
X	1	0	0	1	1	0	X	16-bit High Speed Output
X	1	0	0	0	0	1	0	8-bit PWM
X	1	0	0	1	X	0	X	Watchdog Timer

Figure 7. PCA Module Modes (CCAPMn Register)

**Automatic Address Recognition**

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 15.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the

SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

```
Slave 0   SADDR = 1100 0000
          SADEN = 1111 1101
          Given  = 1100 00X0

Slave 1   SADDR = 1100 0000
          SADEN = 1111 1110
          Given  = 1100 000X
```

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

```
Slave 0   SADDR = 1100 0000
          SADEN = 1111 1001
          Given  = 1100 0XX0

Slave 1   SADDR = 1110 0000
          SADEN = 1111 1010
          Given  = 1110 0X0X

Slave 2   SADDR = 1110 0000
          SADEN = 1111 1100
          Given  = 1110 00XX
```

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

**Reduced EMI Mode**

The AO bit (AUXR.O) in the AUXR register when set disables the ALE output.

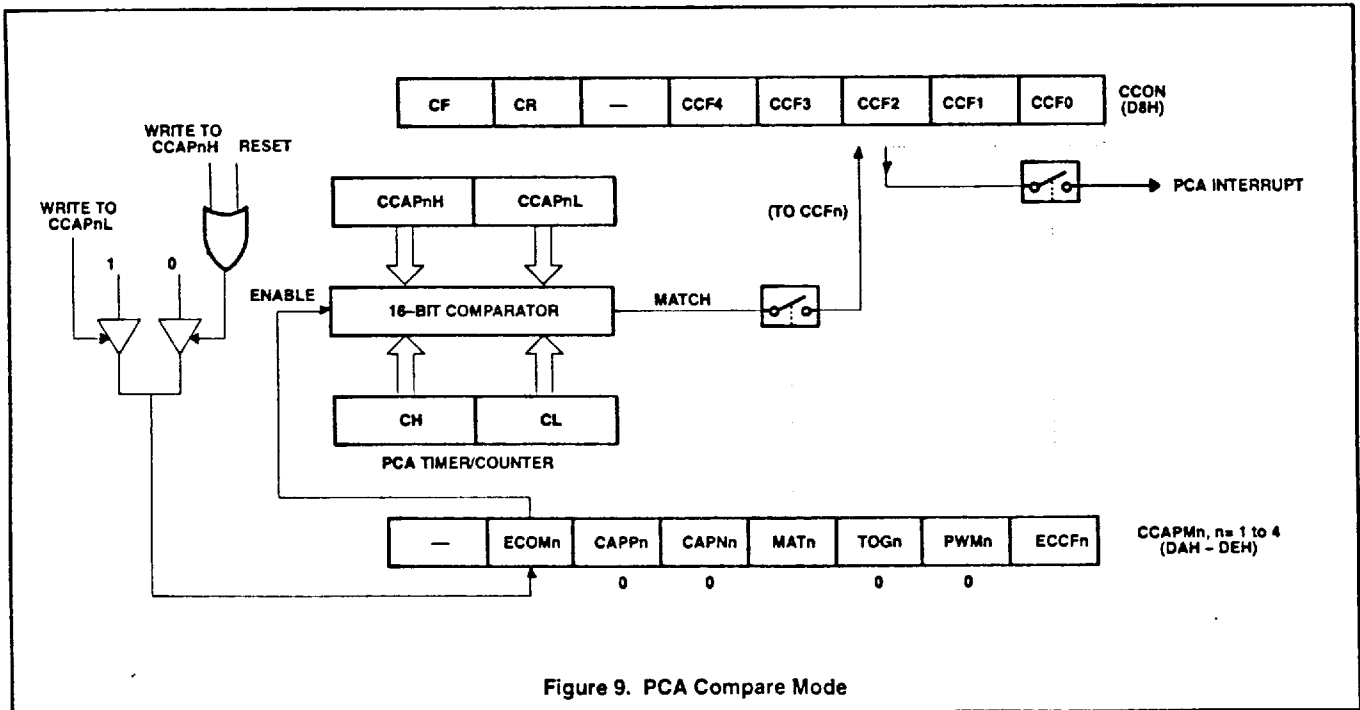
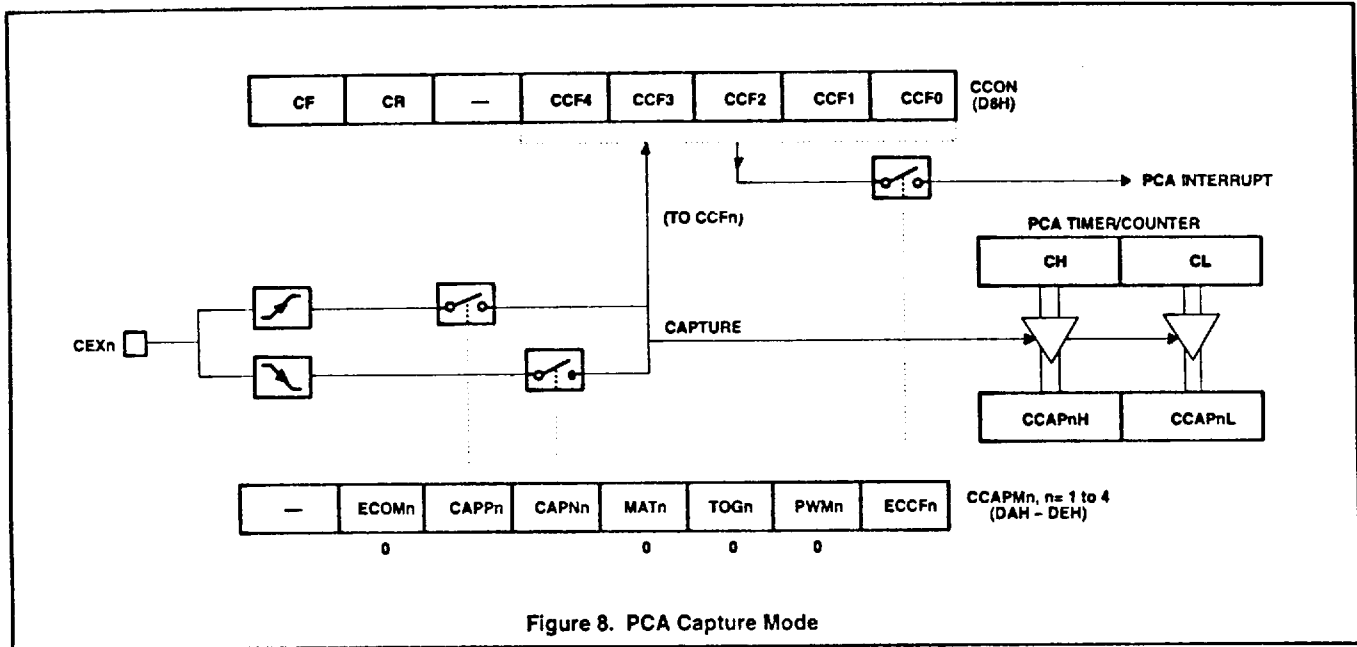
**8XC51FB Reduced EMI Mode****AUXR (0X8E)**

—	—	—	—	—	—	—	—	AO
---	---	---	---	---	---	---	---	----

AO: Turns off ALE output.

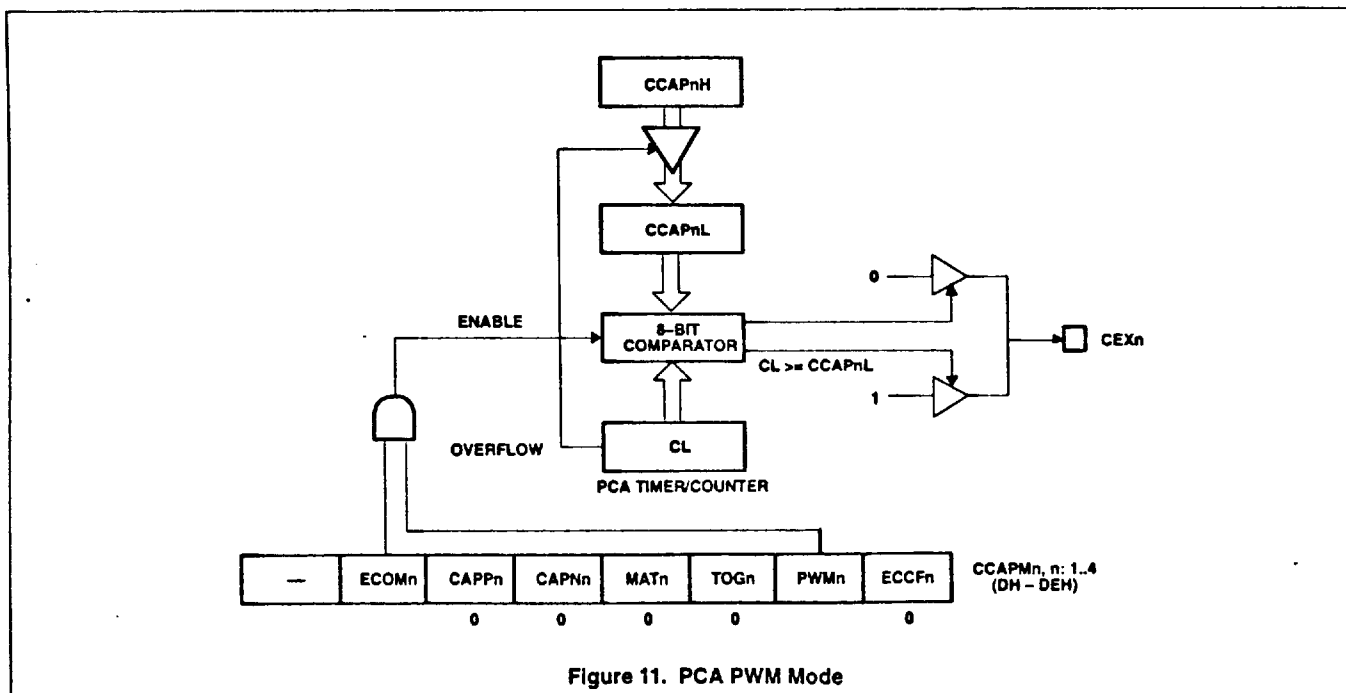
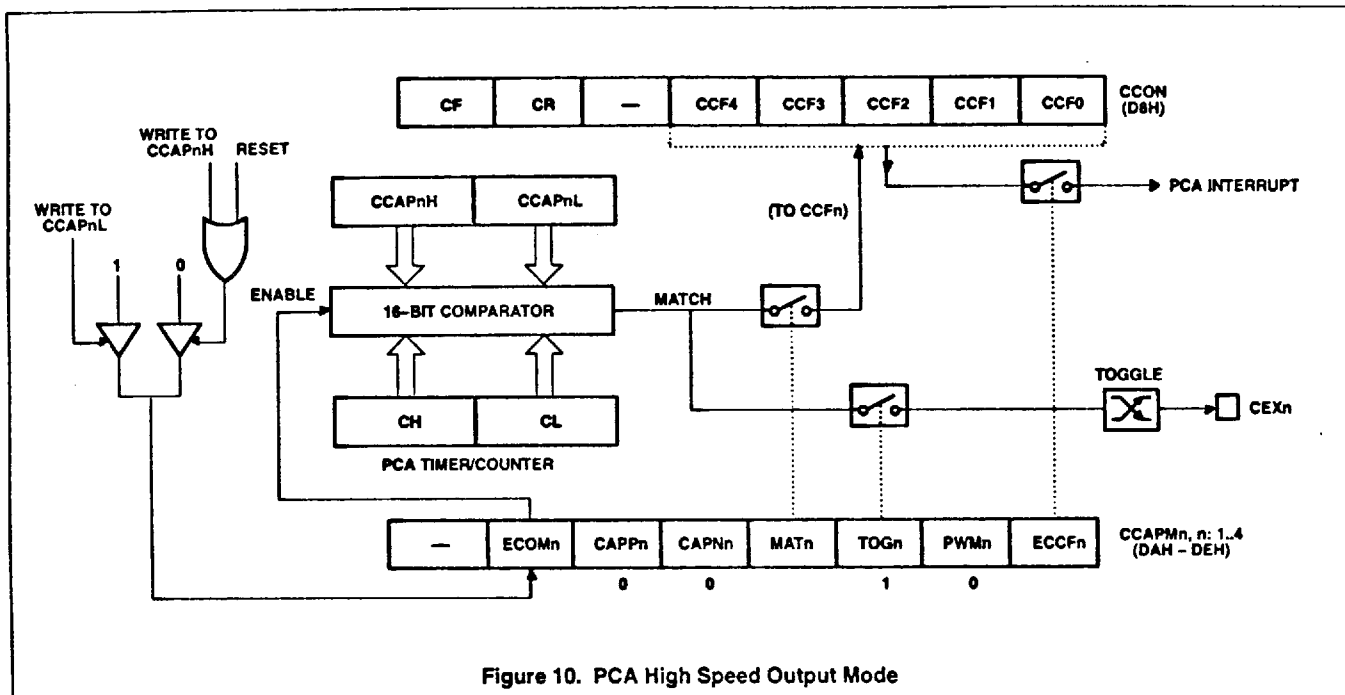
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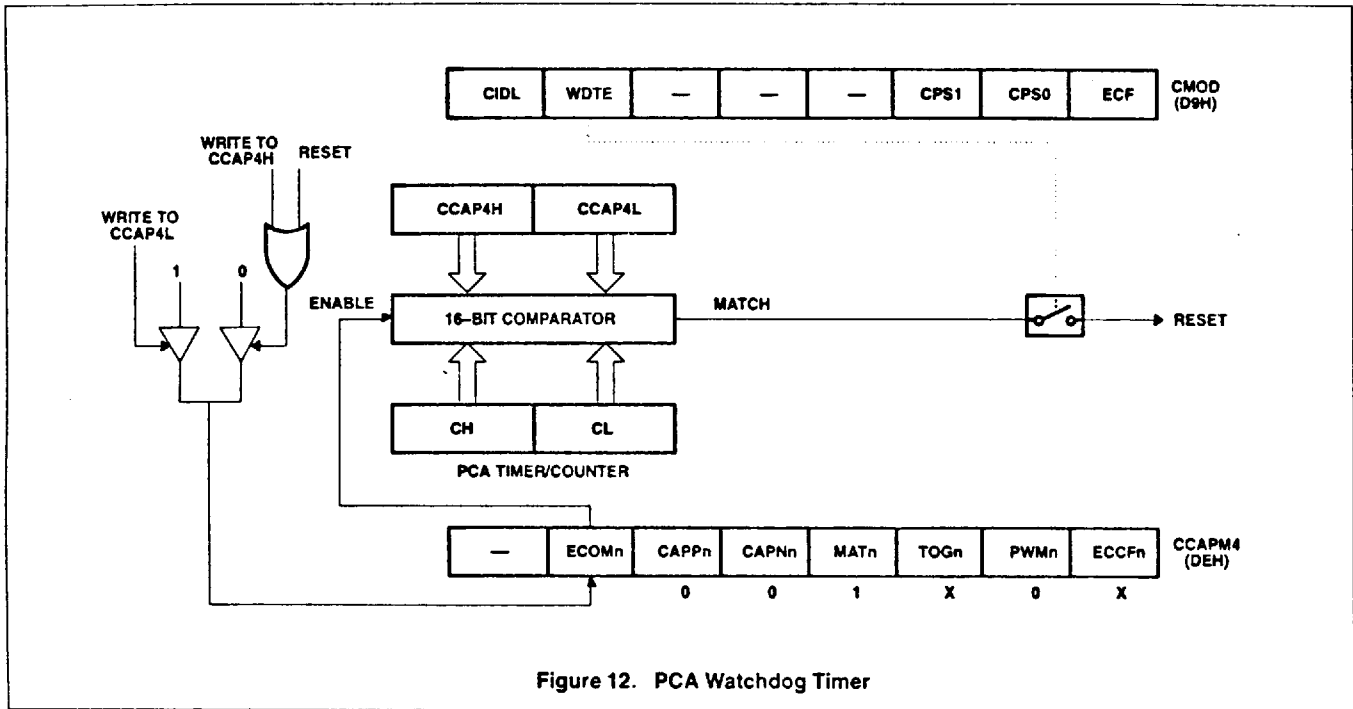


Figure 12. PCA Watchdog Timer

SCON Address = 98H Reset Value = 0000 000B

Bit Addressable

	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
Bit:	7	6	5	4	3	2	1	0

(SMOD0 = 0/1)\*

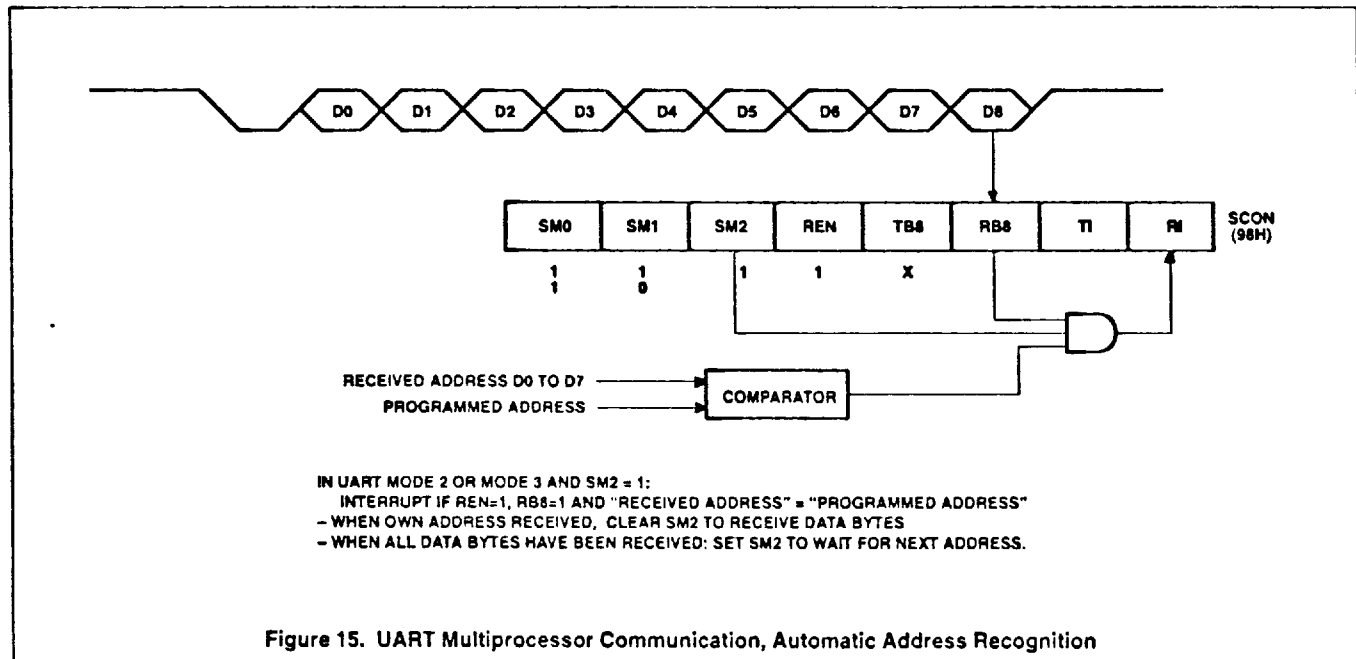
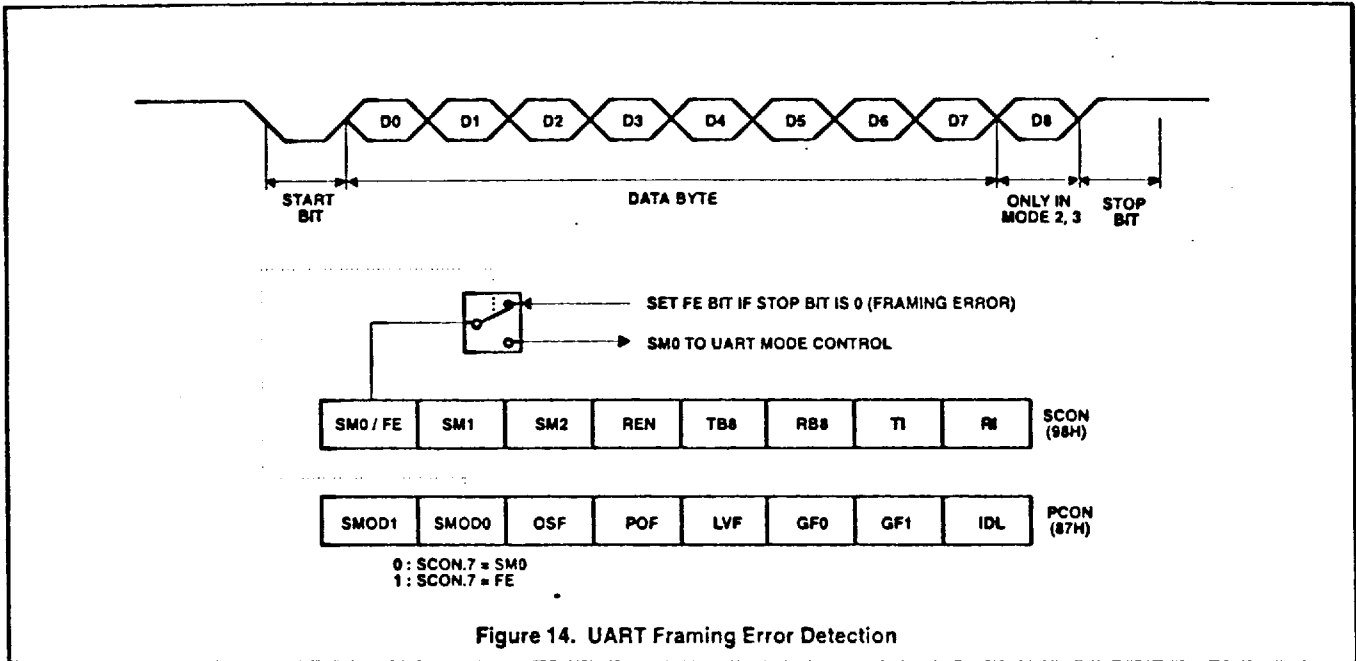
Symbol	Function																									
<b>FE</b>	Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit.																									
<b>SM0</b>	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)																									
<b>SM1</b>	Serial Port Mode Bit 1																									
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>SM0</th> <th>SM1</th> <th>Mode</th> <th>Description</th> <th>Baud Rate**</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>shift register</td> <td>Fosc/12</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>8-bit UART</td> <td>variable</td> </tr> <tr> <td>1</td> <td>0</td> <td>2</td> <td>9-bit UART</td> <td>Fosc/64 or Fosc/32</td> </tr> <tr> <td>1</td> <td>1</td> <td>3</td> <td>9-bit UART</td> <td>variable</td> </tr> </tbody> </table>	SM0	SM1	Mode	Description	Baud Rate**	0	0	0	shift register	Fosc/12	0	1	1	8-bit UART	variable	1	0	2	9-bit UART	Fosc/64 or Fosc/32	1	1	3	9-bit UART	variable
SM0	SM1	Mode	Description	Baud Rate**																						
0	0	0	shift register	Fosc/12																						
0	1	1	8-bit UART	variable																						
1	0	2	9-bit UART	Fosc/64 or Fosc/32																						
1	1	3	9-bit UART	variable																						
<b>SM2</b>	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.																									
<b>REN</b>	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.																									
<b>TB8</b>	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.																									
<b>RB8</b>	In modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.																									
<b>TI</b>	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.																									
<b>RI</b>	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.																									

NOTE:  
 \*SMOD0 is located at PCON6.  
 \*\*Fosc = oscillator frequency

Figure 13. SCON: Serial Port Control Register

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ABSOLUTE MAXIMUM RATINGS<sup>1, 2, 3</sup>

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or -40 to +85	°C
Storage temperature range	-65 to +150	°C
Voltage on EA/V <sub>PP</sub> pin to V <sub>SS</sub>	0 to +13.0	V
Voltage on any other pin to V <sub>SS</sub>	-0.5 to +6.5	V
Maximum I <sub>OL</sub> per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V<sub>SS</sub> unless otherwise noted.

Electrical Deviations from Commercial Specifications for Extended Temperature Range

DC and AC parameters not included here are the same as in the commercial temperature range table.

DC ELECTRICAL CHARACTERISTICS

T<sub>amb</sub> = -40°C to +85°C, V<sub>CC</sub> = 5V ±10%, V<sub>SS</sub> = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V <sub>IL</sub>	Input low voltage, except EA		-0.5	0.2V <sub>CC</sub> -0.15	V
V <sub>IL1</sub>	Input low voltage to EA		0	0.2V <sub>CC</sub> -0.35	V
V <sub>IH</sub>	Input high voltage, except XTAL1, RST		0.2V <sub>CC</sub> +1	V <sub>CC</sub> +0.5	V
V <sub>IH1</sub>	Input high voltage to XTAL1, RST		0.7V <sub>CC</sub> +0.1	V <sub>CC</sub> +0.5	V
I <sub>IL</sub>	Logical 0 input current, ports 1, 2, 3	V <sub>IN</sub> = 0.45V		-75	μA
I <sub>TL</sub>	Logical 1-to-0 transition current, ports 1, 2, 3	V <sub>IN</sub> = 2.0V		-750	μA
I <sub>CC</sub>	Power supply current: Active mode Idle mode Power-down mode	V <sub>CC</sub> = 4.5-5.5V, Frequency range = 3.5 to 16MHz		19 6 50	mA mA μA

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DC ELECTRICAL CHARACTERISTICS

T<sub>amb</sub> = 0°C to +70°C or -40°C to +85°C, V<sub>CC</sub> = 5V ±10%, V<sub>SS</sub> = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IL</sub>	Input low voltage, except EA <sup>7</sup>		-0.5		0.2V <sub>CC</sub> -0.1	V
V <sub>IL1</sub>	Input low voltage to EA <sup>7</sup>		0		0.2V <sub>CC</sub> -0.3	V
V <sub>IH</sub>	Input high voltage, except XTAL1, RST <sup>7</sup>		0.2V <sub>CC</sub> +0.9		V <sub>CC</sub> +0.5	V
V <sub>IH1</sub>	Input high voltage, XTAL1, RST <sup>7</sup>		0.7V <sub>CC</sub>		V <sub>CC</sub> +0.5	V
V <sub>OL</sub>	Output low voltage, ports 1, 2, 3 <sup>9</sup>	I <sub>OL</sub> = 100µA I <sub>OL</sub> = 1.6mA <sup>2</sup> I <sub>OL</sub> = 3.5mA			0.3	V
					0.45	V
					1.0	V
V <sub>OL1</sub>	Output low voltage, port 0, ALE, PSEN <sup>9</sup>	I <sub>OL</sub> = 200µA I <sub>OL</sub> = 3.2mA <sup>2</sup> I <sub>OL</sub> = 7.0mA			0.3	V
					0.45	V
					1.0	V
V <sub>OH</sub>	Output high voltage, ports 1, 2, 3, ALE, PSEN <sup>3</sup>	I <sub>OH</sub> = -60µA, I <sub>OH</sub> = -30µA I <sub>OH</sub> = -10µA	V <sub>CC</sub> - 1.5			V
			V <sub>CC</sub> - 0.7			V
			V <sub>CC</sub> - 0.3			V
V <sub>OH1</sub>	Output high voltage (port 0 in external bus mode), ALE <sup>10</sup> , PSEN <sup>3</sup>	I <sub>OH</sub> = -7.0mA, I <sub>OH</sub> = -3.2mA I <sub>OH</sub> = -200µA	V <sub>CC</sub> - 1.5			V
			V <sub>CC</sub> - 0.7			V
			V <sub>CC</sub> - 0.3			V
I <sub>IL</sub>	Logical 0 input current, ports 1, 2, 3 <sup>7</sup>	V <sub>IN</sub> = 0.45V			-50	µA
I <sub>TL</sub>	Logical 1-to-0 transition current, ports 1, 2, 3 <sup>7</sup>	See note 4			-650	µA
I <sub>LI</sub>	Input leakage current, port 0	0.45 V <sub>IN</sub> < V <sub>CC</sub> - 0.3			±10	µA
I <sub>CC</sub>	Power supply current: <sup>7</sup> Active mode @ 16MHz <sup>5</sup> Idle mode @ 16MHz Power-down mode	See note 6		15	25	mA
				3	5	mA
				10	50	µA
R <sub>RST</sub>	Internal reset pull-down resistor		50		225	kΩ
C <sub>IO</sub>	Pin capacitance <sup>11</sup> (except EA)				15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V<sub>OL</sub>s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I<sub>OL</sub> can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V<sub>OH</sub> on ALE and PSEN to momentarily fall below the 0.9V<sub>CC</sub> specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V<sub>IN</sub> is approximately 2V.
- I<sub>CCMAX</sub> at other frequencies is given by: Active mode: I<sub>CCMAX</sub> = 1.50 × FREQ + 8; Idle mode: I<sub>CCMAX</sub> = 0.14 × FREQ + 2.31, where FREQ is the external oscillator frequency in MHz. I<sub>CCMAX</sub> is given in mA. See Figure 23.
- See Figures 24 through 27 for I<sub>CC</sub> test conditions.
- These values apply only to T<sub>amb</sub> = 0°C to +70°C. For T<sub>amb</sub> = -40°C to +85°C, see table on previous page.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- Under steady state (non-transient) conditions, I<sub>OL</sub> must be externally limited as follows:  
 Maximum I<sub>OL</sub> per port pin: 15mA (\*NOTE: This is 85°C specification.)  
 Maximum I<sub>OL</sub> per 8-bit port: 26mA  
 Maximum total I<sub>OL</sub> for all outputs: 71mA  
 If I<sub>OL</sub> exceeds the test condition, V<sub>OL</sub> may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V<sub>OH1</sub>, except when ALE is off then V<sub>OH</sub> is the voltage specification.
- Pin capacitance is less than 25pF. Pin capacitance of ceramic package is less than 15pF (except EA it is 25pF).

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## AC ELECTRICAL CHARACTERISTICS

 $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C or } -40^{\circ}\text{C to } +85^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}^{1, 2, 3}$ 

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	16	Oscillator frequency -4 -5 -A -B			3.5 3.5	16 24	MHz MHz
$t_{LHLL}$	16	ALE pulse width	85		$2t_{CLCL}-40$		ns
$t_{AVLL}$	16	Address valid to ALE low	22		$t_{CLCL}-40$		ns
$t_{LLAX}$	16	Address hold after ALE low	32		$t_{CLCL}-30$		ns
$t_{LLIV}$	16	ALE low to valid instruction in		150		$4t_{CLCL}-100$	ns
$t_{LLPL}$	16	ALE low to PSEN low	32		$t_{CLCL}-30$		ns
$t_{PLPH}$	16	PSEN pulse width	142		$3t_{CLCL}-45$		ns
$t_{PLIV}$	16	PSEN low to valid instruction in		82		$3t_{CLCL}-105$	ns
$t_{PXIX}$	16	Input instruction hold after PSEN	0		0		ns
$t_{PXIZ}$	16	Input instruction float after PSEN		37		$t_{CLCL}-25$	ns
$t_{AVIV}$	16	Address to valid instruction in		207		$5t_{CLCL}-105$	ns
$t_{PLAZ}$	16	PSEN low to address float		10		10	ns
<b>Data Memory</b>							
$t_{RLAH}$	17, 18	RD pulse width	275		$6t_{CLCL}-100$		ns
$t_{WLWH}$	17, 18	WR pulse width	275		$6t_{CLCL}-100$		ns
$t_{RLDV}$	17, 18	RD low to valid data in		147		$5t_{CLCL}-165$	ns
$t_{RHDX}$	17, 18	Data hold after RD	0		0		ns
$t_{RHDX}$	17, 18	Data float after RD		65		$2t_{CLCL}-60$	ns
$t_{LLDV}$	17, 18	ALE low to valid data in		350		$8t_{CLCL}-150$	ns
$t_{AVDV}$	17, 18	Address to valid data in		397		$9t_{CLCL}-165$	ns
$t_{LLWL}$	17, 18	ALE low to RD or WR low	137	237	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
$t_{AVWL}$	17, 18	Address valid to WR low or RD low	175		$4t_{CLCL}-75$		ns
$t_{QVWX}$	17, 18	Data valid to WR transition	42		$t_{CLCL}-20$		ns
$t_{WHQX}$	17, 18	Data hold after WR	42		$t_{CLCL}-20$		ns
$t_{QVWH}$	18	Data valid to WR high	287		$7t_{CLCL}-150$		ns
$t_{RLAZ}$	17, 18	RD low to address float		0		0	ns
$t_{WHLH}$	17, 18	RD or WR high to ALE high	40	87	$t_{CLCL}-20$	$t_{CLCL}+25$	ns
<b>External Clock</b>							
$t_{CHCX}$	20	High time	12		20		ns
$t_{CLCX}$	20	Low time	12		20		ns
$t_{CLCH}$	20	Rise time		20		20	ns
$t_{CHCL}$	20	Fall time		20		20	ns
<b>Shift Register</b>							
$t_{XLXL}$	19	Serial port clock cycle time	1		$12t_{CLCL}$		$\mu\text{s}$
$t_{QVXH}$	19	Output data setup to clock rising edge	492		$10t_{CLCL}-133$		ns
$t_{XHQX}$	19	Output data hold after clock rising edge	8		$2t_{CLCL}-117$		ns
$t_{XHDX}$	19	Input data hold after clock rising edge	0		0		ns
$t_{XHDX}$	19	Clock rising edge to input data valid		492		$10t_{CLCL}-133$	ns

## NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- Interfacing the 87C51FB to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.

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EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:  
 A - Address  
 C - Clock  
 D - Input data  
 H - Logic level high  
 I - Instruction (program memory contents)  
 L - Logic level low, or ALE

P - PSEN  
 Q - Output data  
 R - RD signal  
 t - Time  
 V - Valid  
 W - WR signal  
 X - No longer a valid logic level  
 Z - Float  
 Examples:  $t_{AVLL}$  = Time for address valid to ALE low.  
 $t_{LLPL}$  = Time for ALE low to PSEN low.

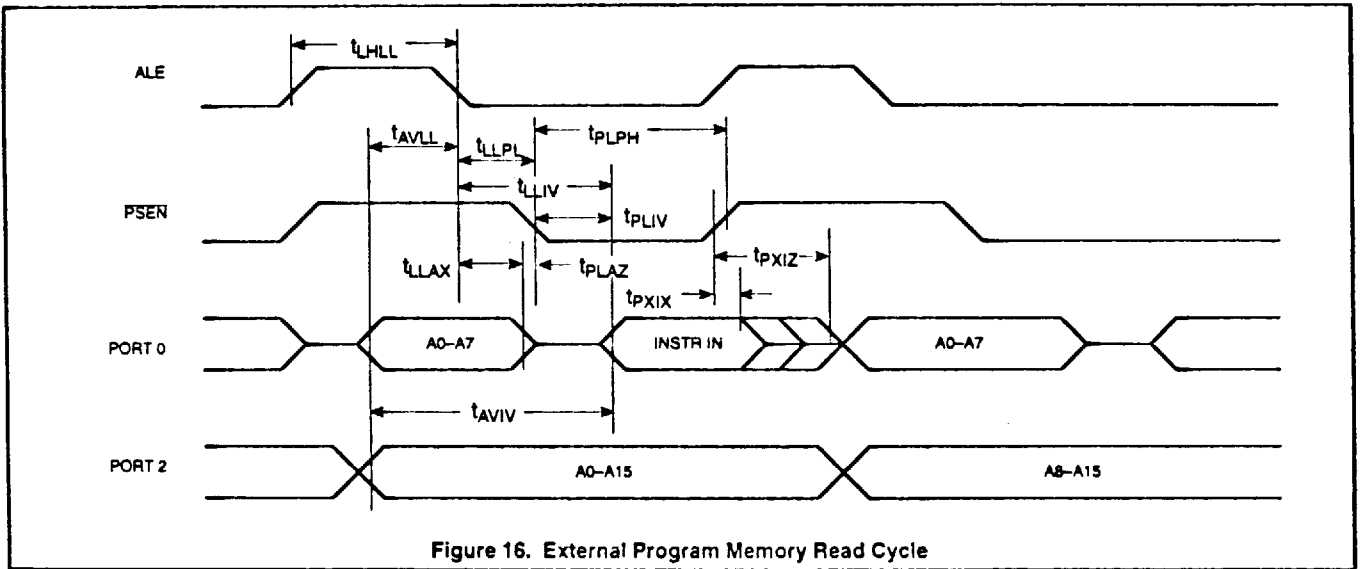


Figure 16. External Program Memory Read Cycle

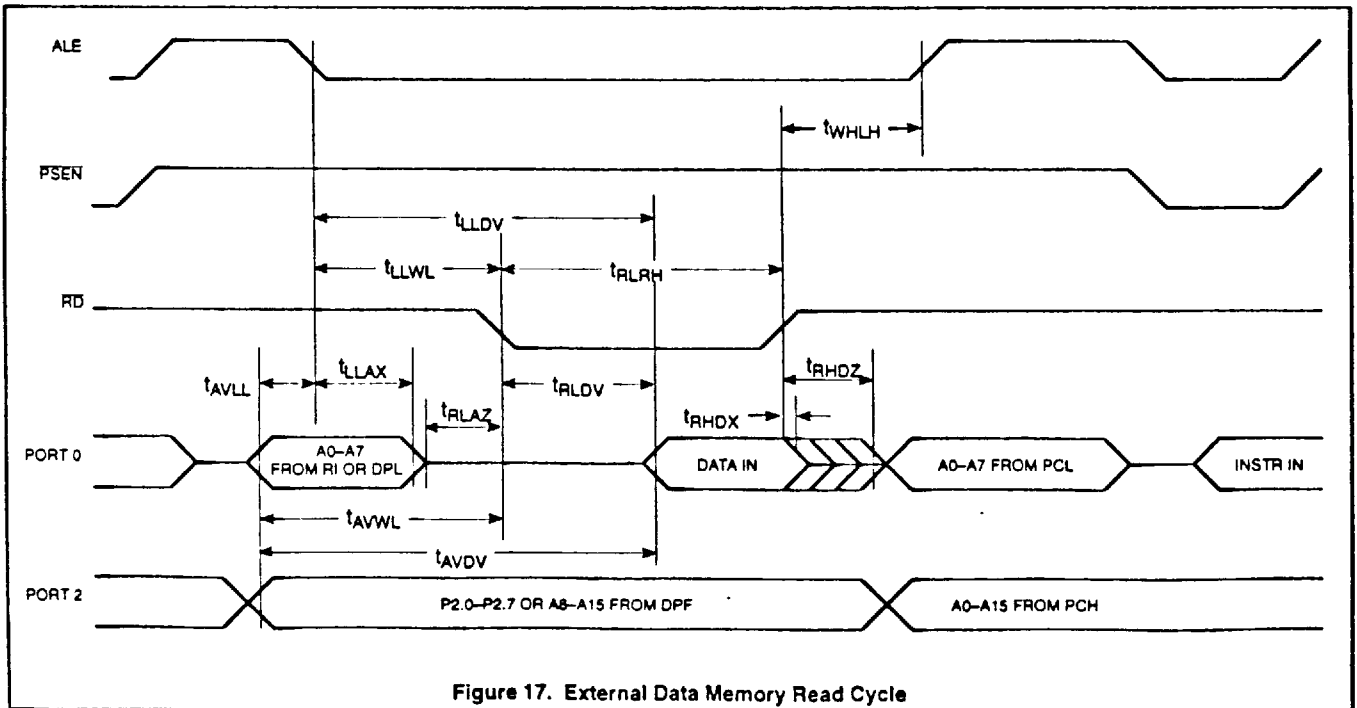
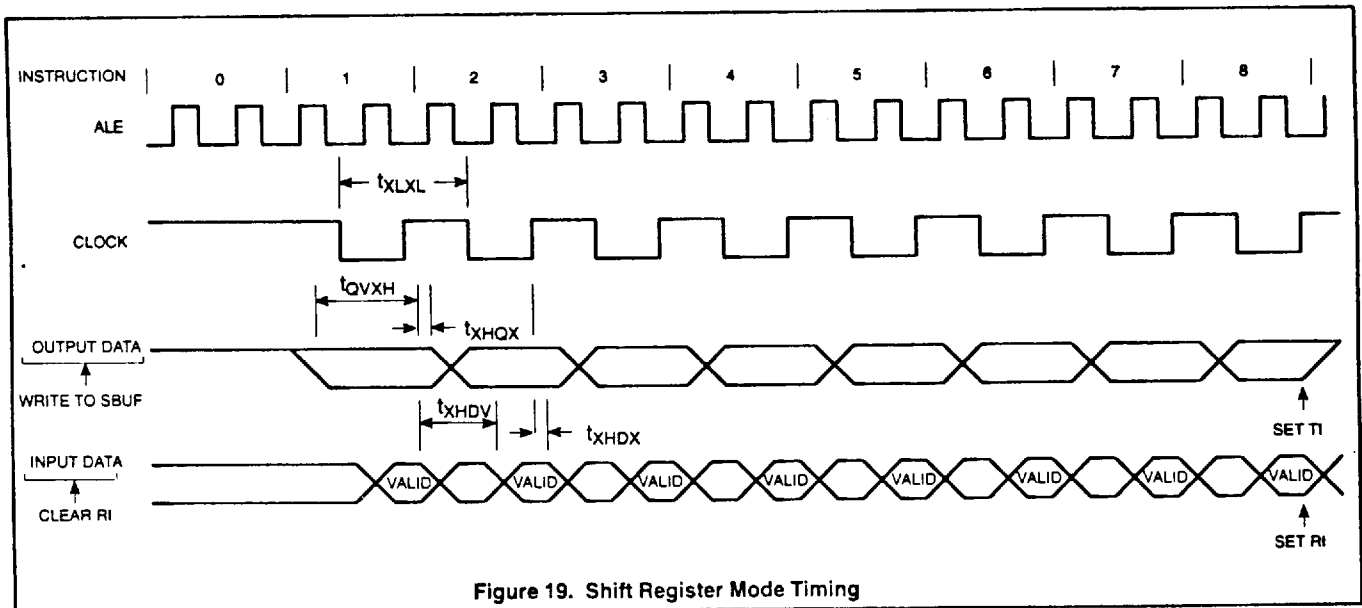
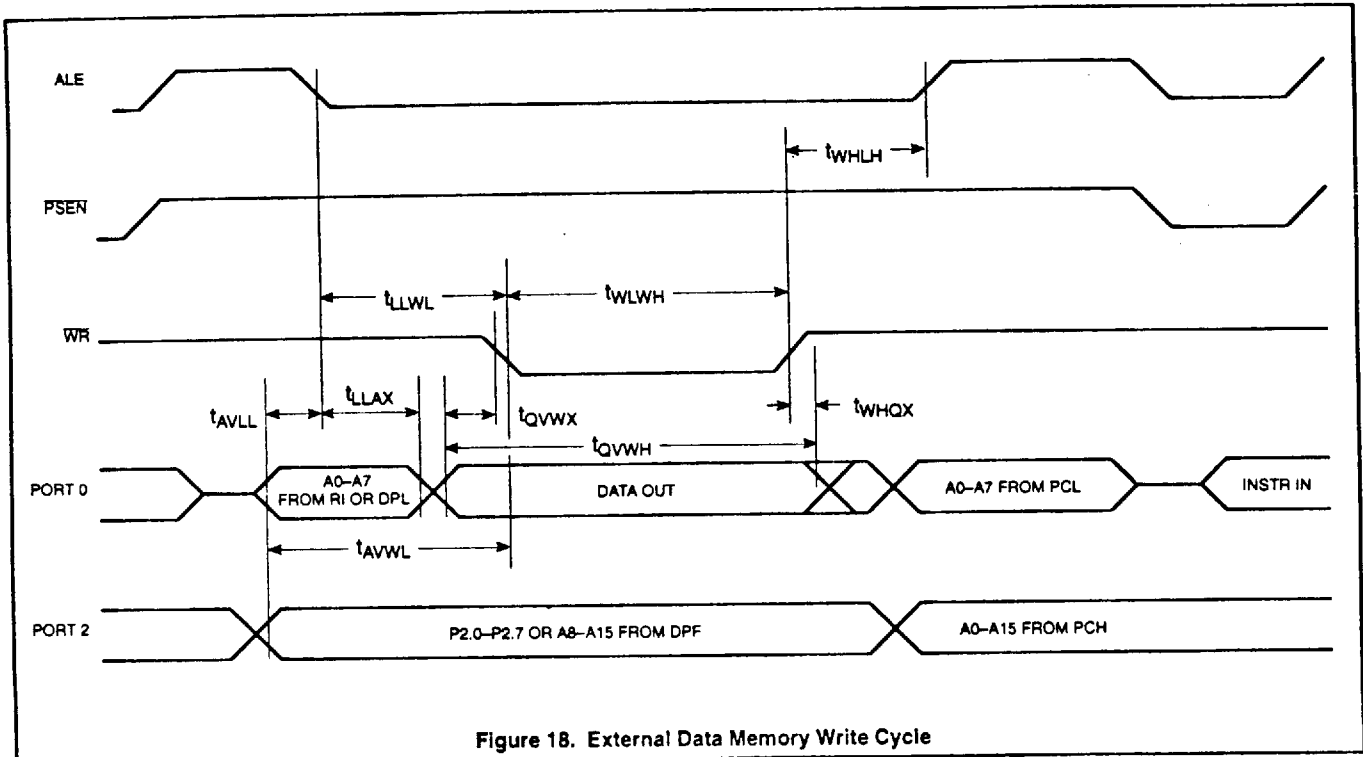


Figure 17. External Data Memory Read Cycle

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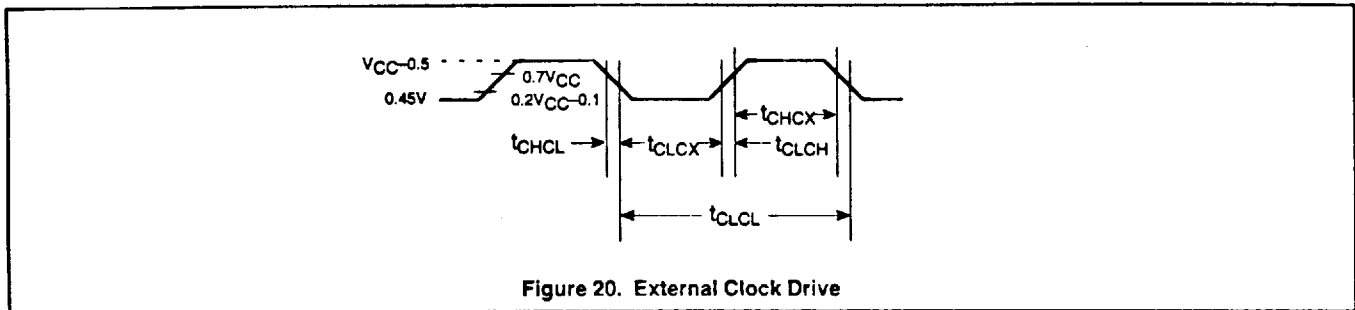


Figure 20. External Clock Drive

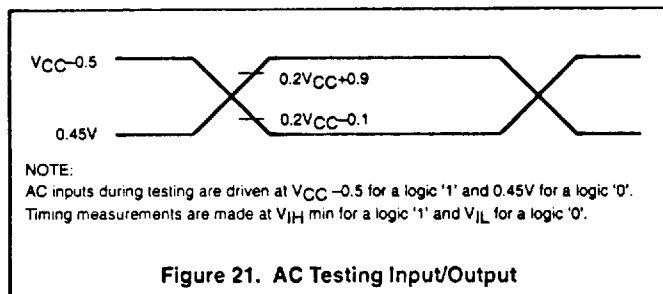


Figure 21. AC Testing Input/Output

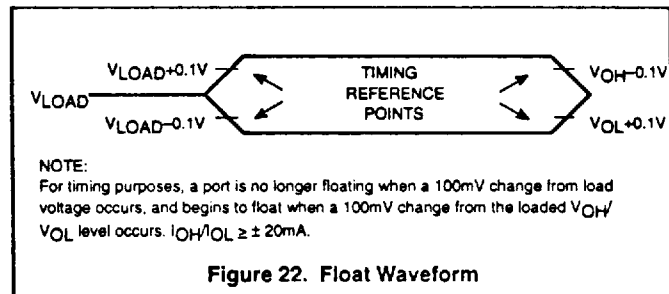


Figure 22. Float Waveform

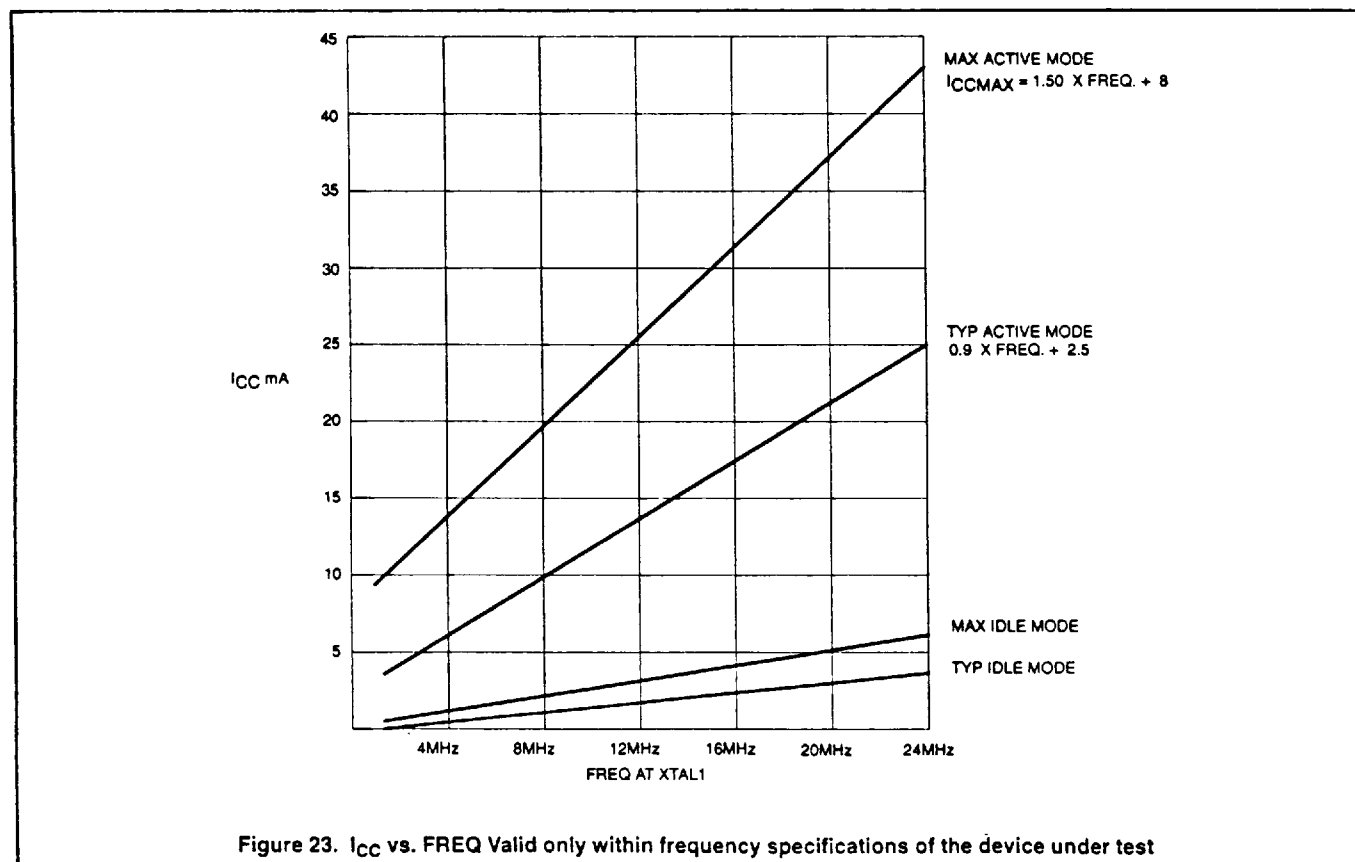
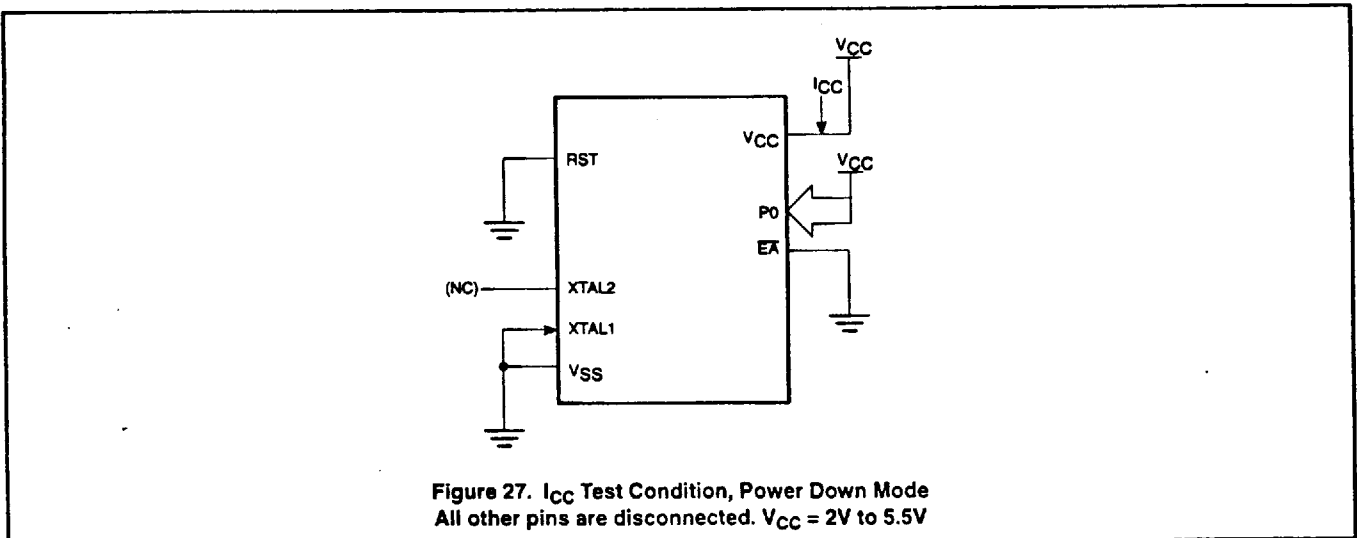
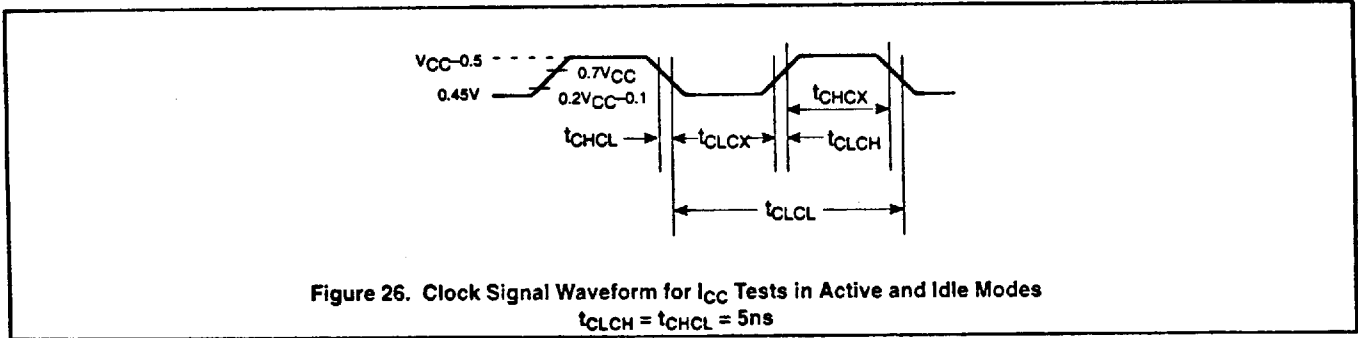
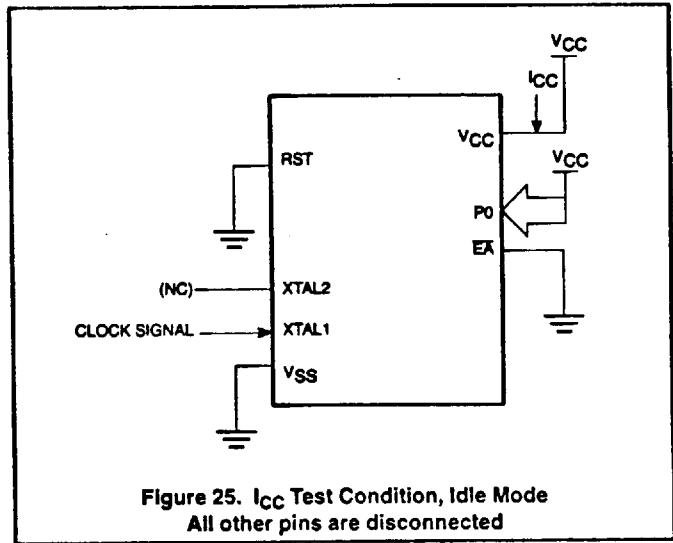
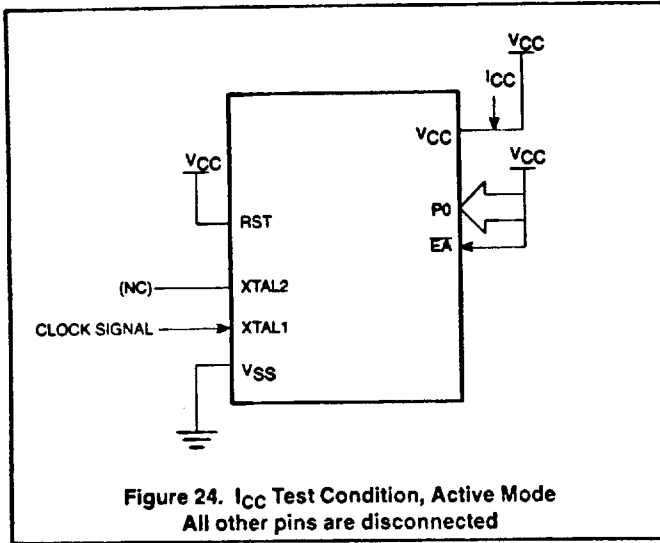


Figure 23.  $I_{CC}$  vs. FREQ Valid only within frequency specifications of the device under test

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## EPROM CHARACTERISTICS

The 87C51FB is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for  $V_{PP}$  (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The 87C51FB contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C51FB manufactured by Philips.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 28 and 29. Figure 30 shows the circuit configuration for normal program memory verification.

## Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 28. Note that the 87C51FB is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 28. The code byte to be programmed into that location is applied to port 0. RST, PSEN and pins of ports 2 and 3 specified in Table 3 are held at the 'Program Code Data' levels indicated in Table 3. The ALE/PROG is pulsed low 25 times as shown in Figure 29.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 25 pulse programming sequence using the 'Pgm Security Bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bit can still be programmed.

Note that the  $\overline{EA}/V_{PP}$  pin must not be allowed to go above the maximum specified  $V_{PP}$  level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The  $V_{PP}$  source should be well regulated and free of glitches and overshoot.

## Program Verification

If security bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 30. The other pins are held at the 'Verify Code Data' levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

## Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips

(031H) = B2H indicates 87C51FB

## Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

## Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. For this and secondary effects, it is recommended that an opaque label be placed over the window. For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345-5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-s/cm<sup>2</sup>. Exposing the EPROM to an ultraviolet lamp of 12,000μW/cm<sup>2</sup> rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Table 3. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	$\overline{EA}/V_{PP}$	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	$V_{PP}$	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	$V_{PP}$	1	0	1	0
Pgm security bit 1	1	0	0*	$V_{PP}$	1	1	1	1
Pgm security bit 2	1	0	0*	$V_{PP}$	1	1	0	0

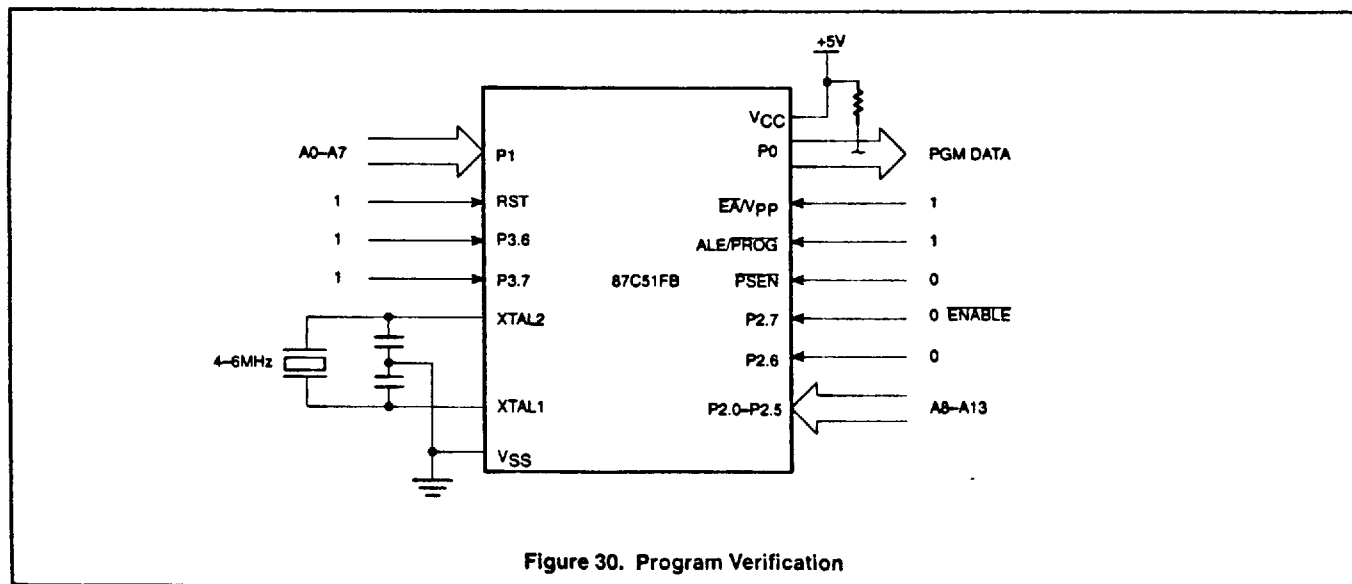
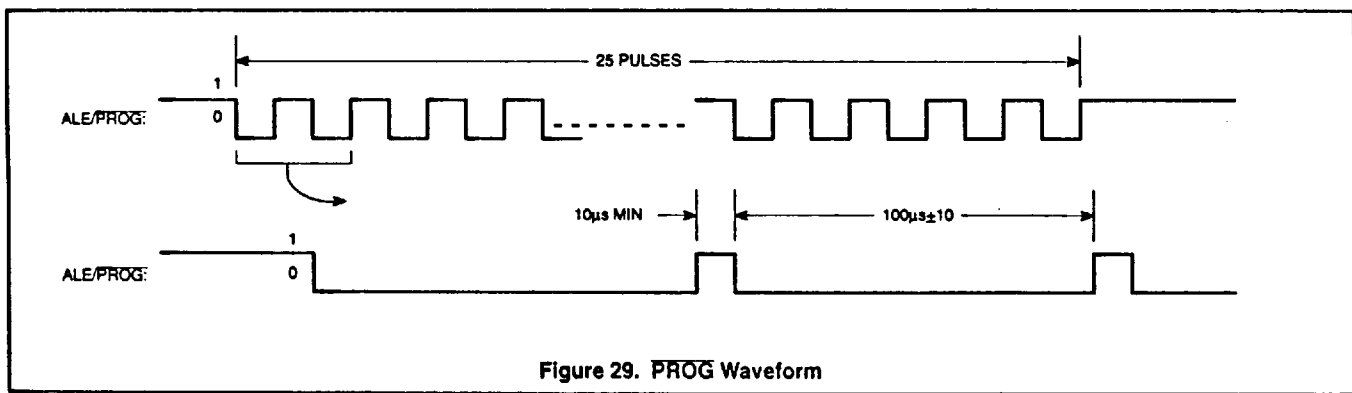
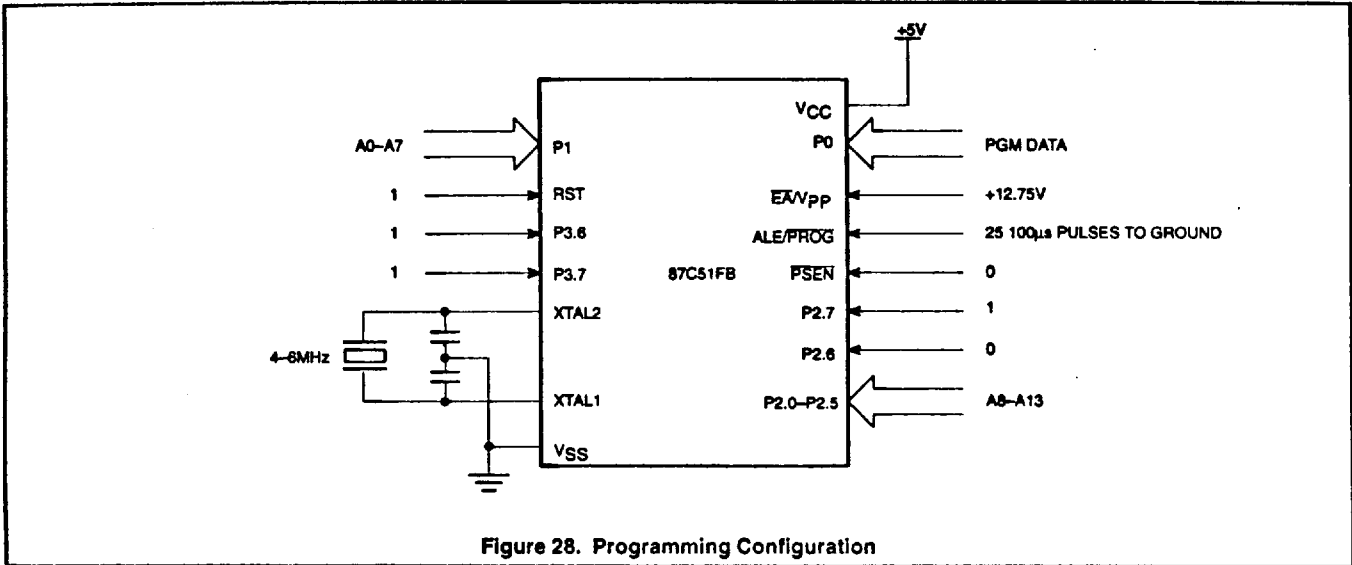
## NOTES:

- '0' = Valid low for that pin, '1' = valid high for that pin.
- $V_{PP} = 12.75V \pm 0.25V$ .
- $V_{CC} = 5V \pm 10\%$  during programming and verification.
- \* ALE/PROG receives 25 programming pulses while  $V_{PP}$  is held at 12.75V. Each programming pulse is low for 100μs (±10μs) and high for a minimum of 10μs.

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## EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

$T_{amb} = 21^{\circ}\text{C}$  to  $+27^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$  (See Figure 31)

SYMBOL	PARAMETER	MIN	MAX	UNIT
$V_{PP}$	Programming supply voltage	12.5	13.0	V
$I_{PP}$	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
$t_{AVGL}$	Address setup to PROG low	$48t_{CLCL}$		
$t_{GHAX}$	Address hold after PROG	$48t_{CLCL}$		
$t_{DVGL}$	Data setup to PROG low	$48t_{CLCL}$		
$t_{GHDX}$	Data hold after PROG	$48t_{CLCL}$		
$t_{ESH}$	P2.7 (ENABLE) high to $V_{PP}$	$48t_{CLCL}$		
$t_{SHGL}$	$V_{PP}$ setup to PROG low	10		$\mu\text{s}$
$t_{GHSL}$	$V_{PP}$ hold after PROG	10		$\mu\text{s}$
$t_{GLGH}$	PROG width	90	110	$\mu\text{s}$
$t_{AVQV}$	Address to data valid		$48t_{CLCL}$	
$t_{ELQZ}$	ENABLE low to data valid		$48t_{CLCL}$	
$t_{EHQZ}$	Data float after ENABLE	0	$48t_{CLCL}$	
$t_{GHGL}$	PROG high to PROG low	10		$\mu\text{s}$

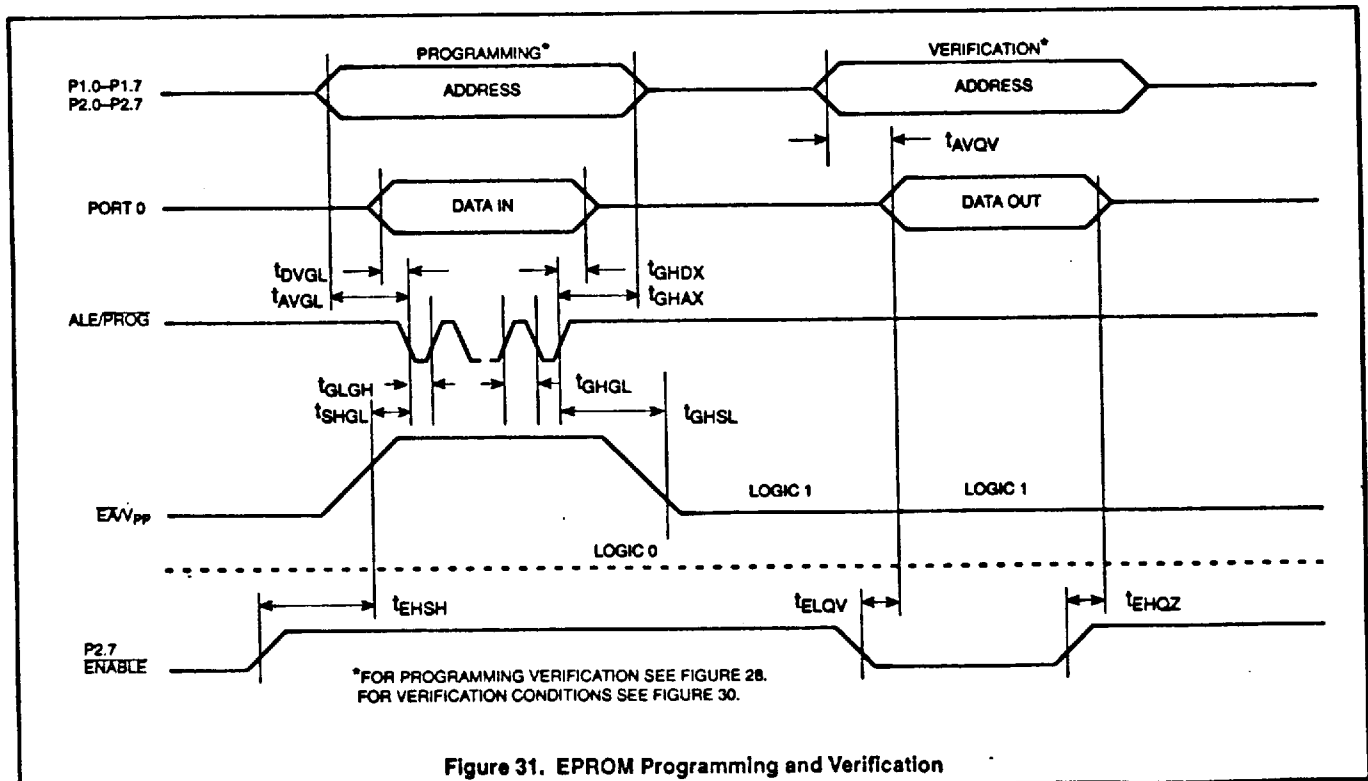


Figure 31. EPROM Programming and Verification