

## 32K x 8 High Speed SRAM

Preliminary, 3/96

### Features

- Fast Access Time: 10ns/12ns/15ns
- 32K x 8 Organization
- Single +5V  $\pm$  10% Power Supply
- Advanced CMOS Process
- Low Power Consumption
- Fully Static Operation
- TTL Compatible I/O
- Common I/O for Low Pin Count
- JEDEC Standard Pinouts
- Three Package Types
  - $\text{D}$  28-pin 300-mil plastic SOJ
  - $\text{D}$  28-pin 300-mil plastic DIP
  - $\text{D}$  28-pin 8 x 13.4mm plastic TSOP 1 (Forward Type)

### Ordering Information

Part Number	Speed	Package
Em51256C-10J	10ns	SOJ
Em51256C-10P	10ns	DIP
Em51256C-12J	12ns	SOJ
Em51256C-12P	12ns	DIP
Em51256C-15J	15ns	SOJ
Em51256C-15P	15ns	DIP
Em51256C-15TS	15ns	TSOP 1

### Key Specifications

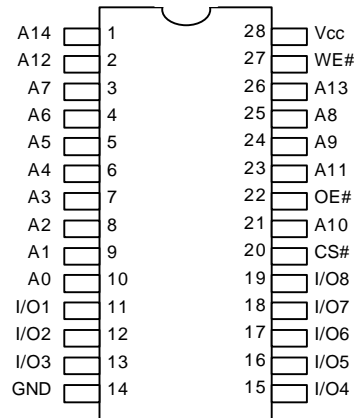
Speed	t <sub>RC</sub>	t <sub>AA</sub>	t <sub>OE</sub>	Active	Stand By
- 10	10ns	10ns	5ns	195mA	20mA
- 12	12ns	12ns	7ns	195mA	20mA
- 15	15ns	15ns	8ns	150mA	10mA

### Overview

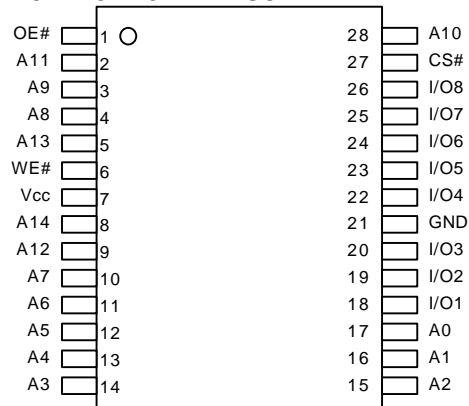
The Em51256C is a high speed SRAM organized in 32,768 words by 8 bits. It is designed with advanced CMOS technology. Each memory cell consists of four transistors and two high valued resistors. It allows lower power consumption and faster access time.

### Pin Assignment

28-Pin 300-mil DIP and SOJ



28-Pin 8 x 13.4mm TSOP 1



### Pin Names

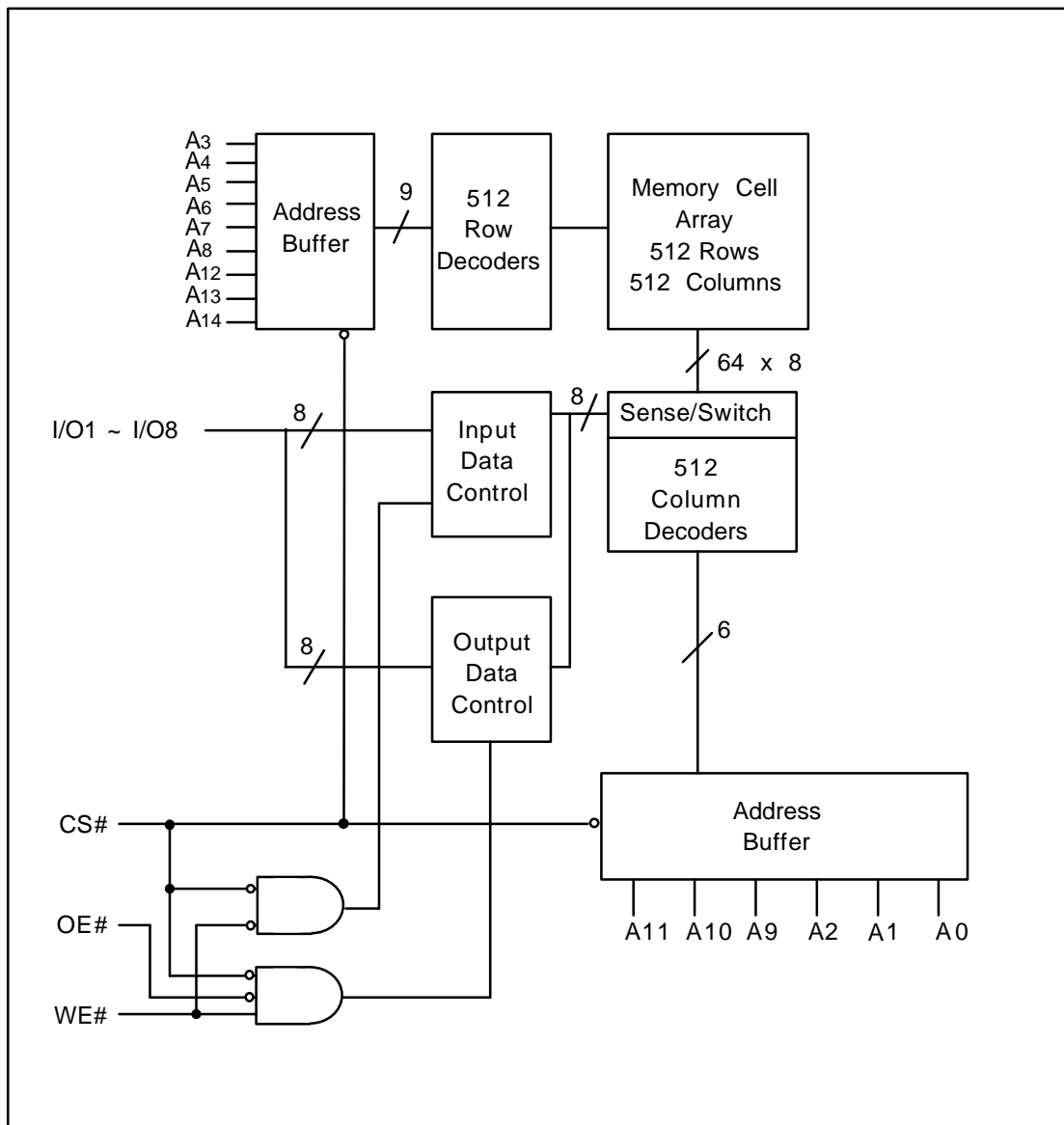
Symbol	Function
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CS#	Chip Select
OE#	Output Enable
WE#	Write Enable
GND	Ground
Vcc	+5V Power Supply

The Em51256C follows JEDEC standard pinouts. It is packaged in three kind of package types, that are 28-pin 300-mil plastic SOJ, 28-pin 300-mil plastic DIP and 28-pin 8 x 13.4mm plastic TSOP 1 (forward type).

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## Block Diagram



## Absolute Maximum Ratings

Supply voltage, $V_{CC}$	-0.5 to +7.0V
Input and output voltages, $V_{IN}$	-0.5 to $V_{CC} + 0.3V$
Operating temperature, $T_{OPR}$	0 to +70°C
Storage temperature, $T_{STG}$	-55 to +125°C
Power dissipation, $P_D$	1.0 W

### Notes:

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The devices should be operated within the limits specified under DC and AC Characteristics.

## Truth Table<sup>1</sup>

CS#	WE#	OE#	Mode	I/O	I <sub>CC</sub>
H	X	X	Not selected	High-Z	Standby
L	H	L	Read	D <sub>OUT</sub>	Active
L	H	H	D <sub>OUT</sub> disabled	High-Z	Active
L	L	X	Write	D <sub>IN</sub>	Active

### Notes:

1. X = don't care

## Capacitance<sup>1</sup>

TA = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C <sub>IN</sub>	i ∅	i ∅	6	pF	V <sub>IN</sub> = 0V
I/O capacitance	C <sub>I/O</sub>	i ∅	i ∅	8	pF	V <sub>I/O</sub> = 0V

### Notes:

1. This parameter is sampled and not 100% tested.

## Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5*	5.0	5.5	V
Input voltage, low	$V_{IL}$	- 0.5	$\bar{i}$ $\bar{D}$	0.8	V
Input voltage, high	$V_{IH}$	2.2	$\bar{i}$ $\bar{D}$	$V_{CC} + 0.3$	V
Ambient temperature	$T_A$	0	$\bar{i}$ $\bar{D}$	70	°C

### Note:

1. For Em51256C-10, supply voltage (min) is 4.75V.

## DC Characteristics

$T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{CC} = +5.0\text{V} \pm 10\%$

Parameter	Symbol	Test Conditions	- 10		- 12		- 15		Unit
			Min	Max	Min	Max	Min	Max	
Input leakage current	$I_{LI}$	$V_{IN} = 0$ to $V_{CC}$ ; $V_{CC} = \text{max}$	- 5	- 5	- 5	- 5	- 5	5	$\mu\text{A}$
Output leakage current	$I_{LO}$	$V_{OUT} = 0$ to $V_{CC}$ ; $OE\#$ or $CS\# = V_{IH}$ ; $V_{CC} = \text{max}$	- 10	- 10	- 10	- 10	- 10	10	$\mu\text{A}$
Operating supply current	$I_{CC}^1$	$CS\# = V_{IL}$ ; $f = \text{MAX}$ $IDOUT = 0$ mA	$\bar{i}$ $\bar{D}$	195	$\bar{i}$ $\bar{D}$	195	$\bar{i}$ $\bar{D}$	150	mA
TTL standby current	$I_{SB}^1$	$CS\# = V_{IH}$ , $f = \text{MAX}$	$\bar{i}$ $\bar{D}$	70	$\bar{i}$ $\bar{D}$	70	$\bar{i}$ $\bar{D}$	50	mA
CMOS standby current	$I_{SB1}^2$	$CS\#; \bar{U} V_{CC} - 0.2\text{V}$ $V_{I/O}, V_{IN}; \bar{O} 0.2\text{V}$ or $\bar{i} \bar{U}$ $V_{CC} - 0.2\text{V}, f = 0$	$\bar{i}$ $\bar{D}$	20	$\bar{i}$ $\bar{D}$	20	$\bar{i}$ $\bar{D}$	10	mA
Output voltage, low	$V_{OL}$	$I_{OL} = 8.0$ mA	$\bar{i}$ $\bar{D}$	0.4	$\bar{i}$ $\bar{D}$	0.4	$\bar{i}$ $\bar{D}$	0.4	V
Output voltage, high	$V_{OH}$	$I_{OH} = - 4.0$ mA	2.4	$\bar{i}$ $\bar{D}$	2.4	$\bar{i}$ $\bar{D}$	2.4	$\bar{i}$ $\bar{D}$	V

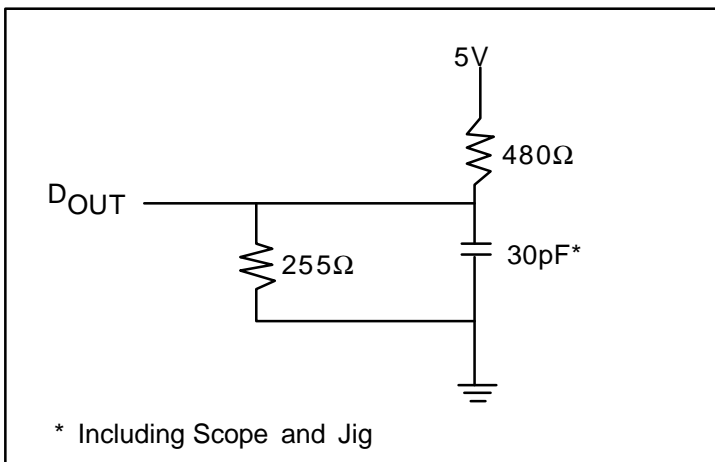
### Notes:

1. At  $f = \text{MAX}$  all I/O pin are cycling at the max frequency of  $1/t_{RC}$ .
2.  $f = 0$  means no I/O lines changes.

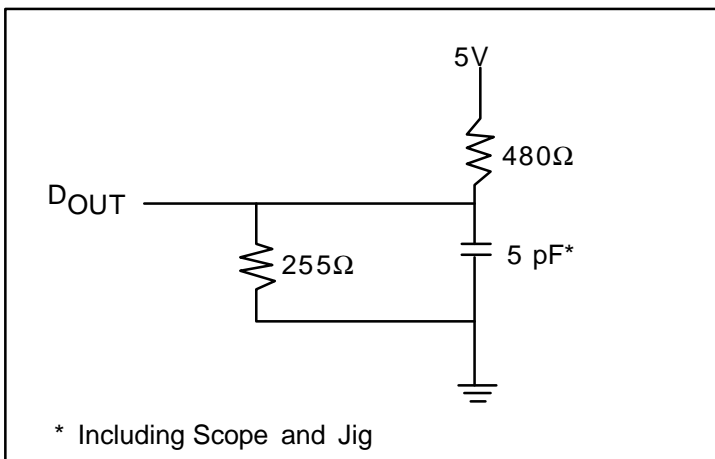
## AC Characteristics

- $T_A = 0$  to  $+70^\circ\text{C}$
- $V_{CC} = 5.5\text{V} \sim 4.5\text{V}$  for Em51256C-12/15  
 $V_{CC} = 5.5\text{V} \sim 4.75\text{V}$  for Em51256C-10
- Input pulse levels:  $V_{SS}$  to  $3.0\text{V}$
- Input rise and fall times:  $3\text{ns}$
- Input and Output timing reference levels:  $1.5\text{V}$
- Output load: See figure 1 and figure 2

**Fig 1. Output Load**



**Fig 2. Output Load for  $t_{CHZ}$ ,  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{OHZ}$ ,  $t_{WZ}$  and  $t_{OW}$**



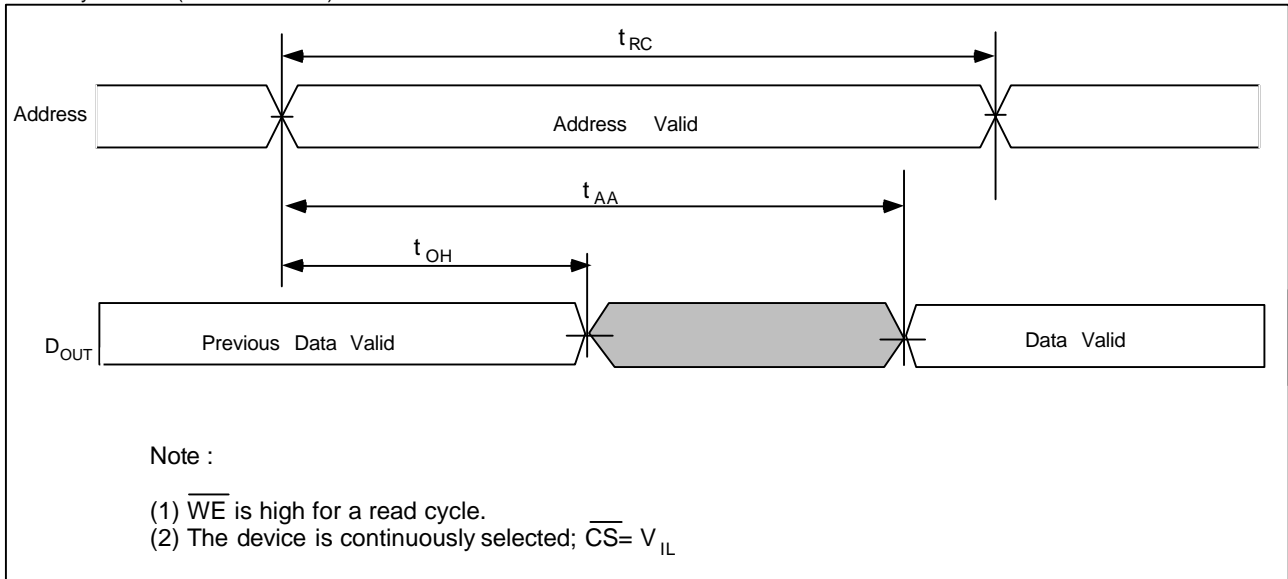
Parameter	Symbol	Em51256C - 10		Em51256C - 12		Em51256C - 15		Unit
		Min	Max	Min	Max	Min	Max	
<b>Read Cycle</b>								
Read cycle time	t <sub>RC</sub>	10	i Ⓟ	12	i Ⓟ	15	i Ⓟ	ns
Address access time	t <sub>AA</sub>	i Ⓟ	10	i Ⓟ	12	i Ⓟ	15	ns
Chip select access time	t <sub>ACS</sub>	i Ⓟ	10	i Ⓟ	12	i Ⓟ	15	ns
Output hold from address change	t <sub>OH</sub>	3	i Ⓟ	5	i Ⓟ	5	i Ⓟ	ns
Chip selection to output in low-Z <sup>1</sup>	t <sub>CLZ</sub>	3	i Ⓟ	3	i Ⓟ	3	i Ⓟ	ns
Chip deselection to output in high-Z <sup>1</sup>	t <sub>CHZ</sub>	0	5	0	5	0	7	ns
Output enable access time	t <sub>OE</sub>	i Ⓟ	5	i Ⓟ	7	i Ⓟ	8	ns
Output disable to output in low-Z <sup>1</sup>	t <sub>OLZ</sub>	0	i Ⓟ	0	i Ⓟ	0	i Ⓟ	ns
Output disable to output in high-Z <sup>1</sup>	t <sub>OHZ</sub>	i Ⓟ	5	i Ⓟ	5	i Ⓟ	7	ns
Chip selection to power-up time	t <sub>PU</sub>	0	i Ⓟ	0	i Ⓟ	0	i Ⓟ	ns
Chip deselection to power-down time	t <sub>PD</sub>	i Ⓟ	10	i Ⓟ	12	i Ⓟ	15	ns
<b>Write Cycle</b>								
Write cycle time	t <sub>WC</sub>	10	i Ⓟ	12	i Ⓟ	15	i Ⓟ	ns
Chip select to end of write	t <sub>CW</sub>	10	i Ⓟ	9	i Ⓟ	10	i Ⓟ	ns
Address valid to end of write	t <sub>AW</sub>	10	i Ⓟ	11	i Ⓟ	13	i Ⓟ	ns
Address setup time	t <sub>AS</sub>	0	i Ⓟ	0	i Ⓟ	0	i Ⓟ	ns
Write pulse width	t <sub>WP</sub>	10	i Ⓟ	8	i Ⓟ	10	i Ⓟ	ns
Write recovery time	t <sub>WR</sub>	0	i Ⓟ	0	i Ⓟ	0	i Ⓟ	ns
Data valid to end of write	t <sub>DW</sub>	7	i Ⓟ	6	i Ⓟ	8	i Ⓟ	ns
Data hold time	t <sub>DH</sub>	0	i Ⓟ	0	i Ⓟ	0	i Ⓟ	ns
Write enable to output in high-Z <sup>1</sup>	t <sub>WZ</sub>	0	3	0	5	0	7	ns
Output active from end of write <sup>1</sup>	t <sub>OW</sub>	3	i Ⓟ	3	i Ⓟ	3	i Ⓟ	ns

**Notes:**

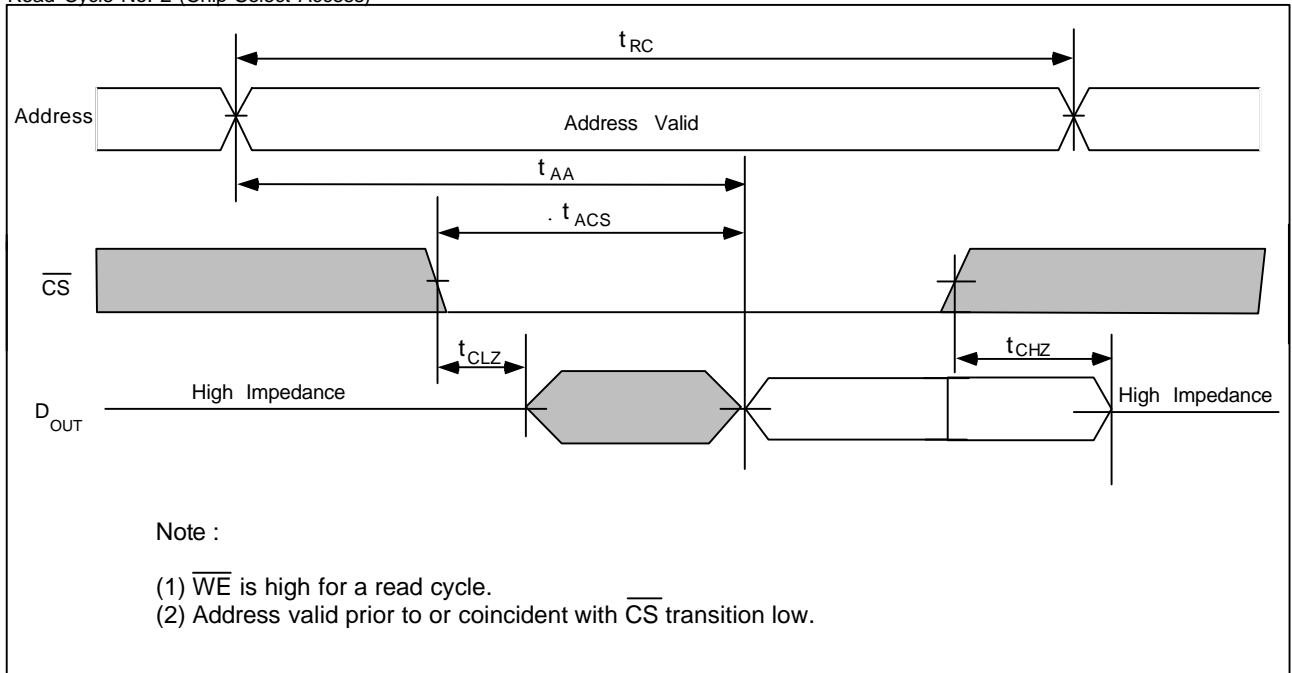
1. Transition is measured at +/-200 mV from steady-state voltage with the loading shown is Fig.2. These AC parameters are sampled but not 100% tested.

## Timing Waveforms

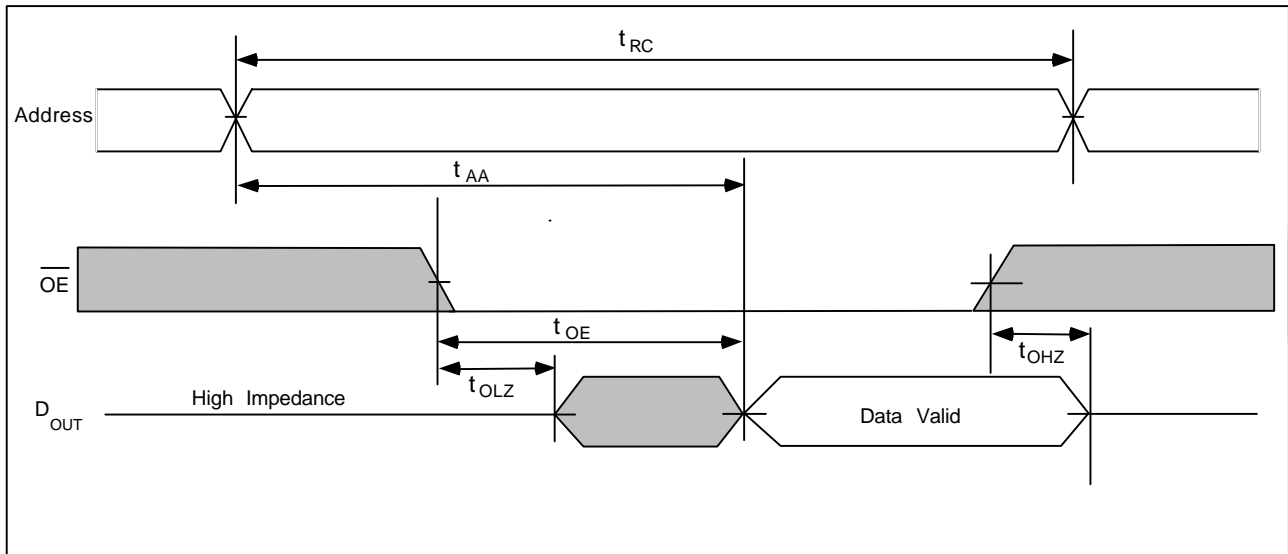
Read Cycle No. 1 (Address Access)



Read Cycle No. 2 (Chip Select Access)

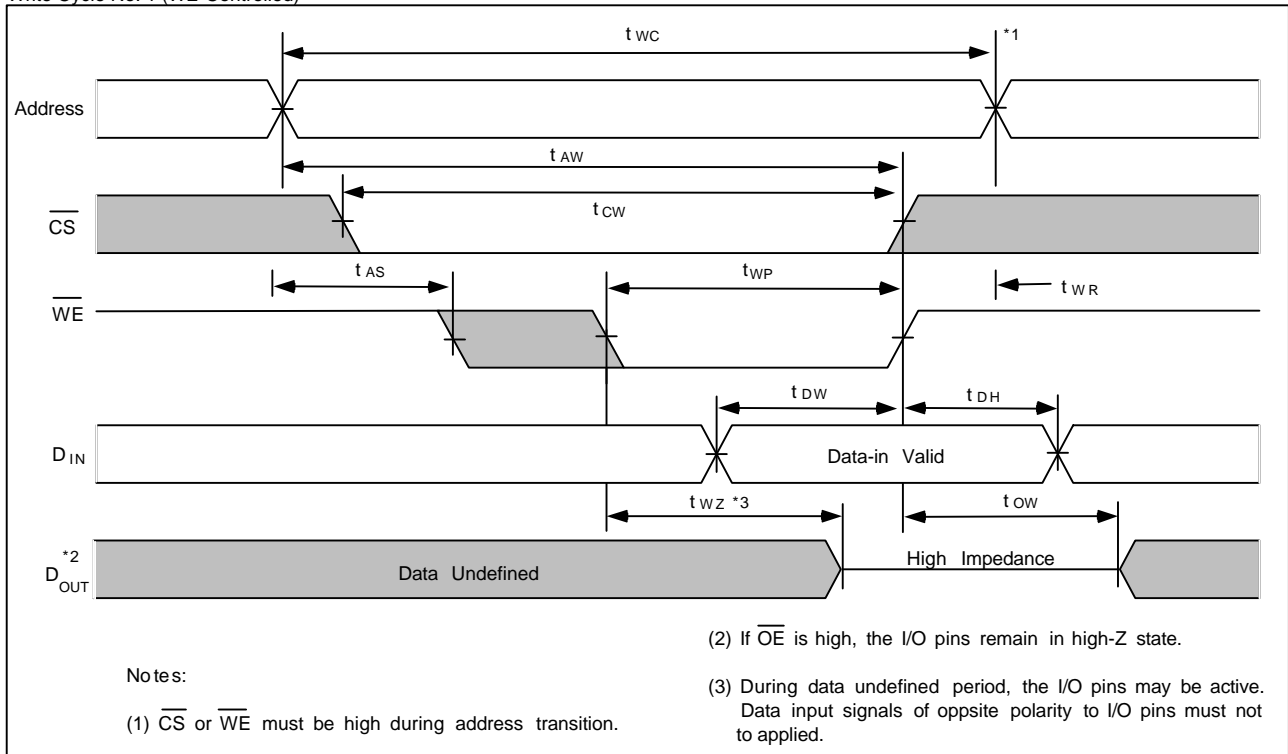


Read Cycle No. 3 ( $\overline{\text{OE}}$  Access)

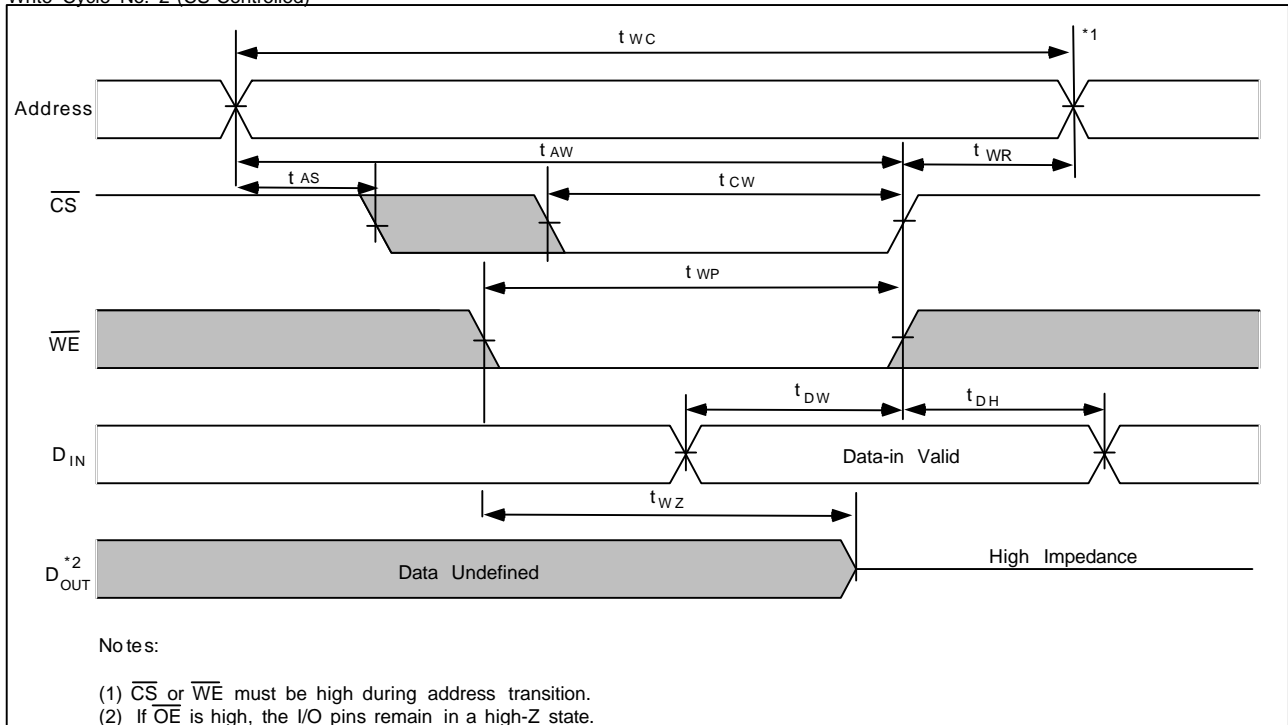


### Timing Waveforms (Cont.)

Write Cycle No. 1 ( $\overline{WE}$ -Controlled)

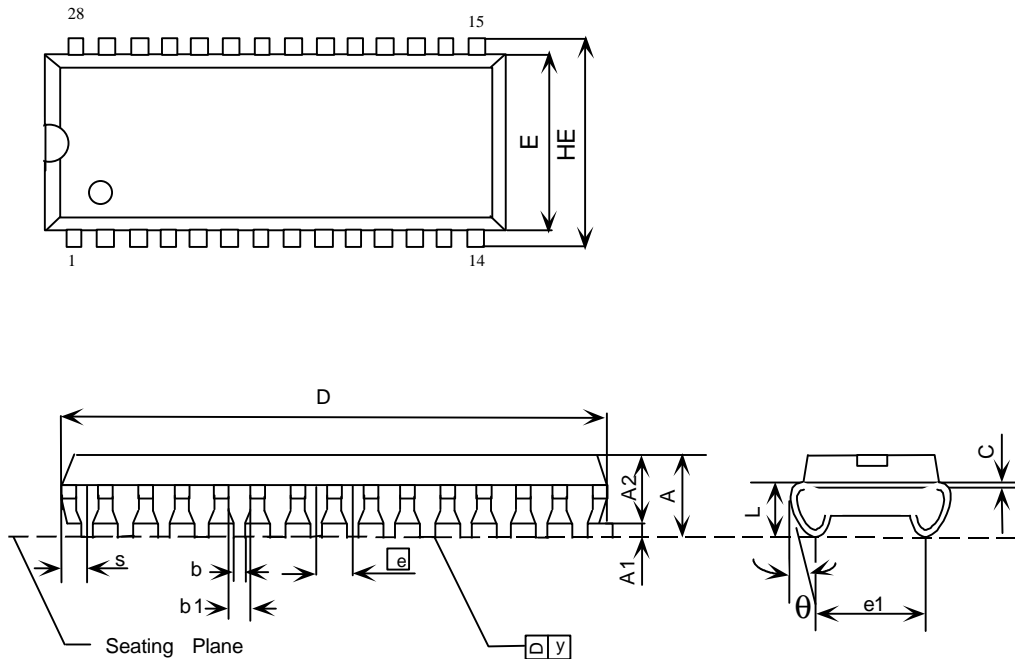


Write Cycle No. 2 ( $\overline{CS}$ -Controlled)



## Outline Drawing

28-pin 300-mil SOJ



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	-----	-----	0.140	-----	-----	3.56
A1	0.027	-----	-----	0.69	-----	-----
A2	0.095	0.100	0.105	2.41	2.54	2.67
b1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	-----	0.710	0.730	-----	18.03	18.54
E	0.295	0.300	0.305	7.49	7.62	7.75
e	0.044	0.050	0.056	1.12	1.27	1.42
e1	0.245	0.265	0.285	6.22	6.73	7.24
HE	0.327	0.337	0.347	8.31	8.56	8.81
L	0.077	0.087	0.097	1.96	2.21	2.46
S	-----	-----	0.045	-----	-----	1.14
Y	-----	-----	0.004	-----	-----	0.10
θ	0°	-----	10°	0°	-----	10°

### Note:

1. Dimension D Max & s include mold flash or tie bar burrs.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and are determined at the mold parting line.
4. Controlling dimension : inch
5. General appearance spec. should be based on final visual inspection spec.

## 28-pin 8 x 13.4mm TSOP 1

