Application Report
SPRAB36A–July 2009

ECG Implementation on the TMS320VC5505 DSP Medical Development Kit (MDK)

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ABSTRACT

The medical development kit (MDK) provides a development platform to TI medical customers, third parties, and other developers. This application report focuses on the VC5505 MDK; however, the analog front ends that are included can also be used with other platforms.

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- The MDK must not be used with a defibrillator or other equipment that produces high voltages in excess of the output supply provided by the AC adapter provided with this ECG device.
- This MDK is intended solely for evaluation and development purposes. It is not intended for use and may not be used as all or part of an end equipment product.
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- You are responsible for the safety of you and your employees and contractors when using or handling the MDK. Further, you are responsible for ensuring that any contacts or interfaces between the MDK and any human body are designed to be safe and to avoid the risk of electrical shock. To minimize the risk of electric shock hazard, use only the following power supplies for the EVM module: Medical Development Applications: SL Power AULT Model MW173KB0503F01.

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1 Introduction

A number of emerging medical applications such as electrocardiography (ECG), digital stethoscope, and pulse oximeters require DSP processing performance at very low power. The TMS320VC5505 digital signal processor (DSP) is ideally suited for such applications. The VC5505 is a member of TI's C5000™ fixed-point DSP platform. To enable the development of a broad range of medical applications on the VC5505, Texas Instruments has developed an MDK based on the VC5505 DSP. A typical medical application includes:

- An analog front end, including sensors to pick up signals of interest from the body
- Signal processing algorithms for signal conditioning, performing measurements and running analytics on measurements to determine the health condition
- User control and interaction, including graphical display of the signal processing results and connectivity to enable remote patient monitoring

1.1 Medical Development Kit (MDK) Overview

The MDK is designed to support complete medical applications development. It includes the following elements:

- Analog front-end boards (FE boards) specific to the key target medical applications of the VC5505 (ECG, digital stethoscope, pulse oximeter), highlighting the use of the TI analog components for medical applications
- VC5505 DSP evaluation module (EVM) main board
- Medical applications software including example demonstrations

Figure 1 shows an overview of the MDK hardware, consisting of individual analog front-end boards for ECG, digital stethoscope, pulse oximeter, and the VC5505 DSP EVM. Any of the analog front-end boards can be connected, one of at a time, to the VC5505 EVM using universal connectors on the front-end boards and the EVM. The analog front-end boards connect to the appropriate sensors for the ECG, digital stethoscope or the pulse oximeter, and perform analog signal conditioning and analog-to-digital (A/D) conversion of the signals from the sensor. Then, the digital signal is sent to the VC5505 EVM where the VC5505 DSP performs signal processing algorithms for the application. The DSP is also responsible for managing user control and interaction including graphical display of the signal processing results. The signal processing results can also be transferred from the VC5505 EVM to a PC for further display, analysis, and storage using the PC application software that is provided with the MDK.

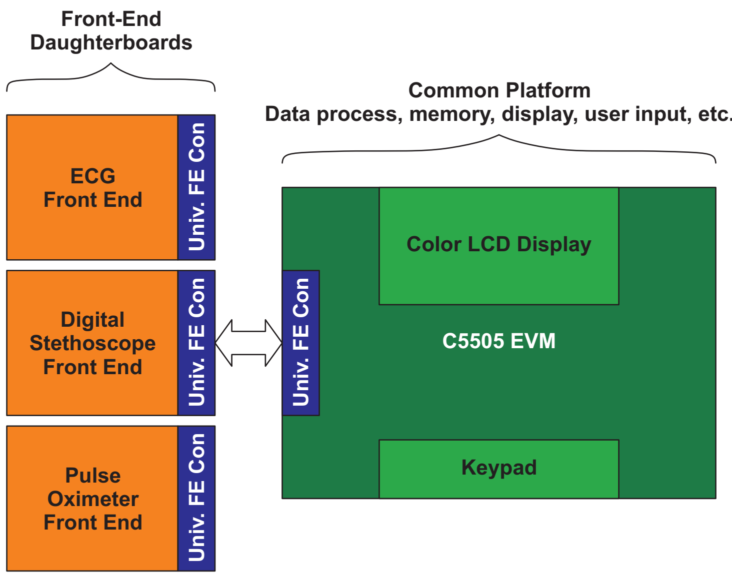


Figure 1. MDK Hardware Overview

1.2 MDK ECG System

An electrocardiogram (ECG/EKG) is the recording of the electrical activities of the heart and is used in the investigation of heart disease. The electrical waves can be measured by selectively placed electrodes (electrical contacts) on the skin.

1.2.1 Key Features

The key features of the MDK ECG system are:

- 12 lead ECG output using 10 electrode input
- Diagnostic quality ECG with bandwidth of 0.05 Hz to 150 Hz
- Heartbeat rate display
- Leads off detection
- Real-time 12 lead ECG waveform display on EVM LCD screen, one lead selectable at a time
- Zoom option for the Y-axis (amplitude) on EVM LCD screen

- Real-time 12 lead ECG waveform display on PC, three leads at a time
- Zoom function on X-axis (time) and Y-axis (amplitude) on PC application
- Freeze screen option on PC Application
- Recording of ECG data and offline view option of recorded ECG data on PC application

1.2.2 MDK Hardware

Several elements of the MDK ECG system are:

- VC5505 EVM
- ECG front-end board
- ECG cable

1.2.2.1 VC5505 EVM

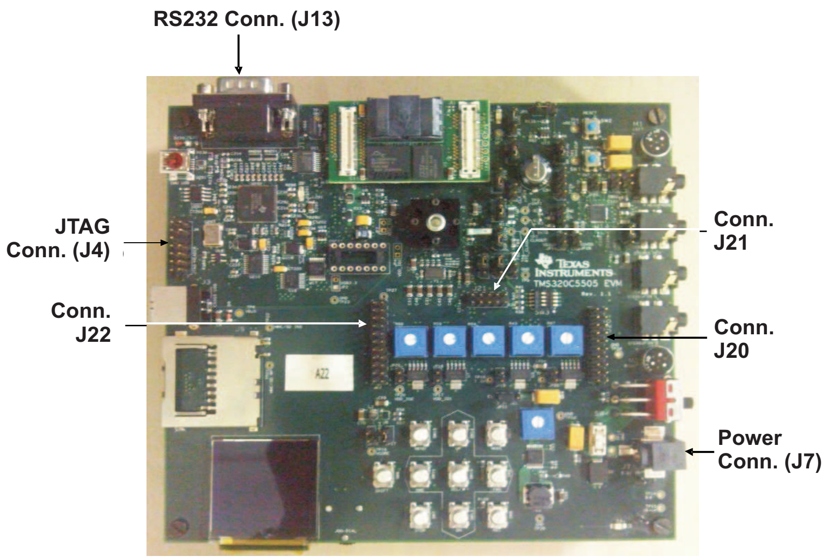


Figure 2. VC5505 EVM

The EVM comes with a full compliment of on-board devices that suit a wide variety of application environments.

For further details on the VC5505 EVM, see the Medical Devlopment Kit provided with your EVM.

Key components and interfaces of the VC5505 EVM used in the MDK ECG system include:

- Texas Instrument's TMS320VC5505 operating at 100 MHz
- User universal serial bus (USB) port via the VC5505
- Inter-integrated circuit (I2C) /serial peripheral interface (SPI) electrically erasable programmable read-only memory (EEPROM)
- External memory interface (EMIF), I2C, universal asynchronous receiver/transmitter (UART), SPI interfaces
- SAR
- External IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) emulation interface
- Embedded JTAG controller
- Color LCD display
- Keys (user switches)

The EVM operates from a + 5 V external power supply or battery and is designed to work with TI’s Code Composer Studio™ integrated development environment (IDE). Code Composer Studio communicates with the EVM board through the external emulator, or on-board emulator.

1.2.2.2 ECG Front-End Board

Figure 3 shows the ECG front-end board. The front end board derives 8 out of 12 ECG leads and provides the digital input to the DSP subsystem. The front-end board can be interfaced with the EVM board through a universal front-end connector. The front-end board is interfaced with and powered by the VC5505 EVM board through the universal front-end connector by using I2C and I2S interfaces.

The 16 channel analog-to-digital converter (ADC) (ADS1258) on the front-end board is configured for 500 Hz sampling with 24-bit data resolution. ADC is interfaced with the VC5505 using the SPI bus.

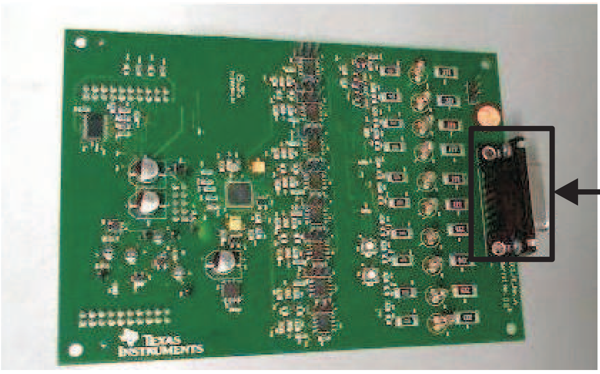


Figure 3. ECG Board

1.2.2.3 ECG Cable

The ECG cable consists of four limb and six chest electrodes. This cable is connected to the front-end board through the DB15 connector. The ECG electrodes pick up ECG signals from the ECG simulator and send them to the ECG front-end board; an off-the-shelf ECG cable is used. For more details regarding ECG cable, see Appendix C.

1.2.3 MDK Software

The software for the MDK application includes:

- VC5505 software application
- PC application

1.2.3.1 VC5505 Software Application

The hardware is initialized by the DSP on the EVM. The DSP reads the digitized signals from the ADC through the SPI interface. The DSP subsystem conditions the ECG signals by removing DC offset and noise using digital filters. Then, the DSP subsystem derives the remaining four ECG electrodes, lead off status, and heart rate. The DSP subsystem also displays one channel ECG wave form, lead off information and heart rate on the LCD screen and sends the the ECG data to the PC application through the UART interface.

1.2.3.2 PC Application

The PC application, which has to be installed on the PC, can be used for viewing the ECG waveform, heart rate, and lead off information. It also provides options to zoom, store and playback the signals transmitted from the EVM. The PC application can operate in two modes: online and offline.

2 Front-End Architecture

The front-end board has a DB15 connector to allow connection for 10 electrode ECG cables; it can be interfaced with the EVM board through the universal front-end connector. The VC5505 EVM board supplies power to the front-end board through the universal front-end connector.

Figure 4 shows the ECG front-end board architecture.

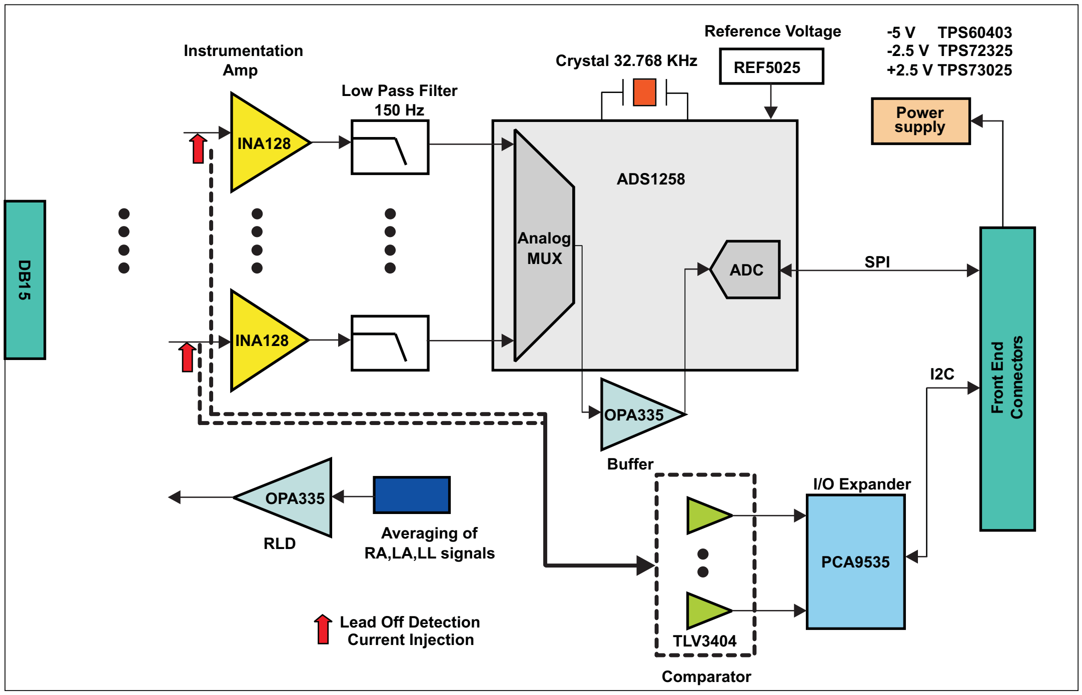


Figure 4. ECG Front-End Block Diagram

The front-end board contains the following stages:

- Right leg driving circuit
- Lead off detection
- Derives eight ECG leads using differential amplifier (instrumentation amplifier)
- Low-pass filtering (anti-aliasing)
- Analog-to-digital conversion (ADC)

2.1 Right Leg Drive Circuit

A right-leg-drive circuit (RLD) is used as an alternative to the grounding of a patient with the MDK ECG system. In the RLD circuit, an electrode attached to the right leg is driven by the output of an auxiliary operational amplifier, where the common-mode voltage is sensed and amplified. The negative feedback of a common-mode signal in this circuit drives the common-mode voltage low. In turn, the body's displacement current flows to the op-amp output circuit, which reduces the pickup of the ECG system and effectively grounds the patient. The averaging is done with the electrode signals RA, LA and LL. OPA335 is used as the inverting amplifier for the RLD circuit. The gain of the RLD circuit design is -39.

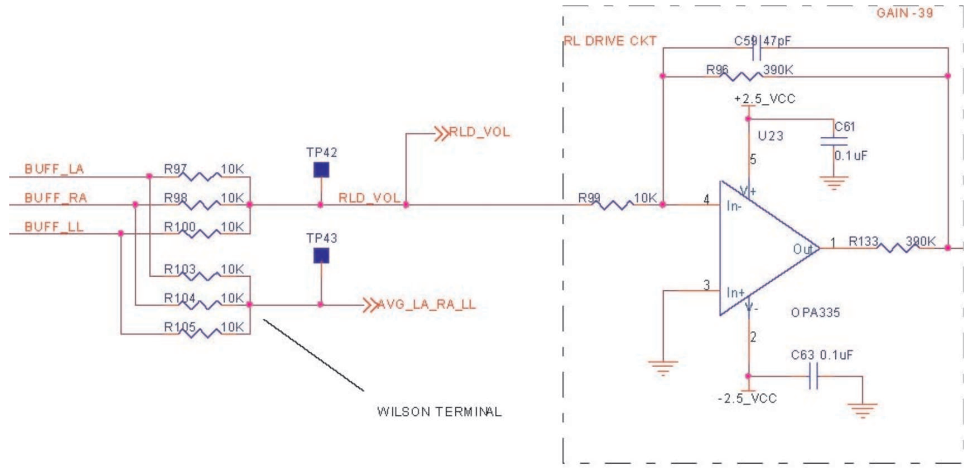


Figure 5. Right-Leg-Drive Circuit

2.2 Lead-Off Detection

The lead-off detection circuit detects the lead status for all the electrodes except RL.The lead-off detection has pull up registers, comparator (TLV3404) and an I2C port expander (PCA9535) as shown in Figure 6.

The ECG electrode leads, except RL, are connected to a pull up resistor (10 M); when any one of the leads is disconnected, the voltage for that lead is pulled up to V_{CC} (+ 2.3 V).

The pull up circuit outputs are connected to the negative and positive terminals of the comparator, and set to 500 mV (threshold voltage). When any lead gets disconnected, the output of the comparator for that lead becomes 0 V. The output of the comparator is connected to the I2C port expander. The port expander generates an interrupt to the DSP whenever there is any change in the input voltage. The interrupt service routine at the DSP reads the output of the port expander using I2C lines and, correspondingly, updates the lead-off status.

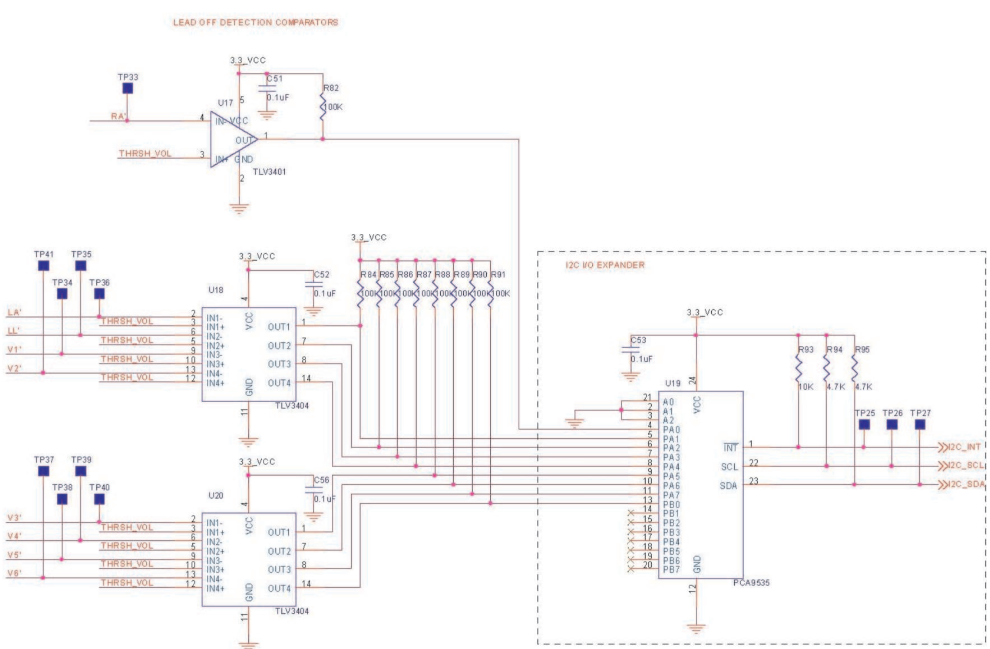


Figure 6. Lead-Off Detection Circuit

2.3 Lead Formation Using Instrumentation Amplifier

The following ECG leads are formed using instrumentation amplifier (INA128) and ECG electrode combinations:

Lead I = LA – RA

Lead II = LL – RA

Lead V1 = V1 - (LA + RA + LL) / 3

Lead V2 = V2 - (LA + RA + LL) / 3

Lead V3 = V3 - (LA + RA + LL) / 3

Lead V4 = V4 - (LA + RA + LL) / 3

Lead V5 = V5 - (LA + RA + LL) / 3

Lead V6 = V6 - (LA + RA + LL) / 3

Where, RA, LL, LA and V1 to V6 are ECG electrodes.

Lead I is formed by connecting LA to the instrumentation amplifier's non-inverting input, while RA is connected to the inverting input. Lead II is formed by connecting LL to the instrumentation amplifier's non-inverting input, while RA is connected to the inverting input.

Uni-polar chest leads (Lead V1 to Lead V6) are formed by applying the corresponding electrodes to the non-inverting input of the instrumentation amplifier, while the inverting input is connected with the average of the RA, LA and LL signals. The average is calculated by addition using three equal value resistors.

Figure 7 shows the lead formation for Lead I.

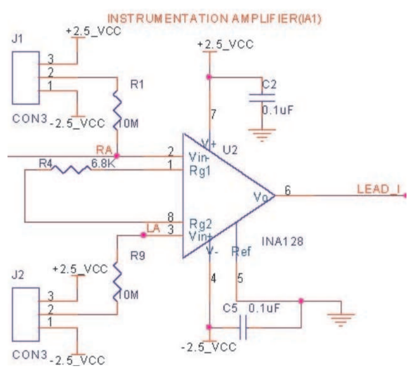


Figure 7. Lead I Formation

The instrumentation amplifier also provides amplification of the weak input signal. The gain of the amplifier is set to 8.35 by using a 6.8K (R4) nominal value precision resistor.

2.4 Low-Pass Filters (Anti-Aliasing)

An active first-order, low-pass filter (LPF) is used for anti-aliasing and for removing frequencies above 150 Hz from each of the ECG leads. The LPF has a cutoff at 150 Hz. The instrumentation amplifier output is fed to the LPF filter input. Figure 8 shows the implementation for the LPF.

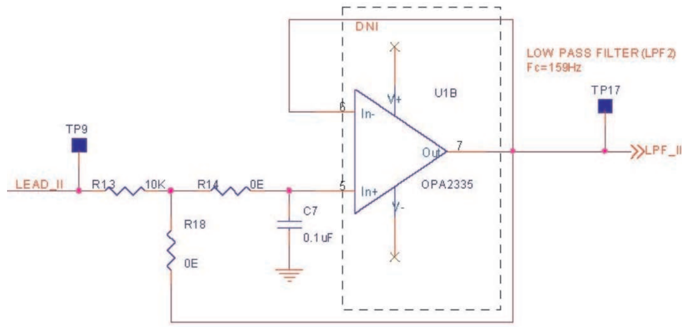


Figure 8. LPF for Lead II

2.5 Analog-to-Digital Conversion (ADC)

Analog signals are converted to digital before sending them to the DSP sub-system. LPF output is connected as input to the ADC (ADS1258).

ADS1258 is a 16-channel, 24-bit delta-sigma ADC. Figure 9 shows the block diagram of ADS1258.

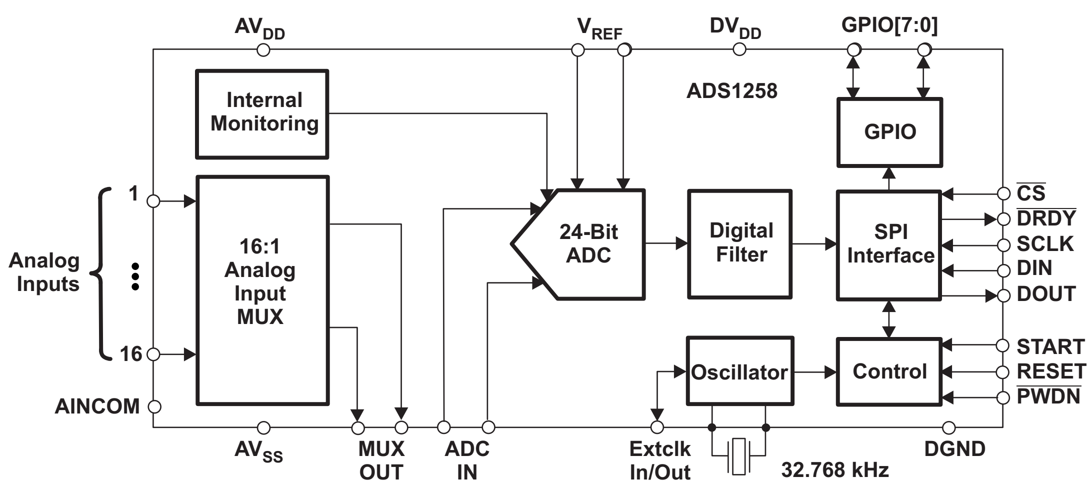


Figure 9. Block Diagram of ADS1258

The following configuration is used for the ADS1258:

Host to ADC interface	SPI
Sampling frequency	500 Hz
Data format	24-bit linear
ADC mode used	Fixed channel mode
Reference voltage	2.5 V

The eight ECG lead outputs from the LPF are connected to eight channels of the ADS1258. Using SPI interface, the ADC is connected to the VC5505 for 500 sps/channels with 24-bit resolution.

The ADS1258 is interfaced to VC5505 DSP as shown in Figure 10.

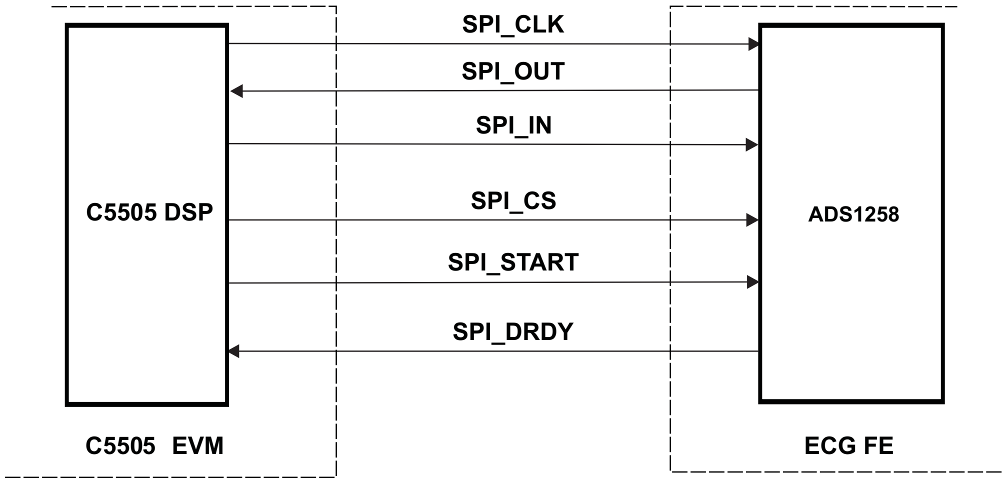


Figure 10. Interface Between ADS1258 and DSP

2.6 Front-End Connector

The front-end board is connected to the EVM through the universal front-end connector, which consists of three connector interfaces with legends on the EVM: J20, J21, and J22.

2.6.1 J20 Connector Interface at VC5505 EVM

The mating for this connector is maintained, but no signals are used by the ECG front-end board.

2.6.2 J21 Connector Interface at VC5505 EVM

This connector carries the 5 V, 3.3 V and 1.8 V from the VC5505 EVM. These voltages act as the primary source for the ECG front-end board.

2.6.3 J22 Connector Interface at VC5505 EVM

This connector carries GPIOs, I2C, SPI and interrupt (INT1) connections from the VC5505 EVM to the front-end board. Pin mapping for the used interfaces are shown in Table 1.

Table 1. J22 Connector Interface

Connector Pin Number	Signal Assigned
1	SPI_START
3	SPI_CLK
7	SPI_CS
11	SPI_IN
12	SPI_DRDY
13	SPI_OUT
15	I2C_INT
16	I2C_SCL
20	I2C_SDA

3 DSP Subsystem

The DSP software, running on the VC5505 EVM, takes the digitized signal from the front-end board and processes it the same. The DSP receives eight ECG lead data from the ADC through the SPI interface. Then, filters are applied to remove DC signal, 50/60 Hz power line noise, and unwanted signals. The filtered signal is used to detect the heart rate and to obtain four ECG leads: Lead III, aVR, aVL and aVF.

The software is designed to handle the following activities:

- Data acquisition through ADC
- Lead-off detection
- DC signal removal
- Multi band-pass filtering
- ECG leads formation
- QRS (HR) detection
- Display of ECG data
- UART communication

Figure 11 shows the high-level architecture of DSP subsystem.

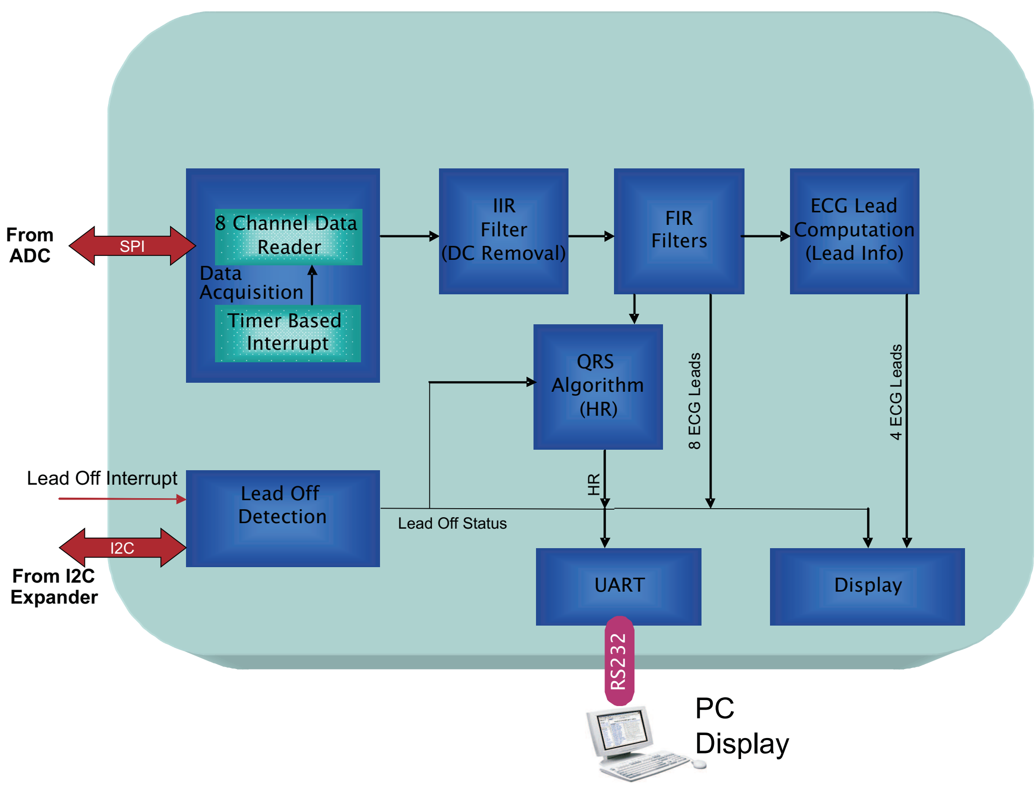


Figure 11. DSP Software Architecture

The various blocks of the DSP subsystem are described in the following sections.

3.1 Data Acquisition

Using the VC5505 timer, an interrupt is generated every 250 µs to sequentially acquire 500 sps of eight ECG leads. The interrupt service routine (ISR) issues a set channel number and (SOC) command to the ADC to acquire 24-bits of ECG data for the selected channel. The acquired data is provided to the infinite impulse response (IIR) filter module after downscaling to 20 bits; the data read for the same channel happens after every 2 ms. The ADC is interfaced with the DSP through the SPI bus.

3.2 Lead-Off Detection

The lead status is read in the IIR for INTR1 of the VC5505 (external interrupt 1). This interrupt is generated in the front ECG board by the I2C port expander as and when the lead status is changed.

3.3 Interrupt Service Routine (IIR) Filter - DC Signal Removal

The DC signals from the eight ECG leads are removed by using the first-order IIR filter. The following transfer function is used for the filter:

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1 - z^{-1}}{1 - \alpha z^{-1}},$$

To provide DC attenuation of 22 dB, the value of alpha is chosen as 0.992. The IIR filter output is downscaled to 16 bits and then provided to the finite impulse response (FIR) filter.

Figure 12 shows the frequency response for the filter.

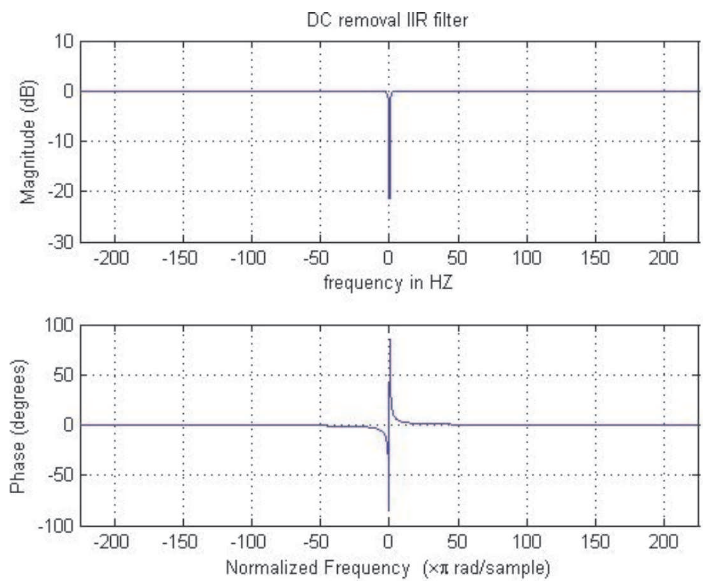


Figure 12. DC Removal Filter Response

Figure 12 shows the pole and zero location for the IIR filter. The pole is located at z = 0.992 and zero at 1 in the Z plane.

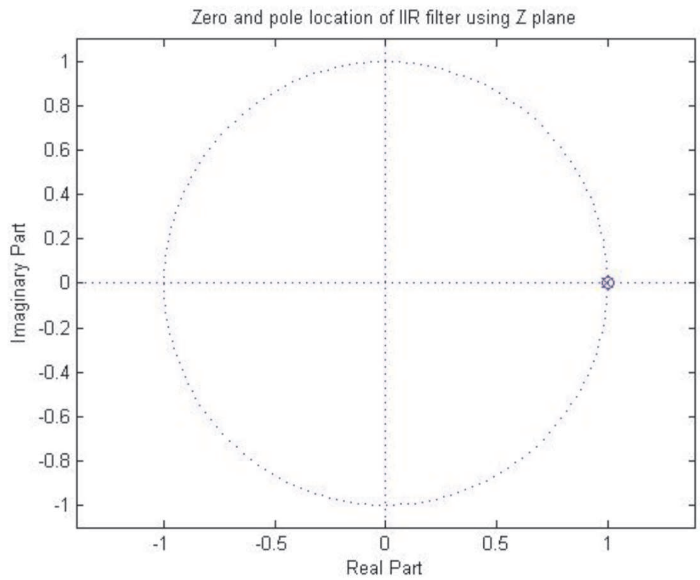


Figure 13. Pole and Zero Location for IIR Filter

Figure 14 shows 1 Hz signal response via the DC removal filter.

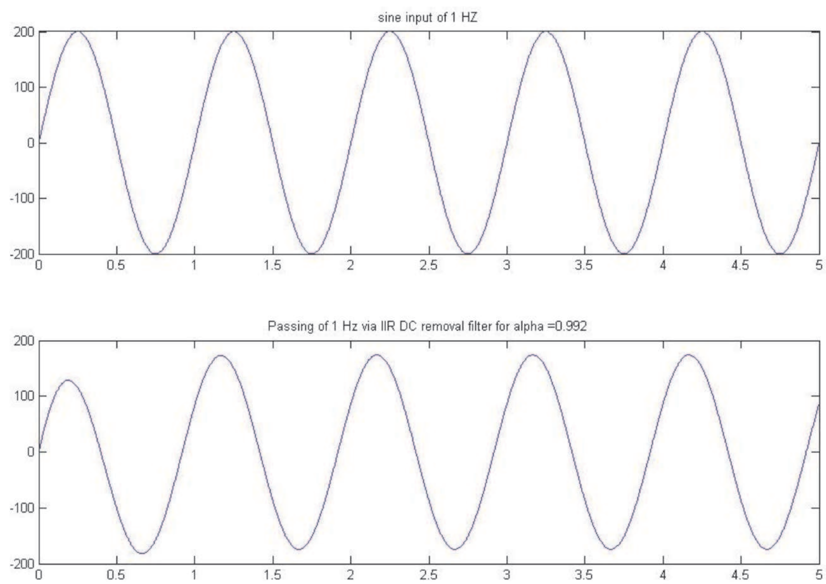


Figure 14. 1Hz Signal Response via DC Removal Filter

3.4 FIR Filter

The multi band-pass filter (MBF) is used for removing unwanted signals and power line noise from the DC removed ECG lead data.

The MBF digital filter being used is the FIR hamming window with the order of 351, which provides cutoff at 150 Hz and notch at 50/60 Hz; the notch frequency is compile-time programmable. This filter also provides a very sharp cutoff at 150 Hz with attenuation of 60 dB at stop-band and notch at 8 dB attenuation. The sampling frequency is 500 samples/second.

Figure 15 shows simulation results for the MBF.

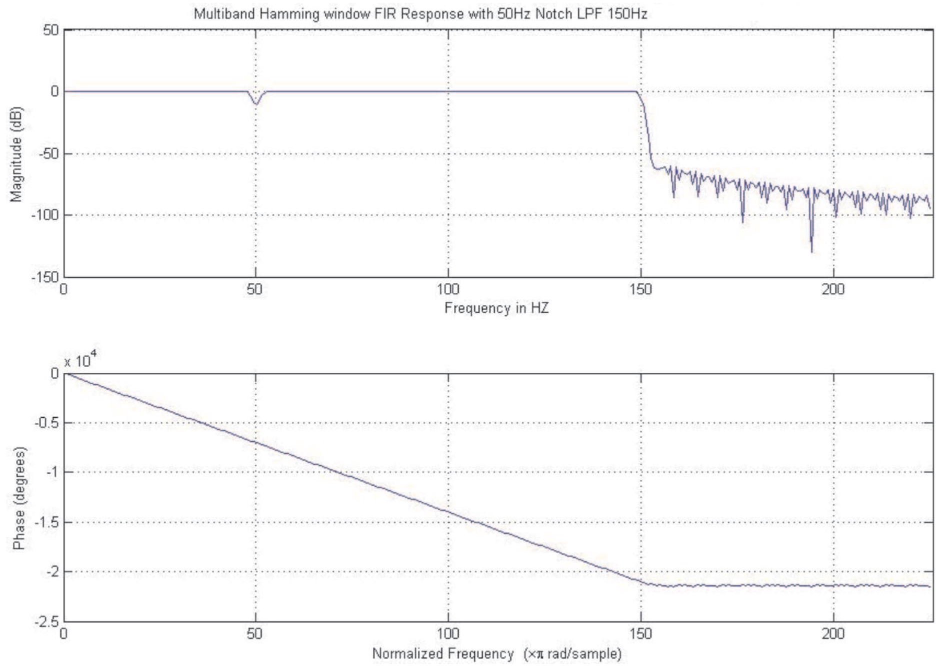


Figure 15. MBF Frequency Response

Buffer-shifting convolution algorithm is used for the realization of the MBF filter. The filter window is shifted for every filtered sample and to insert the new sample into the buffer as depicted in Figure 16.

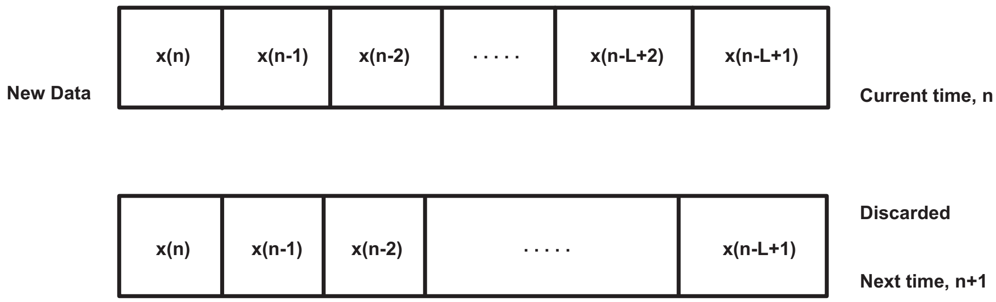


Figure 16. Buffer-Shifting Convolution Algorithm

3.5 ECG Lead Computation

Eight ECG lead data from the MBF filter is fed to the ECG lead formation module. This module computes the remaining four ECG lead data using the following formula:

Lead III = Lead II - Lead I

Lead aVR = - Lead II + 0.5 * Lead III

Lead aVL = Lead I - 0.5 * Lead II

Lead aVF = Lead III + 0.5 * Lead I

3.6 QRS (HR) Detection Algorithm

QRS detection is based on the first derivative of the Lead II ECG signal and threshold. Once five consecutive QRS are detected, the heart rate is calculated by taking the average of the five RR intervals.

The following steps are involved for calculating heart rate:

1. Calculate the first derivative of the Lead II ECG signal samples. The first derivative for any sample is calculated as:

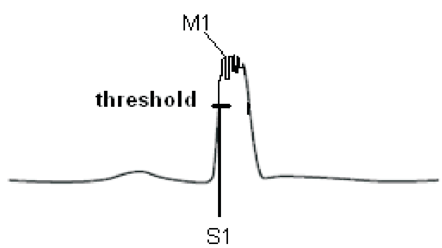
   $y0(n) = |x(n + 1) – x(n - 1)|$

   Where, y0(n) is the first derivative.

   x(n + 1) is the sample value for (n + 1)th sample

   x(n – 1) is the sample value for (n – 1)th sample

   The initial 2sec of the first derivatives in a buffer are stored and the maximum value (P) in this buffer are obtained.
2. Calculate the threshold as 0.7 * P.
3. Compare each of the first derivative values calculated with the calculated threshold.
4. Mark the ECG sample index (S1) of that particular sample, whenever a derivative crosses the threshold.
5. Detect the QRS peak by scanning the next 40 derivatives (MAXIMA_SEARCH_WINDOW = 40) and obtaining the maxima (M1). This maxima (M1) value is stored in another buffer.



6. Skip the next 50 samples (SKIP_WINDOW = 50) to take care of the minimum RR interval that can occur in case of maximum detectable heart rate (i.e., 240 BPM), after detecting a QRS peak.
7. Detect the next five QRS peaks by repeating steps 3 to 6.
8. Calculate the RR interval as the number of samples between two consecutive QRS peaks.
9. Calculate heart rate using the following formula:

   HR per Minute = (60 * Sampling Rate)/(Average RR interval for five consecutive RR intervals)
10. Recalculate threshold from the QRS peak values detected.

3.7 LCD Display

The LCD display shows the ECG, heart rate, and lead-off status. The display is controlled using the SW7 and SW8 keys on the EVM as mentioned in Section 7.1.1. For each of these keys, an interrupt is generated and communicated to the DSP through the SAR interrupt. The interrupt service routine for the key that is pressed takes care of the corresponding action for the interrupt.

3.8 Universal Asynchronous Receiver/Transmitter (UART)

The data sent to the PC through UART has eight ECG lead data; these signals are sent at 250 sps/lead. The PC application derives the remaining four ECG leads using the Lead I and Lead II data. A synchronization frame (header) of 5 bytes is also sent to the UART interface every 1 s. The packet number, heart rate, and lead status values are sent along with the ECG header. The header is followed by interleaved samples of eight ECG leads. The interval between the two ECG data packets is 500 µs. The packet number gets incremented for every new sample sent.

The UART configuration is set as 115200 bps, 8 bits data, 1 stop bit and no parity.

ECG Header

00	80	00	80	00	Packet Number	Heart Rate	Lead Status (Low)	Lead Status (High)

ECG Data

Current Channel Low 8 Bits	Current Channel High 8 Bits

4 PC Application

The PC application is used for viewing the ECG waveform and ECG values. It also provides options to zoom, store and playback the signals.

The PC application has two modes of operation: online and offline.

- Online mode: the ECG data is plotted in real-time as a scrolling display
- Offline mode: the recorded ECG data is displayed for analysis

Two timers run on the application for online mode: acquisition and display timer.

The acquisition timer is set for 100 ms intervals and reads the data from the serial port. After fetching the data from serial port, it parses the stream of bytes to different variables like packet number, heart rate, lead-off status and to the ECG data object containing the digital value of eight leads ECG samples. The four non-acquired leads, Lead III, aVR, aVL and aVF data, are derived from Lead I and Lead II as follows:

Lead III = Lead II - Lead I

aVR = - Lead II + 0.5 * Lead III

aVL = Lead I - 0.5 * Lead II

aVF = Lead III + 0.5 * Lead I

The ECG data object for each sample is stored in a queue buffer.

The display timer is set to an interval of 60 ms and is used to plot the ECG wave forms, and update the heart rate and lead-off status information on the screen. This timer is elapsed every 60 ms; in each elapsed event 15 samples of the leads are plotted on the screen. Figure 17 shows a sample PC application snapshot.

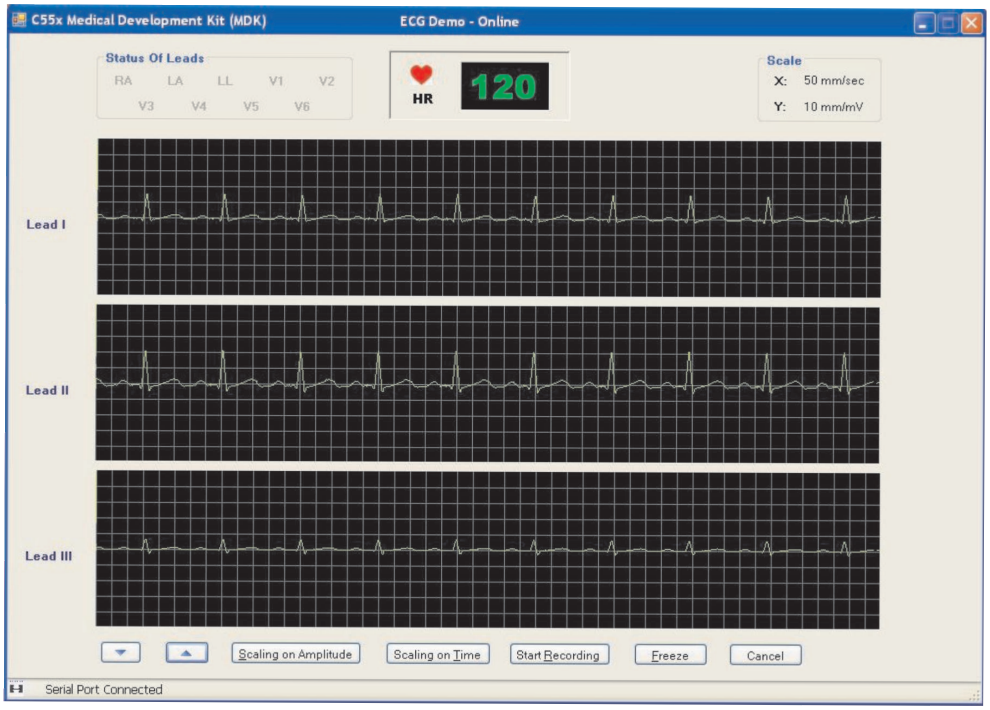


Figure 17. PC Application Snapshot

5 Installation

5.1 Components and Accessories Required

The following components and accessories are required for the MDK ECG installation.

- VC5505 EVM with power supply
- ECG front-end board (ECG FE)
- Code Composer Studio v3.3
- RS232 cable
- USB cable
- 10 lead ECG patient cable
- VC5505 DSP application software
- PC application software

5.2 Hardware Installation

1. Mount the ECG front-end board on top of the VC5505 EVM at connectors J20, J21 and J22. Ensure that there is a firm connection between the front-end board and the EVM. Figure 18 shows the connector positions on the VC5505 EVM.

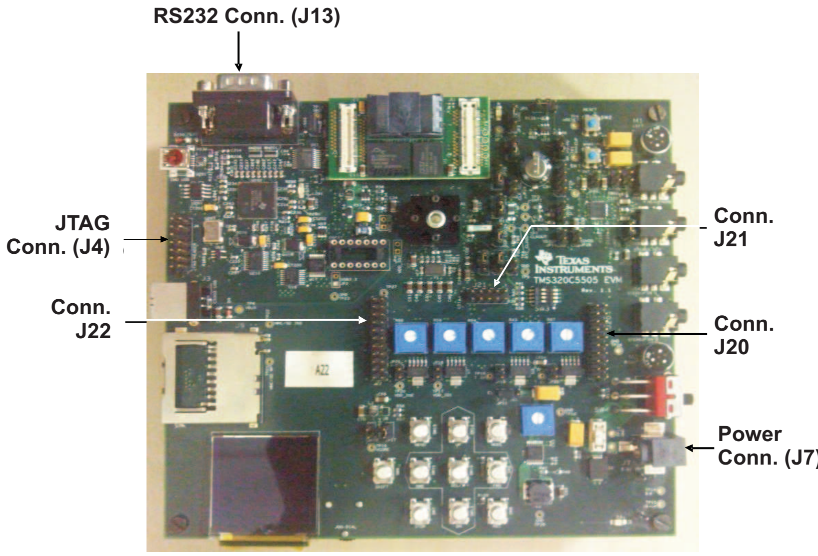


Figure 18. VC5505 EVM Connector Details

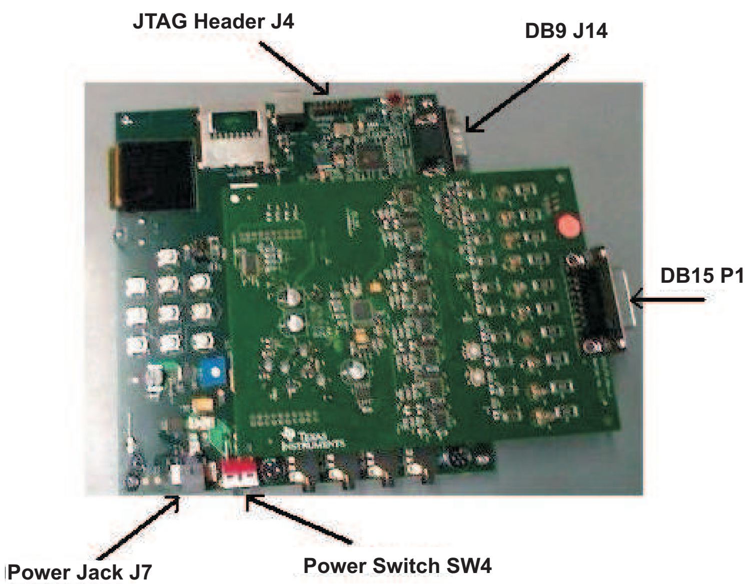


Figure 19. ECG Front-End Mounted on the VC5505 EVM

2. Connect the USB cable between the PC and the VC5505 EVM for the debug mode of operation.
3. Connect the VC5505 emulator JTAG cable to the VC5505 EVM.
4. Connect the serial cable (UART) to the DB9 connector (J13) of the VC5505 EVM and the other end to the serial port of the PC, for viewing the signals on the PC application.
5. Connect the ECG cables to DB15 connector P1.
6. Connect the other end of the ECG cable (there are 10 leads) to an ECG simulator.
7. Power on the system using slide switch SW4 on the VC5505 EVM.

Note: The ECG simulator has 10 connector points that are assigned to different electrodes, i.e., RA, RL, LA, etc. Ensure that the ECG leads are connected to the corresponding connectors on the simulator.

5.3 Software Installation

5.3.1 System Requirements

The following installations are required to run the software provided with the MDK ECG kit.

- Code Composer Studio v3.3
- bios_5_32_01
- Spectrum Digital XDS510 USB driver for Code Composer Studio v_3.3
- .NET 2.0 frame work

Table 2 explains the content of the CD provided with the MDK ECG kit.

Table 2. Release CD Contents

S Number	Directory/Filename	Contains
1	ECGSystem_V_5_0	Project source code
2	Output	Contains three files: ECGSystem.out c5505evm.gel and VC5505 XDS510USB Emulator.ccs
3	PCApplication	Executable for PC application
4	BootImageCreation.zip	Folder that contains the following files: bootImage.exe convertBind0.bat convertEnc0.bat convertInsecure.bat programmer.out readme.txt
5	Document	Contains the following documents: ReleaseNote.txt Quick starter guide V6.0 doc

5.3.2 VC5505 DSP Software (debug mode) Installation Steps

1. Copy the *c5505evm.gel* file from the CD to *<CCS installation dir>/CC/GEL/*.
2. Copy the *ECGSystem* directory from the CD to a local directory on the PC where Code Composer Studio is installed.

5.3.3 VC5505 DSP Software (standalone mode) Installation Steps

1. Copy the *BootImageCreation.zip* file from the CD to a local directory on the PC where Code Composer Studio is installed. This path needs to be used later for Flashing; ensure that there are no spaces in the path name.
2. Copy the *ECGSystem.out* file from the CD to the < BootImageCreation> folder.
3. Execute *convertInsecure.bat* from the <BootImageCreation> folder to create the new *InsecureBootImage.bin* file.
4. Open Code Composer Studio.
5. Power on the VC5505 EVM.
6. Select Debug → Connect in Code Composer Studio to connect to the VC5505 EVM.
7. Load *programmer.out* VC5505 EVM from the < BootImageCreation> folder.
8. Select Debug → Run in Code Composer Studio.

9. Enter *241:<BootImageCreation Folder>\InsecureBootImage.bin* and press OK in the popup window shown in Figure 20.

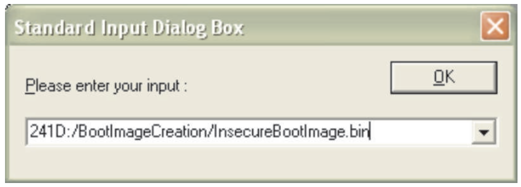


Figure 20. Input Dialog Box

10. Wait until *Programming Complete*.
11. Power off the VC5505 EVM and disconnect.

5.3.4 PC Application Installation Steps

Prior to installing the PC application, ensure that .NET 2.0 framework is installed on the system. .NET 2.0 redistributable framework can be downloaded from the following URL: http://www.microsoft.com/downloads/details.aspx?familyid=0856eacb-4362-4b0d-8edd-aab15c5e04f5&displaylang=en.

1. Open the *PCApplication* folder on the CD and double click on *C55x ECG Medical Development Kit.msi*.
2. Click *Next* on the welcome screen to continue the installation.
3. Browse to the folder where the application is installed. Select the installation mode for Everyone or Self and click *Next*.
4. Click *Next* on the Confirmation screen. This installs the application into the specified folder.
5. Click *Close* to complete and exit the installation.

6 Running the Demo Application

The ECG application can be run in two modes: standalone and debug.

- Standalone mode, for running from Flash memory
- Debug mode, for loading and debugging using Code Composer Studio

6.1 Running in Standalone Mode

1. Complete the installation steps provided in Section 5.3.
2. Power on VC5505 EVM using slide switch SW4.
3. Switch on the ECG simulator to view the ECG signal on the VC5505 EVM.

6.2 Running in Debug Mode

1. Complete the installation steps provided in Section 5.3.
2. Power on the VC5505 EVM using slide switch SW4.
3. Open Code Composer Studio.
4. Click on Debug → Connect in Code Composer Studio to connect to the VC5505 EVM.
5. Click on Project → Open in Code Composer Studio and select the *ECGSystem.pjt* file.
6. Click on File → Load .out file in Code Composer Studio.
7. Execute the application.
8. Switch on the ECG simulator to view the ECG signal on the VC5505 EVM.

6.3 Running the PC Application

6.3.1 Online Mode

The following steps are required to view signals in online mode using the PC application:

1. Connect the RS232 cable between the PC COM port and the VC5505 EVM.
2. Complete the installation steps provided in Section 5.3.
3. Open the PC application.
4. Select online mode and click OK.
5. Select the available COM port and click OK.
6. Signals transmitted from the VC5505 EVM can be viewed on the PC application.

6.3.2 Offline Mode

The following steps are required to view signals in offline mode stored on the PC using the PC application:

1. Open the PC application.
2. Select offline mode and click OK.
3. Browse and select the previously saved .wav file and click OK.
4. View the static ECG waveforms along with the heart rate and lead-off status on the PC application.

7 Options and Selections

7.1 On the VC5505 EVM

7.1.1 ECG Display on the VC5505 EVM Side

The ECG display on the LCD screen starts by showing the *ECG Monitor* followed by lead and heart rate; by default, ECG Lead II is displayed.

SW7 switch on the EVM can be pressed to view one channel after the other. Pressing the switch displays the next ECG lead in a cyclic manner: II, I, III, aVR, aVL, aVF, V1, V2, V3, V4, V5 and V6.

The SW8 switch on the EVM can be used for the zoom in and zoom out feature for the ECG waveform. Low, Medium (default) and High are the three levels of zooming provided.

If all 10 leads are connected, a green color dot is displayed at the lead status location on the EVM display. In case any one lead fails, the failed lead name is displayed at the lead status location. If more than one lead off is detected, a red color dot is displayed at the lead status location.

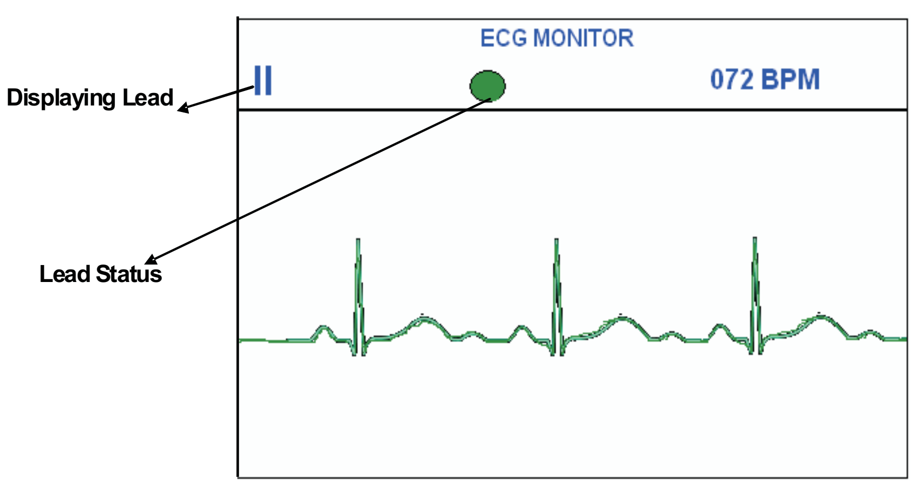


Figure 21. Display on the EVM LCD Screen

7.1.2 PC Application

Figure 17 shows the PC monitor application in online mode. By default, three leads are displayed simultaneously. The sequence of the leads are I, II, III, aVR, aVL, aVF, V1, V2, V3, V4, V5 and V6. Lead-off status and heart rates are displayed on the screen and the values are refreshed once every second. The serial port connection status (RS232) for the device is displayed on the status bar.

The following features are available on the PC application.

- **Next (up arrow)** - This button can be used to view the next three lead wave forms.
- **Previous (down arrow) -** This button can be used to view the previous three lead wave forms.
- **Scaling on Amplitude -** This button can be used to vertically *zoom in* and *zoom out* of the ECG waveform display on the PC application.
- **Scaling on Time -** This button can be used to horizontally *zoom in* and *zoom out* of the ECG waveform display on the PC application.
- **Start Recording** - This can be used to start the recording of the ECG waveform. During recording, this same button is used for the *Stop Recording* operation. Note that after the start recording option is selected, the zoom options get disabled.
- **Stop Recording** - This can be used to stop recording and save the ECG waveform as an .ECG file. It can be played back using the PC application in offline mode.
- **Freeze -** This button can be used to view a static waveform. Particular portions of the waveform can be viewed by moving the Left and Right cursors during the Freeze option.
- **Unfreeze** - Pressing this button enables the waveform to be in continuous scrolling mode.
- **Cancel**: This can be used to close the form.

8 References

- *TMS320VC5505 DSP Medical Development Kit (MDK) Quick Start Guide* (SPRUGO1)

Appendix A Front-End Board Schematics

A Front-End Board Schematics

The schematics for the ECG front-end board are shown below:

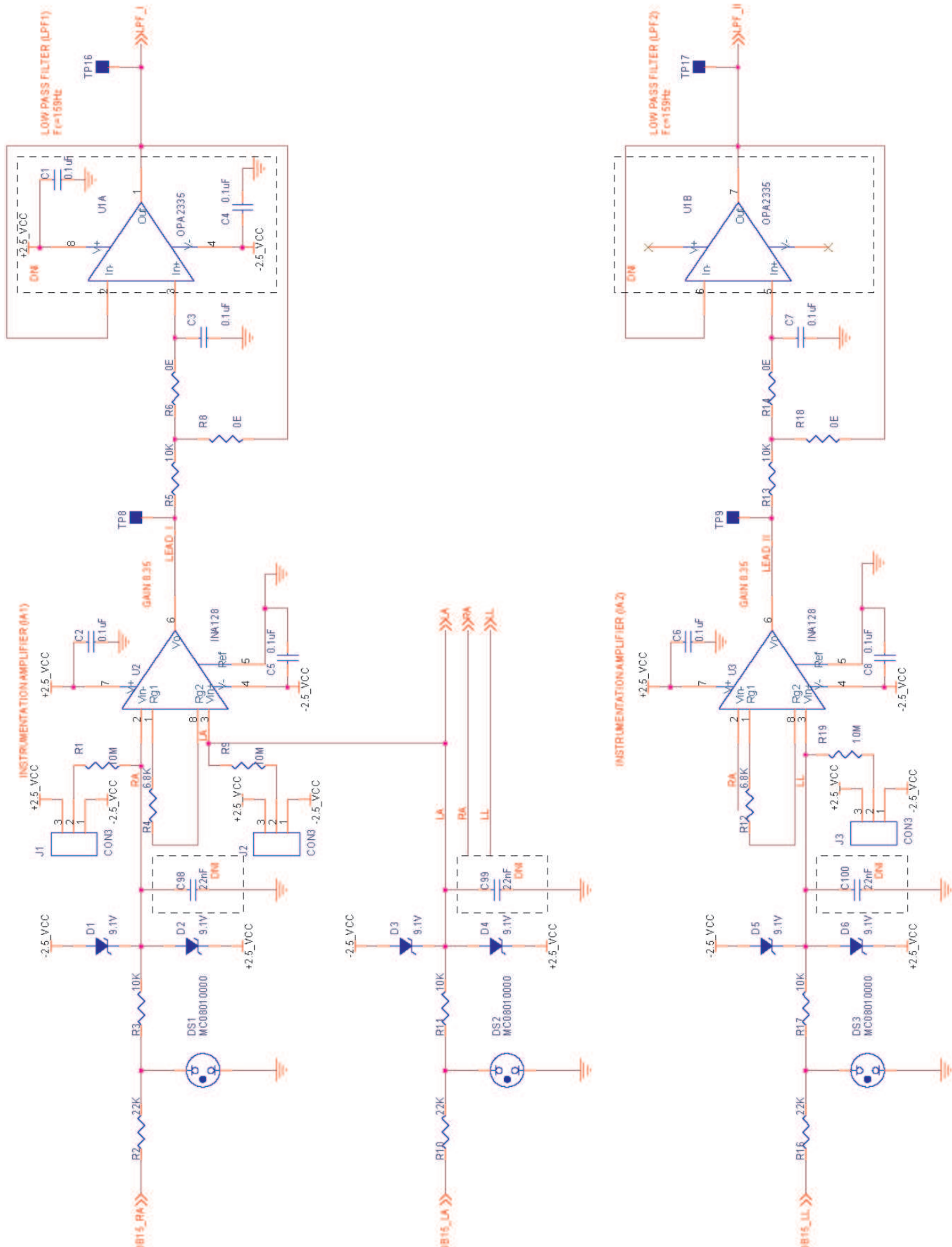


Figure A-1. ECG_I_II

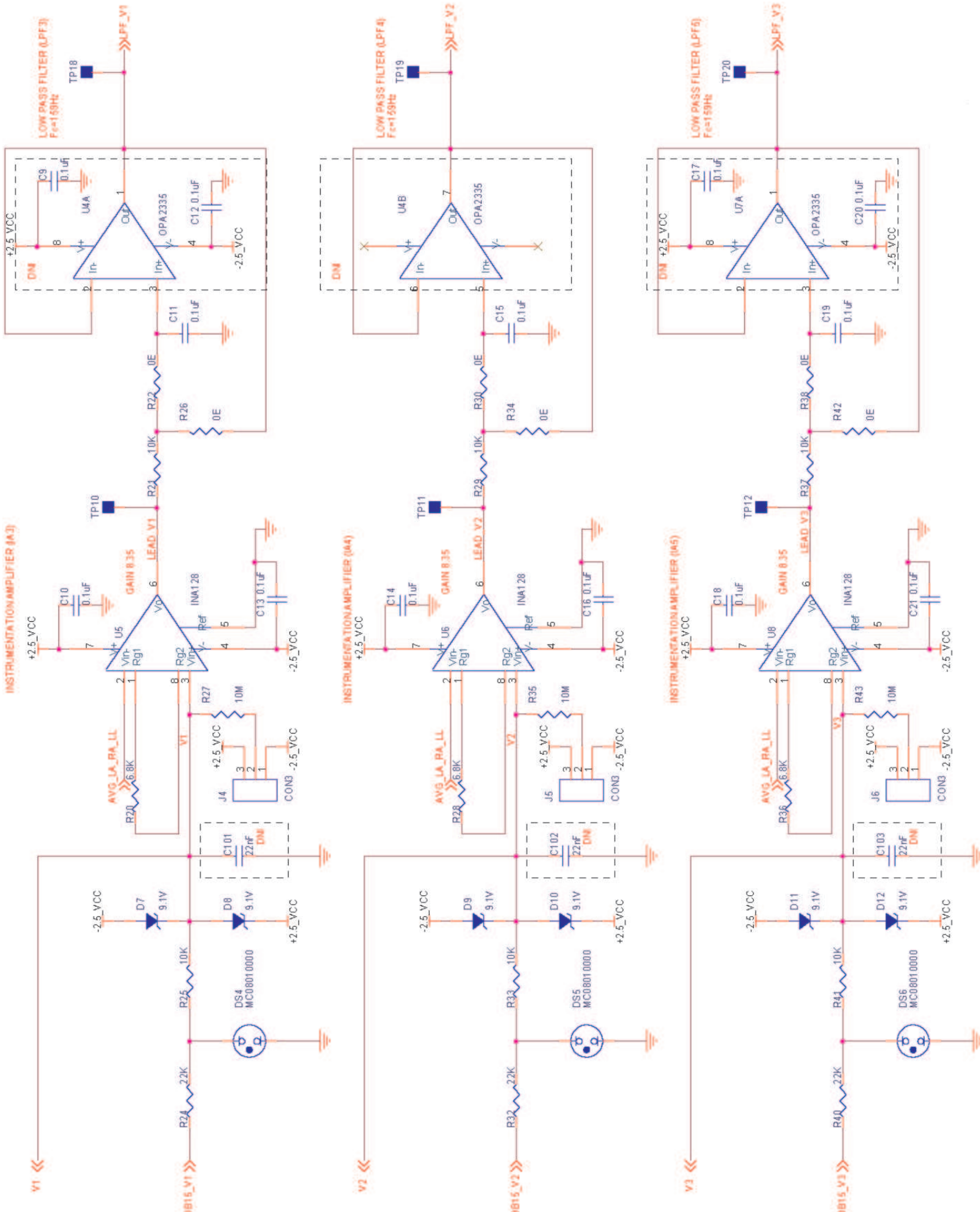


Figure A-2. ECG_LEAD_V1_V2_V3

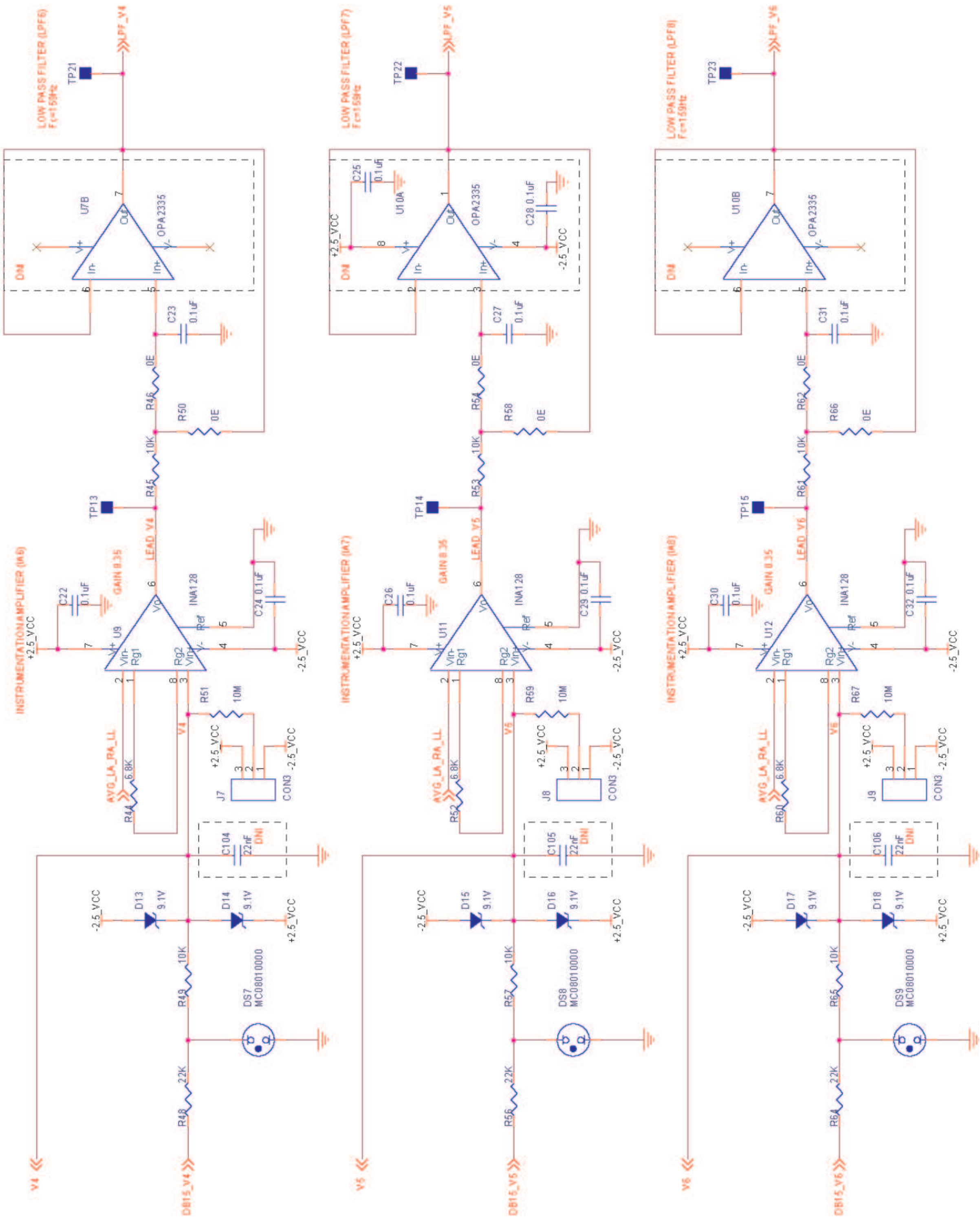


Figure A-3. ECG_LEAD_V4_V5_V6

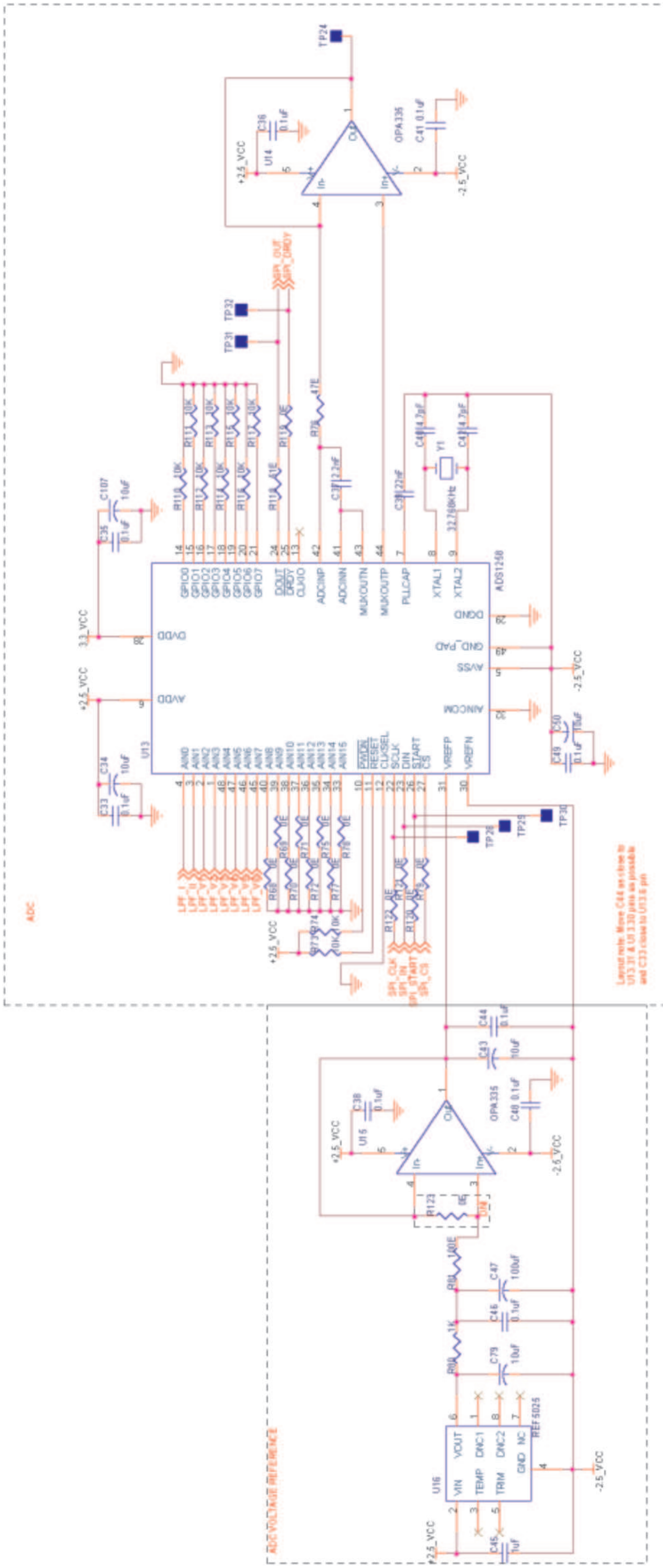


Figure A-4. ECG_ADC

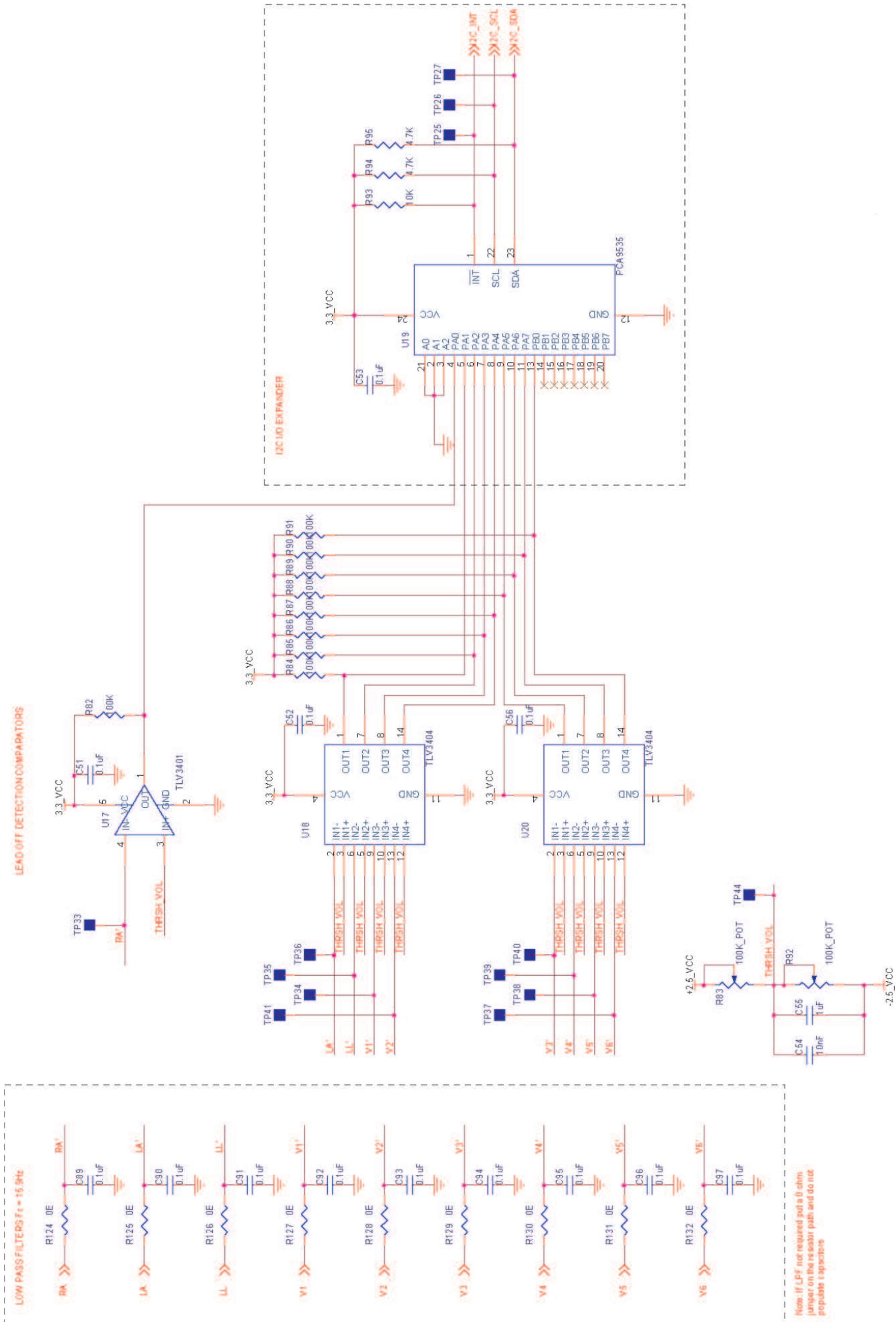


Figure A-5. ECG_LEAD_OFF_DET

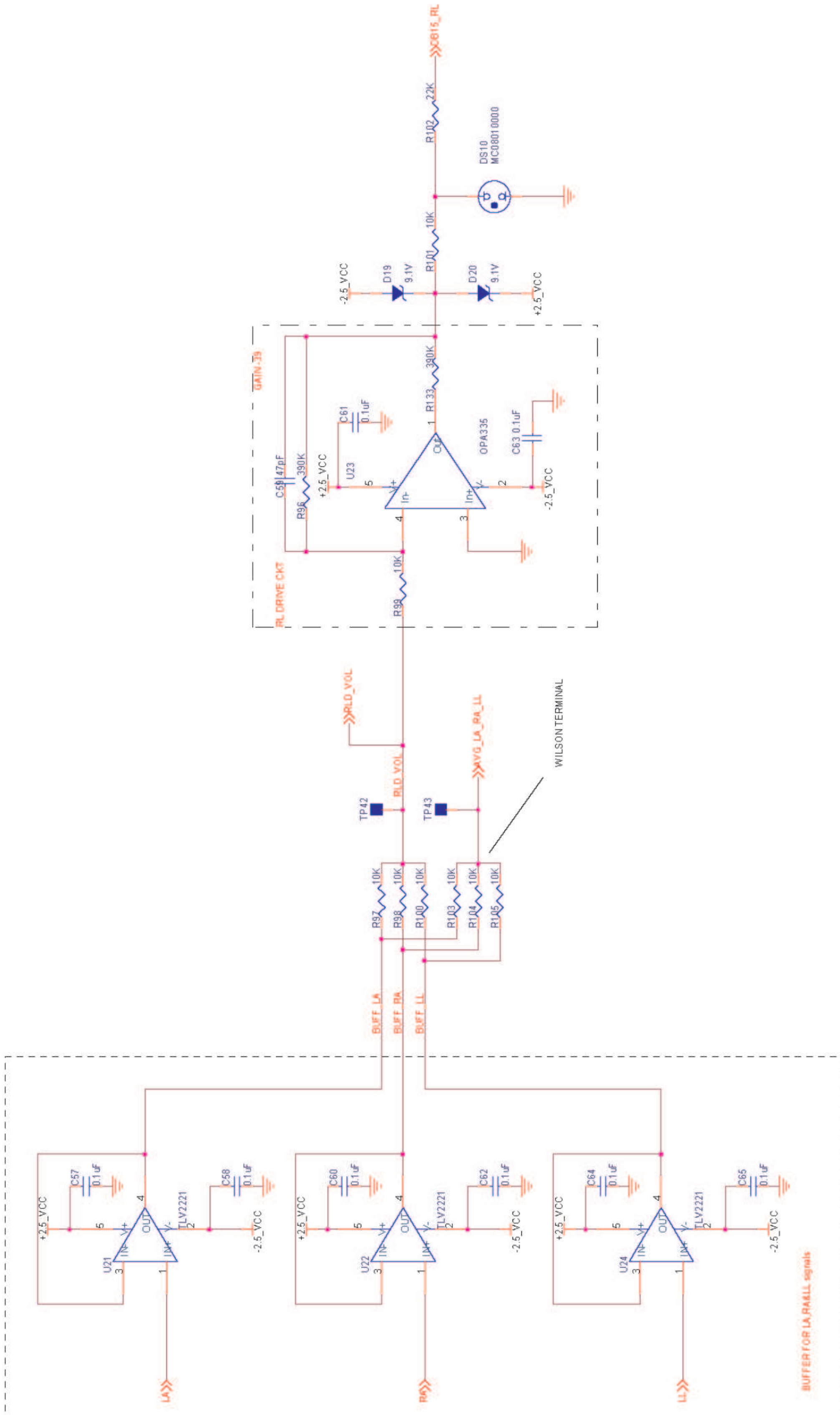


Figure A-6. Right Leg Drive

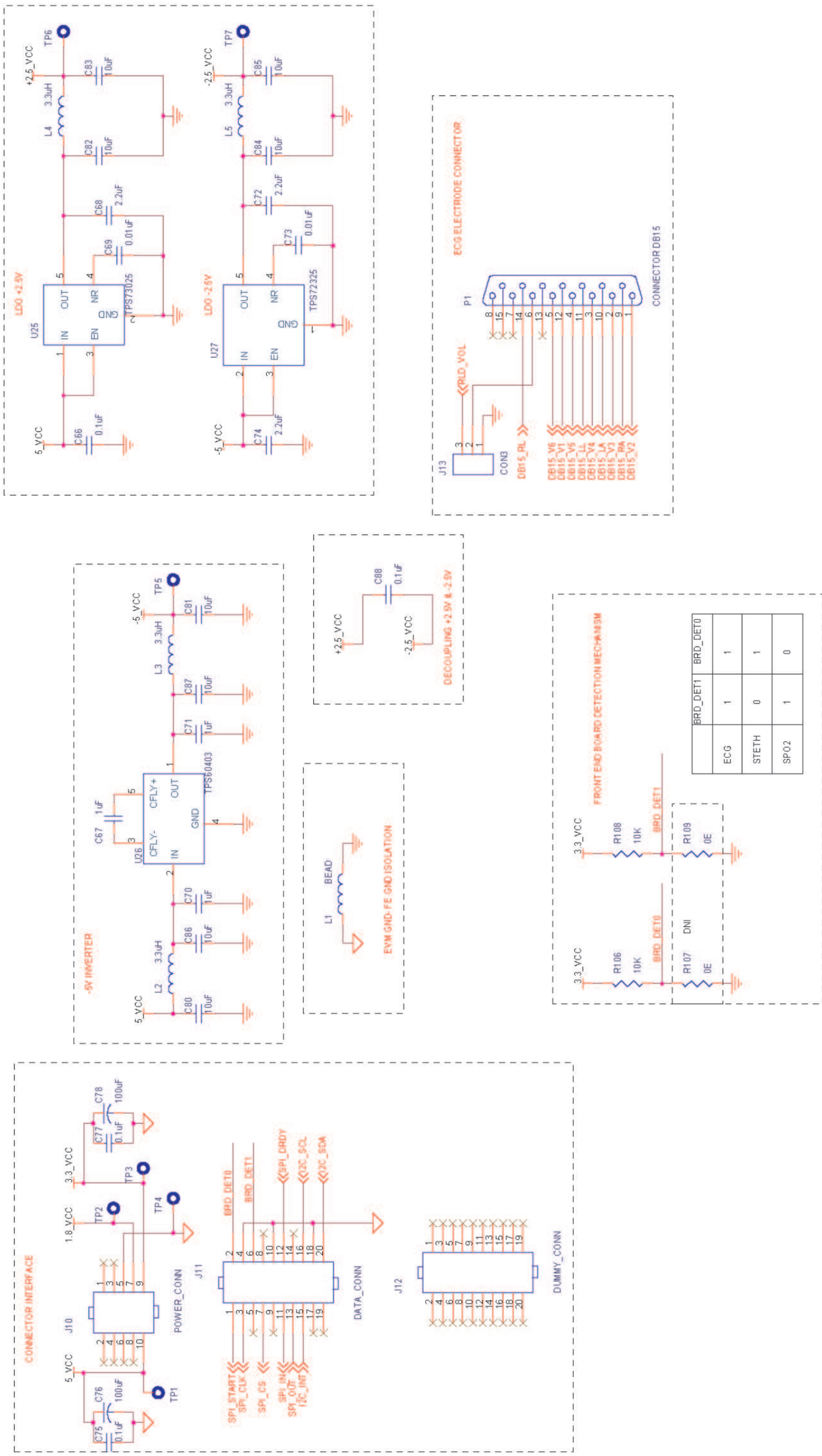


Figure A-7. PWR_CONN_INTRFCE

Appendix B Front-End Board BOM

B.1 Front-End Board BOM

Table B-1 provides the bill of material for the digital stethoscope front-end board.

Table B-1. Bill of Material

Item	Quantity	Value	Reference	Description	Part Number	Manufacturer	DNI
1	17	0.1 µF	C1,C4,C9,C12,C17, C20,C25,C28,C89, C90,C91,C92,C93, C94,C95,C96,C97	CAP CERM 0.10 µF 50 V 5% 0805 SMD	08055C104JAT2A	AVX Corporation	DNI
2	49	0.1 µF	C2,C3,C5,C6,C7, C8,C10,C11,C13, C14,C15,C16,C18, C19,C21,C22,C23, C24,C26,C35,C36, C38,C41,C44,C46, C27,C29,C30,C31, C32,C33, 48,C49, C51,C52,C53,C56, C64,C65,C66,C75, C77,C88 C57,C58, C60,C61,C62,C63	CAP CERM 0.10 µF 50 V 5% 0805 SMD	08055C104JAT2A	AVX Corporation	
3	5	10 µF	C34,C43,C50,C79, C107	CAP TANT LOESR 10 µF 16 V 10% SMD	TPSB106K016R0800	AVX Corporation	
4	1	2.2 nF	C37	CAP CERM 2200 pF 5% 50 V NPO 0805	08055A222JAT2A	AVX Corporation	
5	1	22 nF	C39	CAP CER 22000 pF 50 V X7R 0805	08055C223J4T2A	AVX Corporation	
6	2	4.7 nF	C40,C42	CAP CER 4.7 pF 50 V NPO 0805	08055A4R7BAT2A	AVX Corporation	
7	5	1 µF	C45,C55,C67,C70, C71	CAP CERM 1.0 µF 10% 25 V X7R 0805	08053C105KAZ2A	AVX Corporation	
8	3	100 µF	C47,C76,C78	CAP ELECT 100 µUF 16 V TK SMD	EEE-TK1C101P	Panasonic-ECG	
9	1	10 nF	C54	CAP CER 10000 pF 16 V NPO 0805	0805YA103JAT4A	AVX Corporation	
10	13	47 pF	C59	CAP CERM 47 pF 5% 50 V NPO 0805	08055A470JAT2A	AVX Corporation	
11	3	2.2 µF	C68,C72,C74	CAP CER 2.2 µUF 25 V X7R 0805	08053C225MAT2A	AVX Corporation	
12	2	0.01 µF	C69,C73	CAP CERM 0.01 10% 50 V X7R 0805	08055C103KAT2A	AVX Corporation	
13	8	10 µF	C80,C81,C82,C83,C84, C85, C86,C87	CAP CER 10 µF 16 V X5R 0805	EMK212BJ106KG-T	Taiyo Yuden	
14	9	22 nF	C98,C99,C100,C101,C102, C103,C104,C105,C106	CAP CER 22000 pF 50 V X7R 0805	08055C223J4T2A	AVX Corporation	
15	10	MC08010000	DS1,DS2,DS3,DS4,DS5, DS6, DS7,DS8,DS9,DS10	Neon lamp	MC08010000	Multicomp	
16	20	9.1 V	D1,D2,D3,D4,D5,D6,D7, D8, D9,D10,D11,D12,D13,D14, D15,D16,D17,D18,D19, D20	DIODE ZENER 1W 9.1 V SOD-106	PTZTE259.1B	ROHM	
17	10	CON3	J1,J2,J3,J4,J5,J6,J7, J8, J9,J13	CONN HEADER 3POS .100 VERT TIN	22-28-4030	Molex	
18	1	POWER_CONN	J10	Elevated Female Header 5x2	BB02-KD102-T03-100000	Gradconn	
19	1	DATA_CONN	J11	Elevated Female Header 10x2	BB02-KD202-T03-100000	Gradconn	

Table B-1. Bill of Material (continued)

Item	Quantity	Value	Reference	Description	Part Number	Manufacturer	DNI
20	1	DUMMY_CONN	J12	Elevated Female Header 10x2	BB02-KD202-T03-100000	Gradconn	
21	1	BEAD	L1	FERRITE BEAD 470 Ω 0805	BK2125HM471-T	Taiyo Yuden	
22	4	3.3 µH	L2,L3,L4,L5	INDUCTOR POWER 3.3 µH 1.3A SMD	VLF4012AT-3R3M1R3	DK Corporation	
23	1	CONNECTOR DB15	P1	CONN D-SUB RCPT R/A 15POS PCB AU	745782-4	Tyco Electronics	
24	9	10M	R1,R9,R19,R27,R35,R43, R51,R59,R67	RES 10.0MΩ 1/8W 1% 0805 SMD	CRCW080510M0FKEA	Vishay	
25	10	22K	R2,R10,R16,R24,R32,R40,R48,R56,R64,R102	RES 22KΩ 1W 5% 2512 SMD	CRCW251222K0JNEG	Vishay	
26	10	10K	R3,R11,R17,R25, R33,R41, R49,R57,R65,R101	RES 10KΩ 1/2W 5% 2010 SMD	CRCW201010K0JNEF	Vishay	
27	8	6.8K	R4,R12,R20,R28,R36, R44, R52,R60	High Precision Chip Resistor 6.8KΩ	Y162406K8000T9R	Vishay	
28	15	10K	R5,R13,R21,R29,R37, R45,R53,R61,R97, R98, R99,R100, R103,R104,R105	High Precision Chip Resistor 10KΩ	Y162410K0000T9R	Vishay	
29	38	0E	R6,R8,R14,R18,R22, R26,R30,R34,R38, R42,R46,R50,R54, R58,R62,R66,R68, R69,R70,R71,R72, R75,R77,R78, R79, R119,R120,R121, R122,R124,R125, R126,R127,R128, R129,R130,R131, R132	RES 0.0 Ω 1/8W 5% 0805 SMD	CRCW08050000Z0EA	Vishay	
30	11	10K	R73,R74,R93,R110, R111,R112,R113, R114,R115,R116, R117	RES 10.0KΩ 1/8W 1% 0805 SMD	CRCW080510K0FKEA	Vishay	
31	1	47E	R76	High Precision Chip Resistor 47 Ω	Y162447R0000T9R	Vishay	
32	1	1K	R80	RES 1.00KΩ 1/8 W 1% 0805 SMD	CRCW08051K00FKEA	Vishay	
33	1	100E	R81	High Precision Chip Resistor 100 µ	Y1624100R000T9R	Vishay	
34	9	100K	R82,R84,R85,R86, R87,R88,R89,R90, R91	RES 100KΩ 1/8W 1% 0805 SMD	CRCW0805100KFKEA	Vishay	
35	2	100K_POT	R83,R92	POT 100KΩ 4MM SQ CERMET SMD	3314G-1-104E	Bourns Inc	
36	2	4.7K	R95,R94	RES 4.70KΩ 1/8W 1% 0805 SMD	CRCW08054K70FKEA	Vishay	
37	2	390K	R96,R133	High Precision Chip Resistor 390KΩ	TNPW0805390KBYTA	Vishay	
38	2	10K	R108,R106	RES 10.0KΩ 1/8W 1% 0805 SMD	CRCW080510K0FKEA	Vishay	DNI
39	3	0E	R107,R109,R123	RES 0.0 Ω 1/8W 5% 0805 SMD	CRCW08050000Z0EA	Vishay	DNI
40	1	51E	R118	RES 51 Ω 1/8W 5% 0805 SMD	CRCW080551R0JNEA	Vishay	
41	4	OPA2335	U1,U4,U7,U10	IC OP AMP CMOS SGL SPLY 8-MSOP	OPA2335AIDGKT	TI	DNI
42	8	INA128	U2,U3,U5,U6,U8,U9,U11, U12	IC LOW PWR INSTR AMP 8-SOIC	INA128UA	TI	
43	1	ADS1258	U13	IC ADC 24 BIT 125 ksps 48-QFN	ADS1258IRTCT	TI	
44	3	OPA335	U14,U15,U23	IC OP AMP CMOS SGL SPLY SOT-23-5	OPA335AIDBVT	TI	
45	1	REF5025	U16	IC PREC V-REF 2.5 V LN 8-SOIC	REF5025AID	TI	

Table B-1. Bill of Material (continued)

Item	Quantity	Value	Reference	Description	Part Number	Manufacturer	DNI
46	1	TLV3401	U17	IC OUT COMPARATOR NANOPWR SOT23-5	TLV3401IDBVR	TI	
47	2	TLV3404	U18,U20	COMPARATOR LW POWER R-R 14-SOIC	TLV3404IDR	TI	
48	1	PCA9535	U19	IC REMOTE 16-BIT I/O EXP 24-TSSOP	PCA9535PWR	TI	
49	3	TLV2221	U21,U22,U24	IC RAIL-TO-RAIL OP AMP SOT-23-5	TLV2221CDBVR	TI	
50	1	TPS73025	U25	IC LDO REG HI-PSRR 2.5 V SOT23-5	TPS73025DBV	TI	
51	1	TPS60403	U26	IC UNREG CHRG PUMP V INV SOT23-5	TPS60403DBVT	TI	
52	1	TPS72325	U27	IC LDO REG 200MA 2.5 V SOT23-5	TPS72325DBVT	TI	
53	1	32.768KHz	Y1	CRYSTAL 32.7680 KHz 12.5 pF CYL	C-001R 32.7680K-A:PBFREE	Epson Toyocom Corporation	

Appendix C Sensors and Accessories

C.1 ECG Cable Details

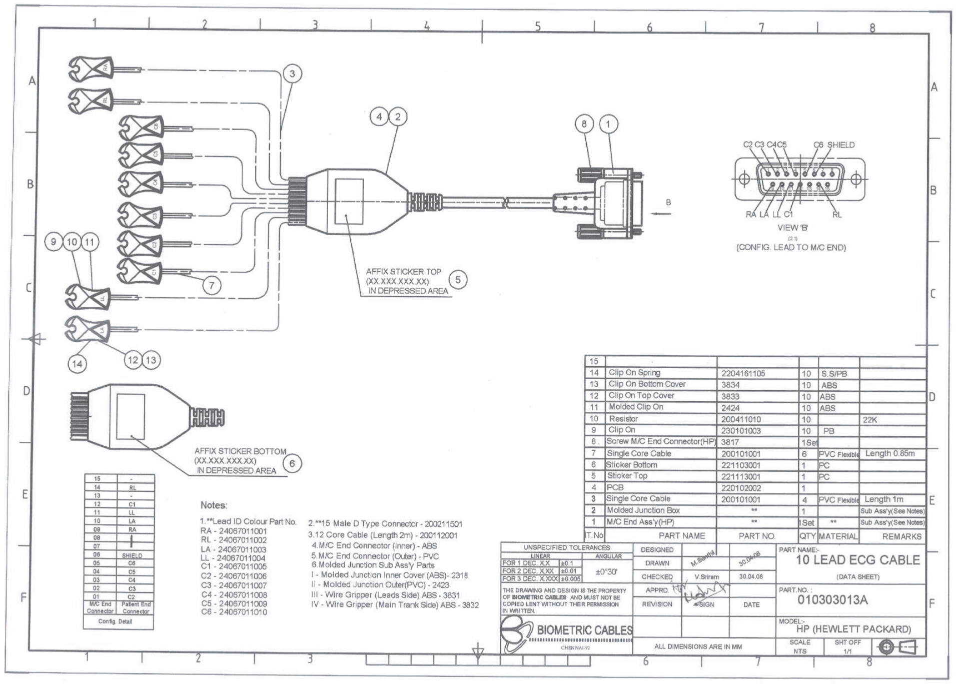


Figure C-1. ECG Cable Details

Cable details: 10 lead ECG cable for philips/hp -snap, button (Part No: 010302013)
http://www.biometriccables.com/index.php?productID=692

Cable details: 10 lead ECG cable for philips/hp -Clip-on type (P/n-010303013A)
http://www.biometriccables.com/index.php?productID=693

Other compatible cables for MDK: HP/Philips/Agilent Compatible 10 Lead ECG cable

C.2 ECG Sensor

Sensor details: Disposable Electrodes - Medico Lead - Lok

Vendor name: Medico Electrodes International Link : http://www.medicoleadlok.com/

Other compatible parts: Any Ag/AgCl solid gel ECG electrode on the market.

Appendix D MEDICAL DEVELOPMENT KIT (MDK) WARNINGS, RESTRICTIONS AND DISCLAIMER

Not for Diagnostic Use: Not for Use with a Defibrillator: For Feasibility Evaluation Only in Laboratory/Development Environments.

- The MDK must not be used for diagnostic purposes.
- The MDK must not be used with a defibrillator or other equipment that produces high voltages in excess of the output supply provided by the AC adapter provided with this ECG device.
- This MDK is intended solely for evaluation and development purposes. It is not intended for use and may not be used as all or part of an end equipment product.
- This MDK should be used solely by qualified engineers and technicians who are familiar with the risks associated with handling electrical and mechanical components, systems and subsystems.
- You are responsible for the safety of you and your employees and contractors when using or handling the MDK. Further, you are responsible for ensuring that any contacts or interfaces between the MDK and any human body are designed to be safe and to avoid the risk of electrical shock. To minimize risk of electric shock hazard, use only the following power supplies for the EVM module: Medical Development Applications: SL Power AULT Model MW173KB0503F01.

Your Obligations and Responsibilities.

Please consult the *TMS320VC5505 DSP Medical Development Kit (MDK) Quick Start Guide* (SPRUGO1) prior to using the MDK. Any use of the MDK outside of the specified operating range may cause danger to the users and/or produce unintended results, inaccurate operation, and permanent damage to the MDK and associated electronics. You acknowledge and agree that:

- You are responsible for compliance with all applicable Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, UL, CSA, VDE, CE, RoHS and WEEE,) that relate to your use (and that of your employees, contractors or designees) of the MDK for evaluation, testing and other purposes.