SoC Test Board

REVISION HISTORY

DATE:	DESCRIPTION	REVISION
08/16/10	Initial	1.0
01/31/11	Pull up Pin EROEN make WRSTO active low. Invert the WRSTO before it generates the G_RESETN.	1.1

MICREL SEMICONDUCTOR		
Title: SoC Test Board		
Size: Custom	Document Number: Revision History	Rev: 1.1
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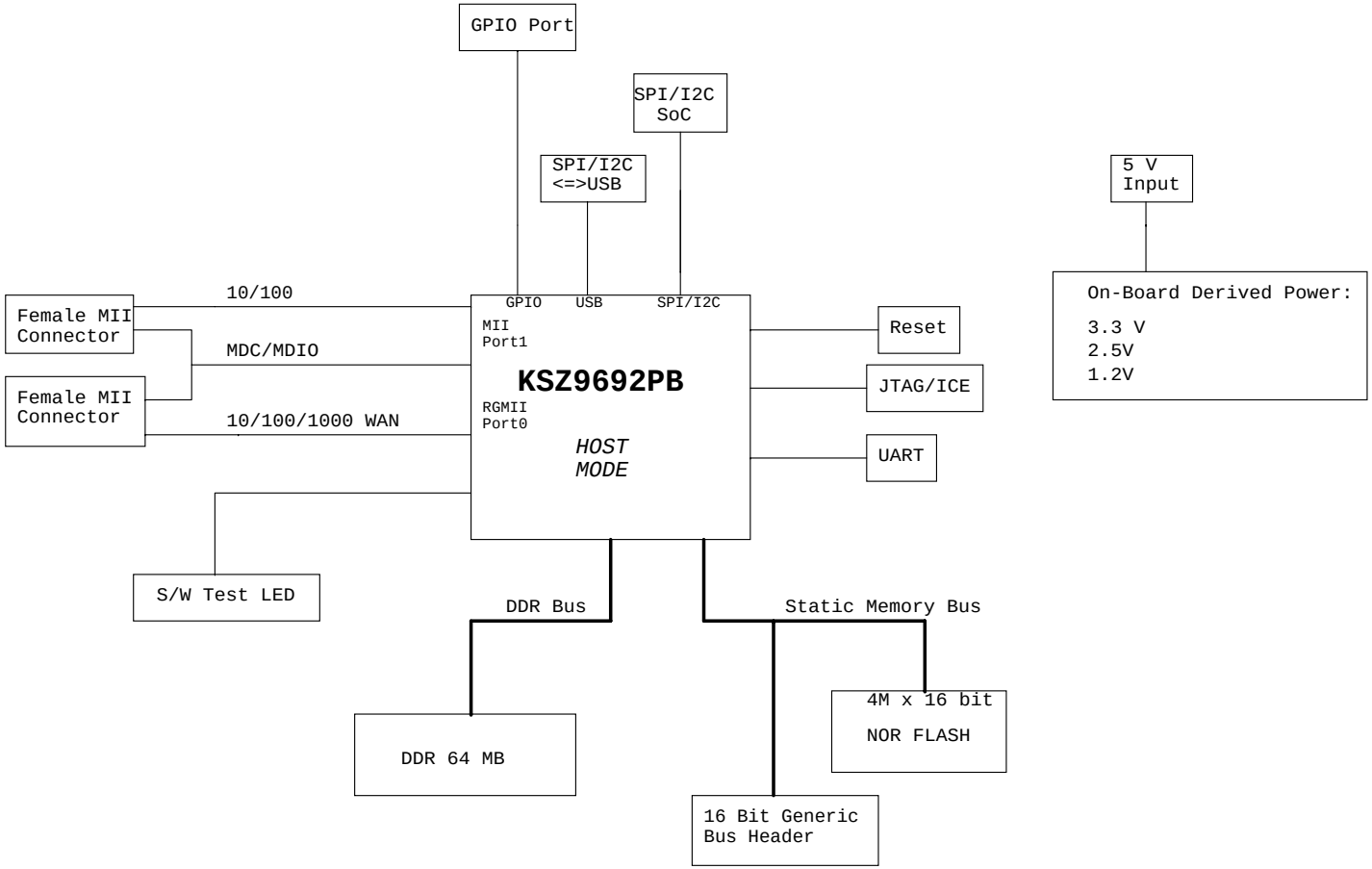

MICREL SEMICONDUCTOR		
Title: SoC Test Board		
Size: Custom	Document Number: Block Diagram	Rev: 1.0
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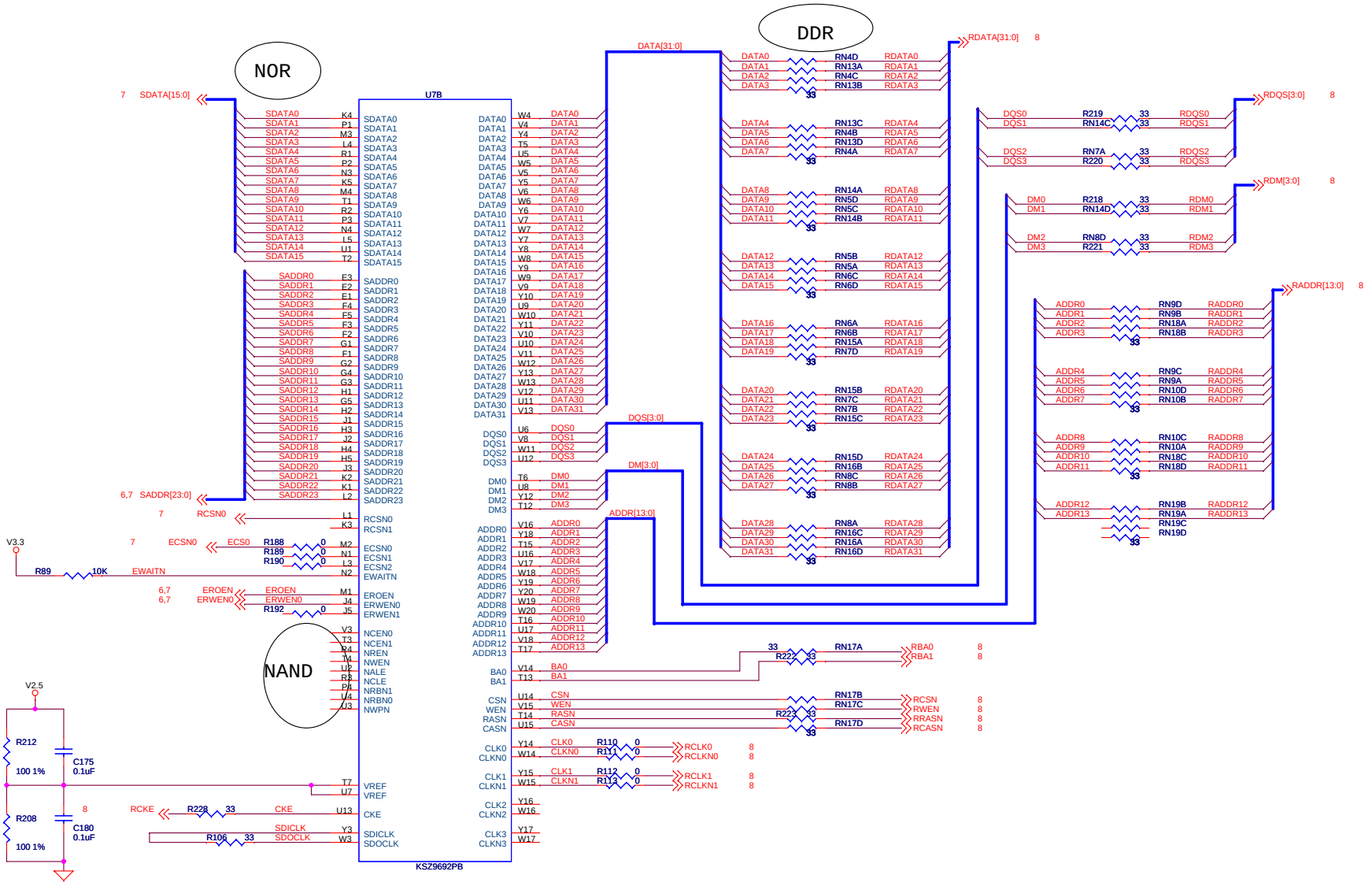
Note: Support DDR 32-bit data width.



MICREL SEMICONDUCTOR		
Title: SoC Test Board		
Size: Custom	Document Number: Memory Bus	Rev: 1.0
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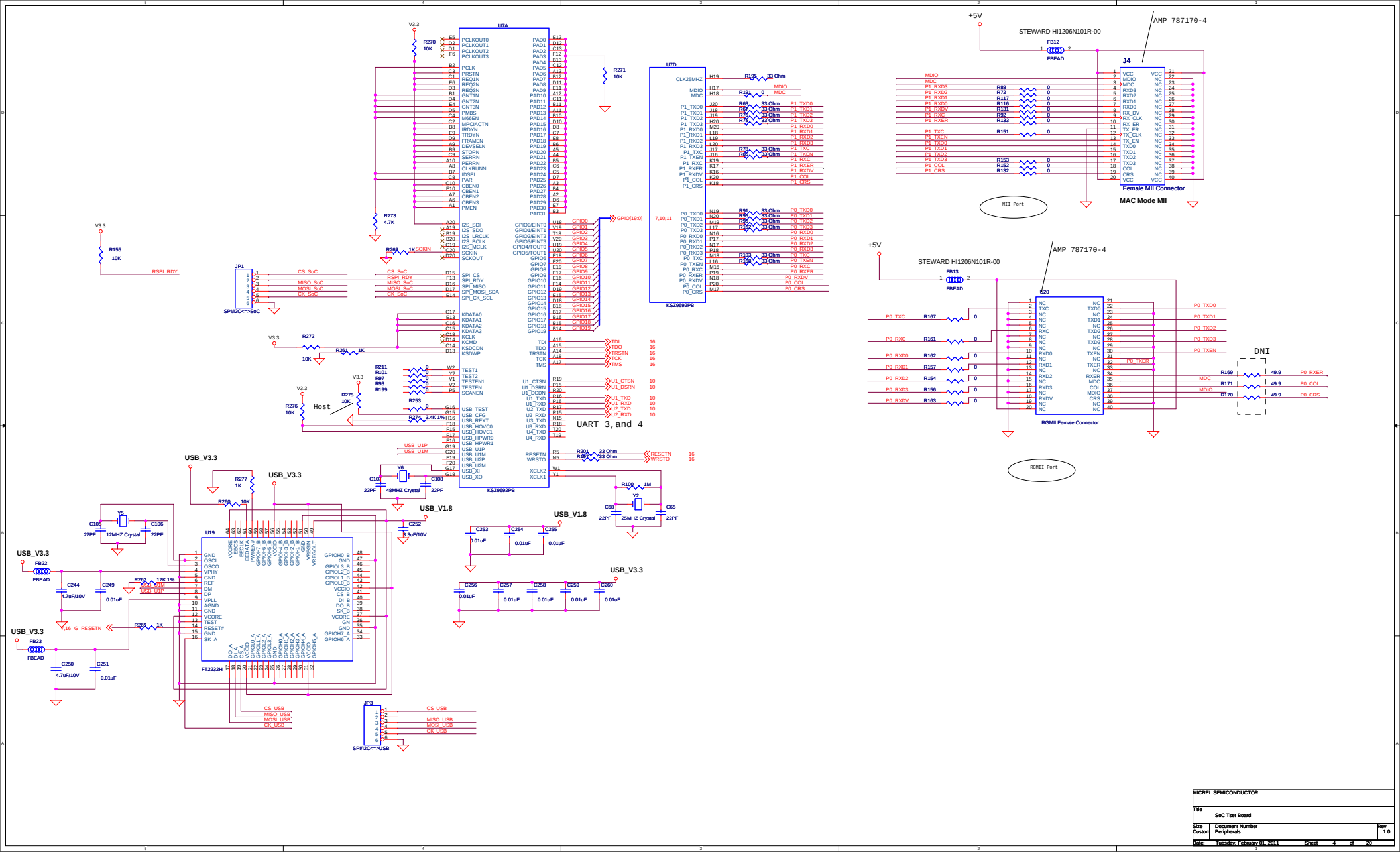

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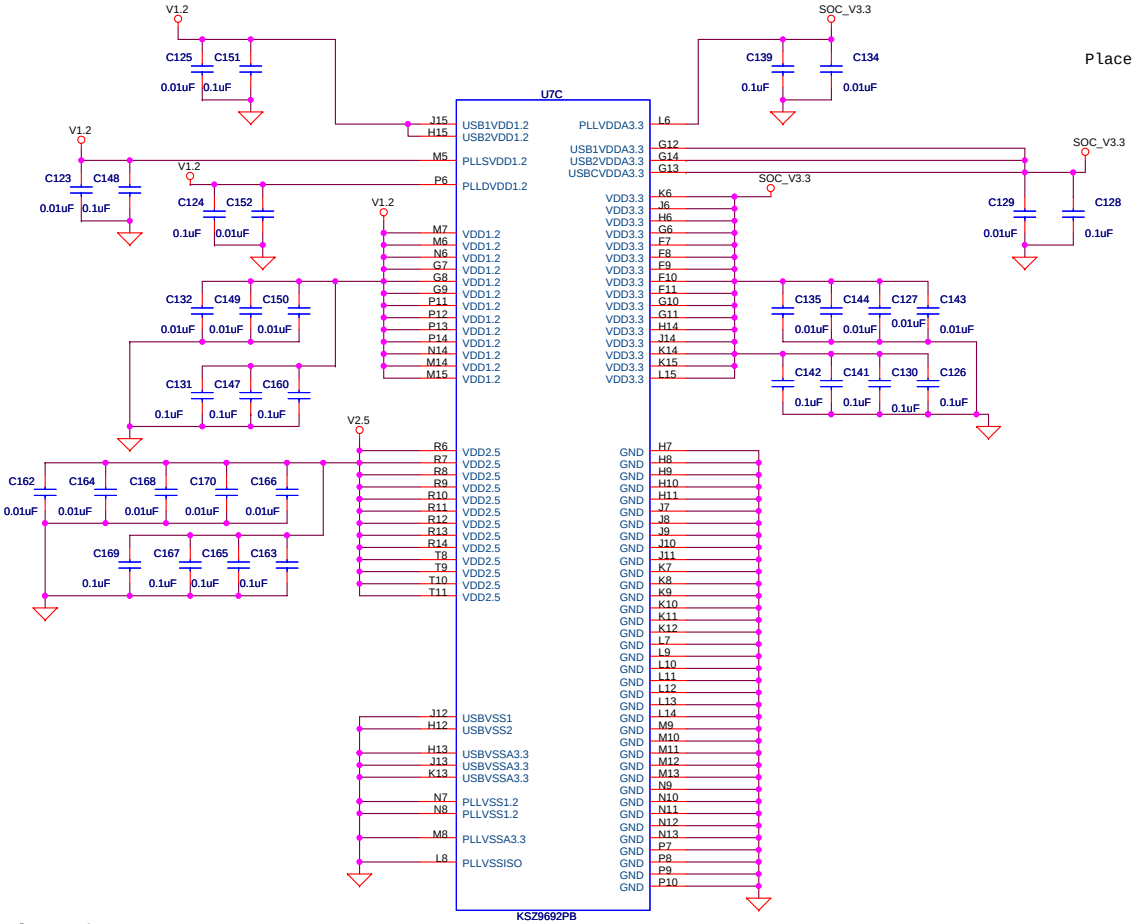
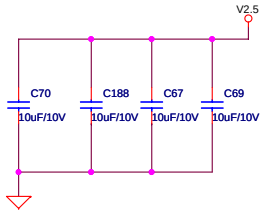
Place V1.2 bypass caps next to BGA power pins

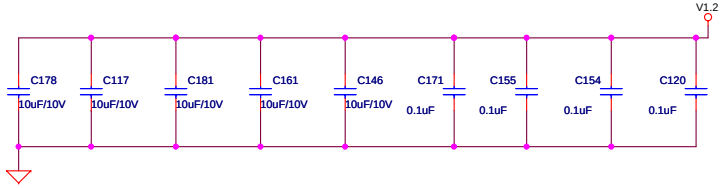
Place SOC_V3.3 bypass caps next to BGA power pins

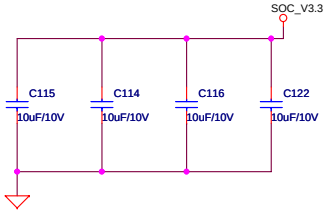
Place V2.5 bypass caps next to BGA power pins

Place caps close to the group of respective voltage pins









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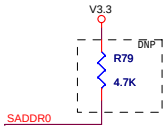
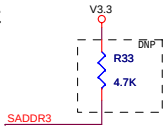
Not Support NAND Boot



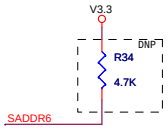
Internal Pull-Down: NAND boot device small page size 512 byte (default)

External Pull-Up: NAND boot device small page size 528 byte



Internal Pull-Down: NAND boot device small block size (default)

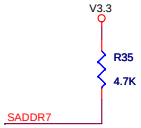
External Pull-Up: NAND boot device large block size



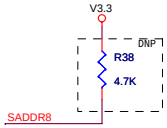
Internal Pull-Down: NAND FLASH device does not support automatic page crossing (default)

External Pull-Up: NAND FLASH device supports automatic page crossing

Not Support NAND Boot

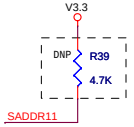


External Pull-Up: 16-bit boot device



Internal Pull-Down: boot from NOR device (default)

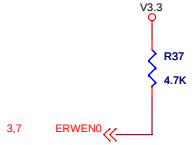
External Pull-Up: boot from NAND device



Port 1 Set to MII

Internal Pull-Down: MII mode (Default)

External Pull-Up: RGMII mode

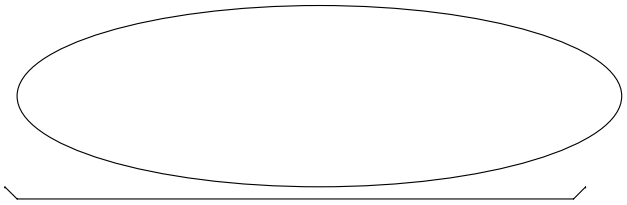


Port 0 Set to RGMII

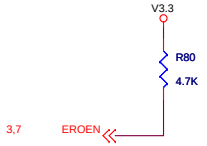
Internal Pull-Down: MII mode (default)

External Pull-Up: RGMII mode

NAND



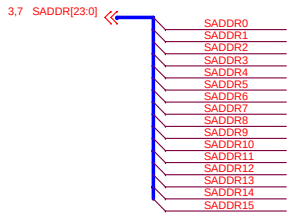
NAND boot device size:128Mbit (default)



For Globe Rest at page 7 (NOR), page 12 (WAN LAN), at Page 11 (Generate RESET signal)

External Pull-Up: WRSTO is active low

Pull-Down: WRSTO is active High (Default)



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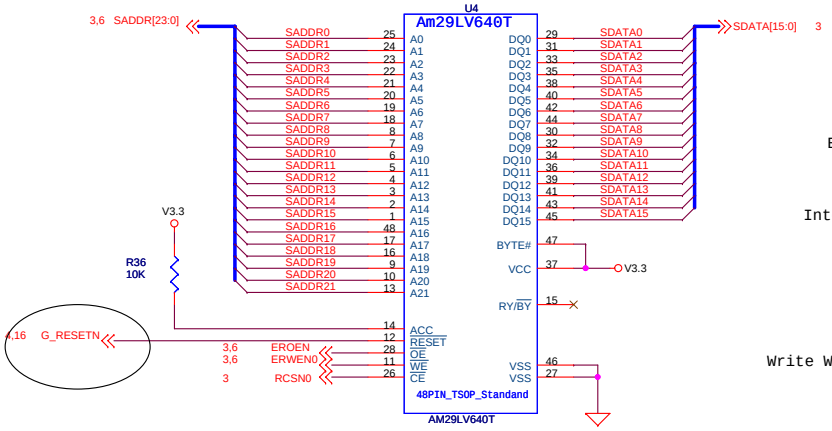
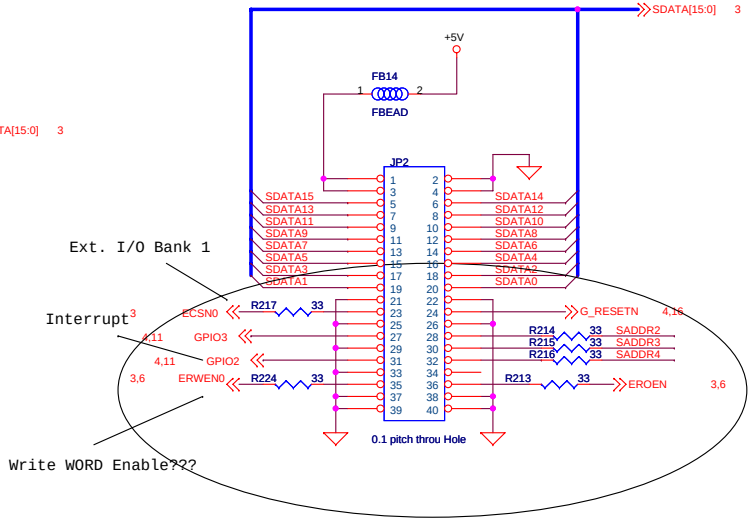
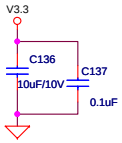
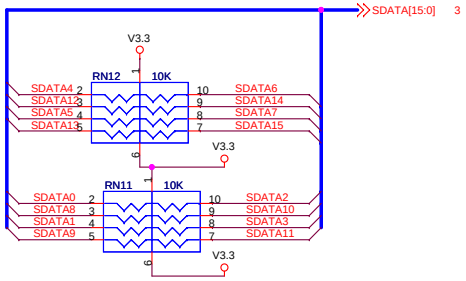
Boot NOR Flash







Static memory data bus pullup



MICREL SEMICONDUCTOR		
Title: SoC Tset Board		
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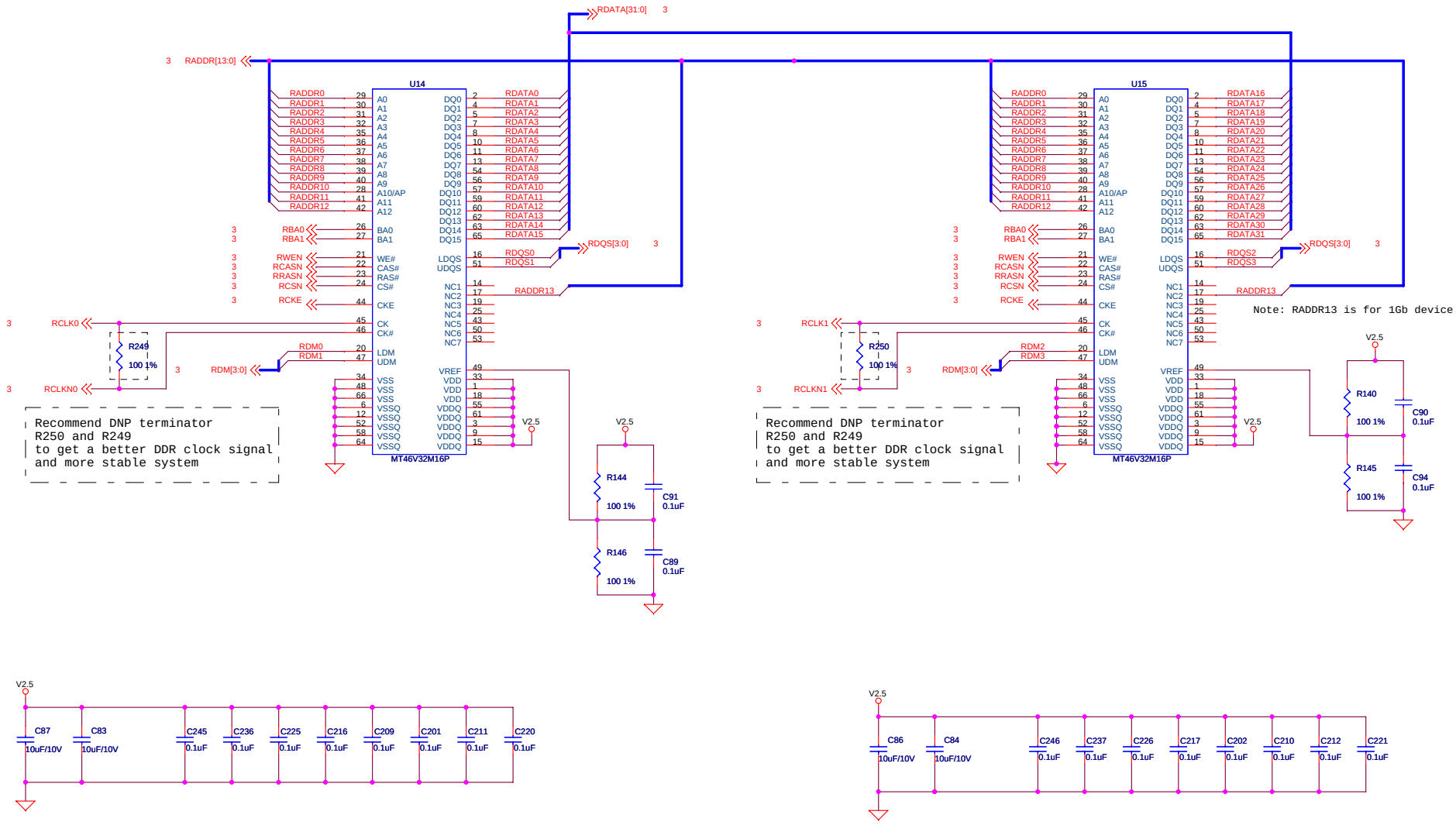
Note: Support DDR 32-bit data width



MICREL SEMICONDUCTOR		
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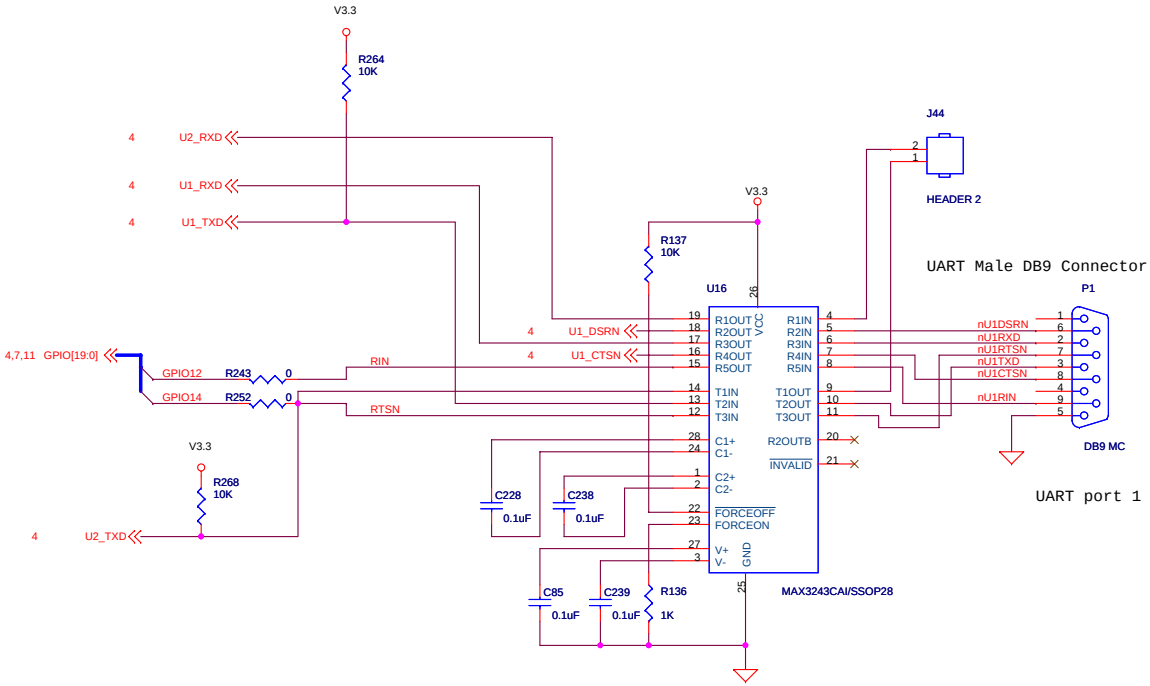

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Title: SoC Tset Board		
Size: Custom	Document Number: UART	Rev: 1.0
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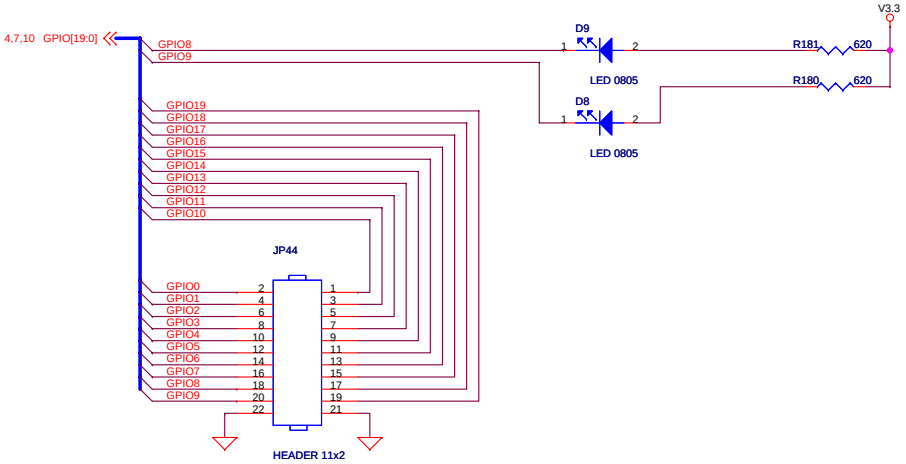
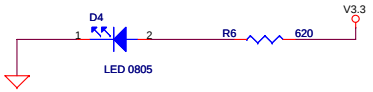
Programmable GPIO LED Indicators



User Programmable GPIO

3.3V POWER LED



MICREL SEMICONDUCTOR		
Title: SoC Tset Board		
Size: Custom	Document Number: GPIO-LED	Rev: 1.0
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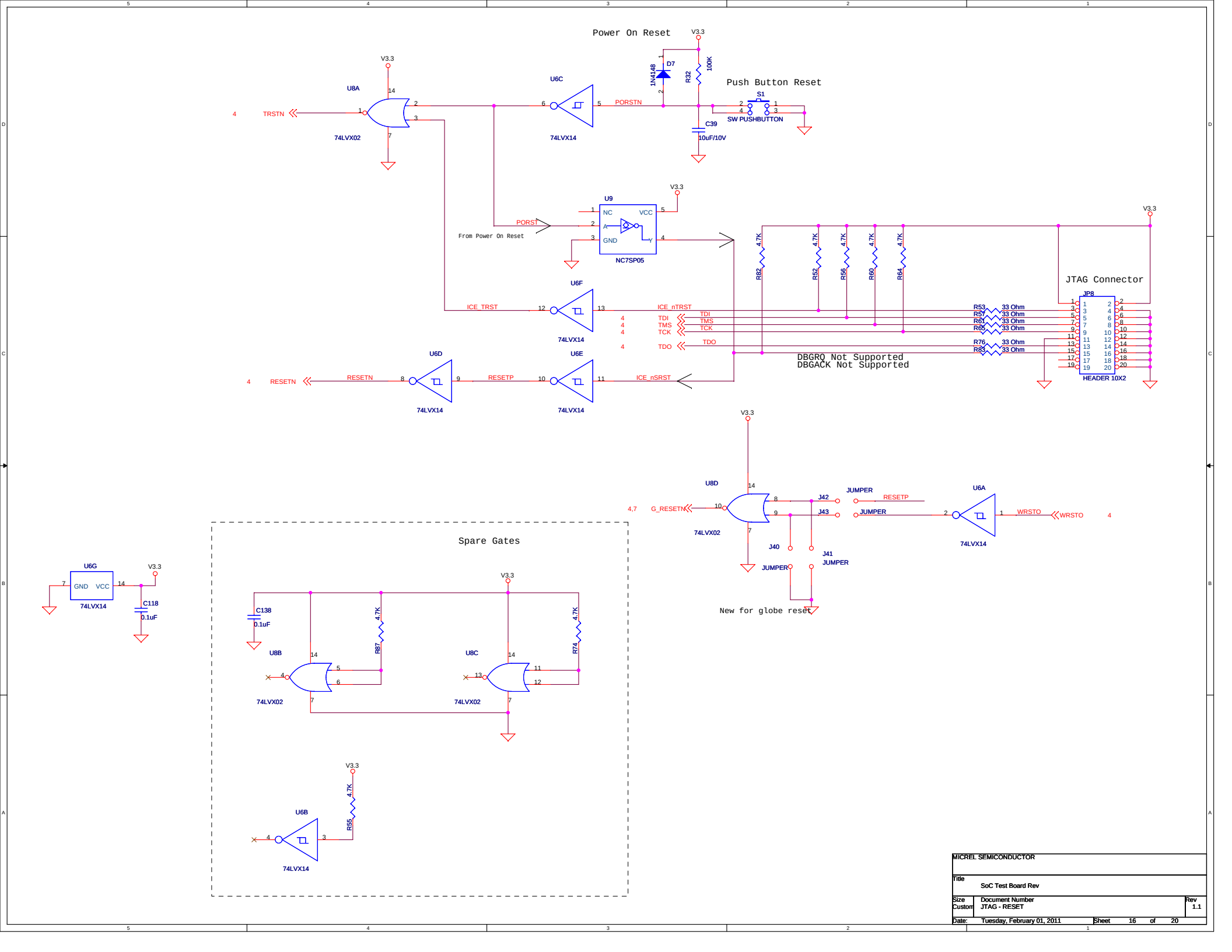
Power On Reset
Push Button Reset
SW PUSHBUTTON
JTAG Connector
HEADER 10X2
DBGRQ Not Supported
DBGACK Not Supported
From Power On Reset
New for globe reset
Spare Gates
MICREL SEMICONDUCTOR
Title
SoC Test Board Rev
Size
Custom
Document Number
JTAG - RESET
Rev
1.1
Date:
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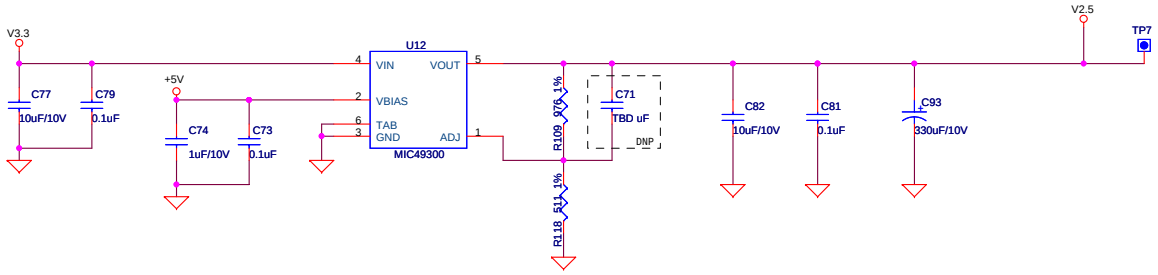
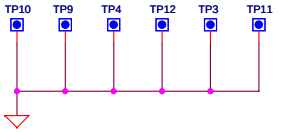


Note: V2.5 must be adjusted to 2.6V for Micron DDR device MT46V32M16-5B. See Micron Electrical Specification.
For DDR devices that require 2.5V, install 1K in R109, 562 ohm in R118

Ground Test Points



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Title: SoC Tset Board		
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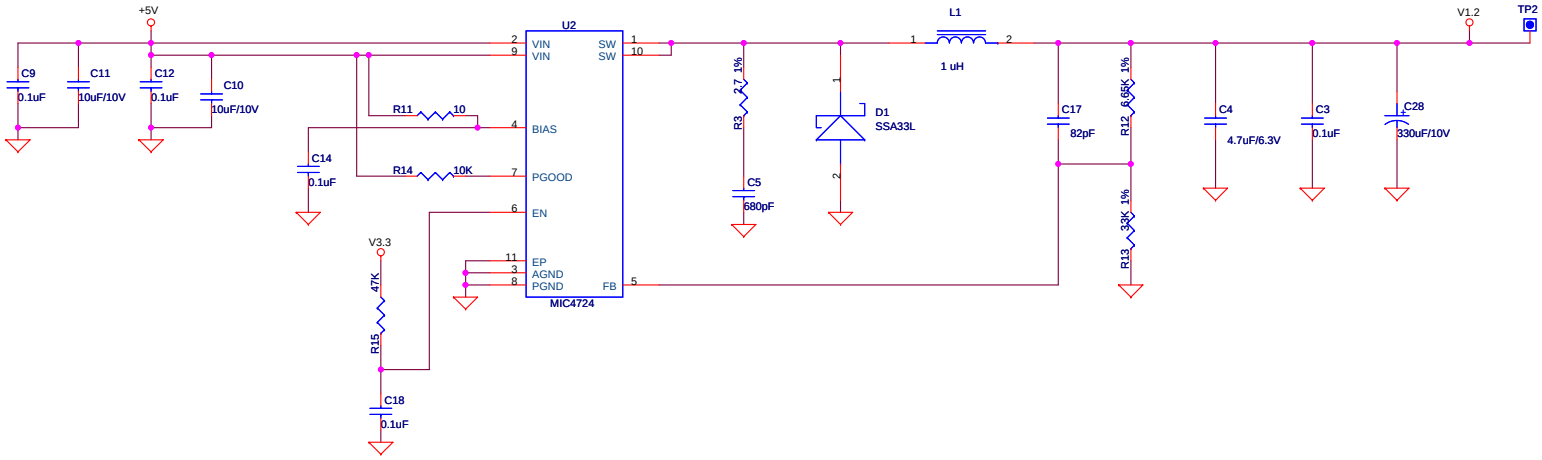

Note: RC added to EN control to enforce power sequencing

MICREL SEMICONDUCTOR		
Title: SoC Tset Board		
Size: Custom	Document Number: 1.2V Power	Rev: 1.0
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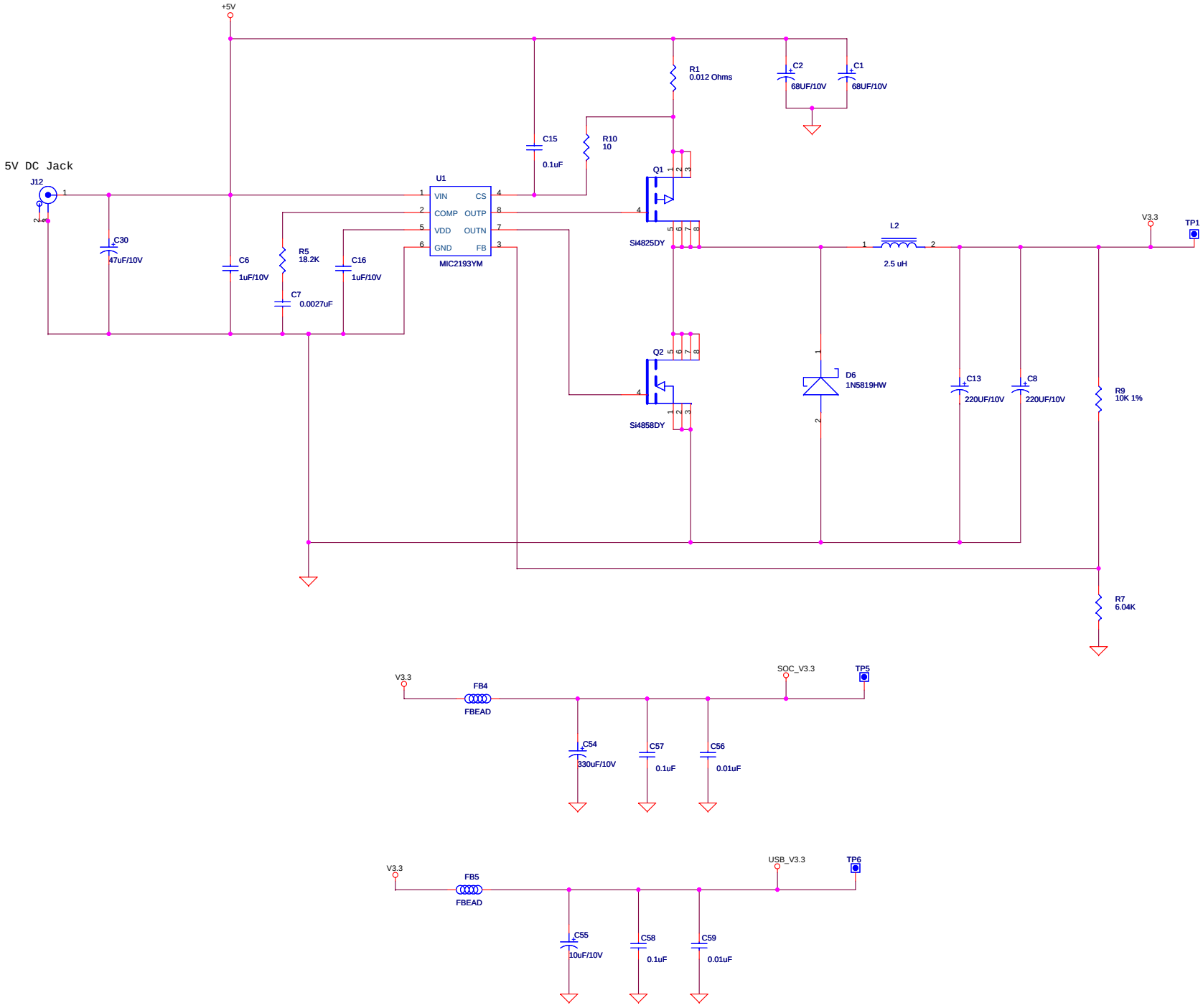

MICREL SEMICONDUCTOR		
Title: SoC Test Board		
Size: Custom	Document Number: 3.3V Power	Rev: 1.0
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