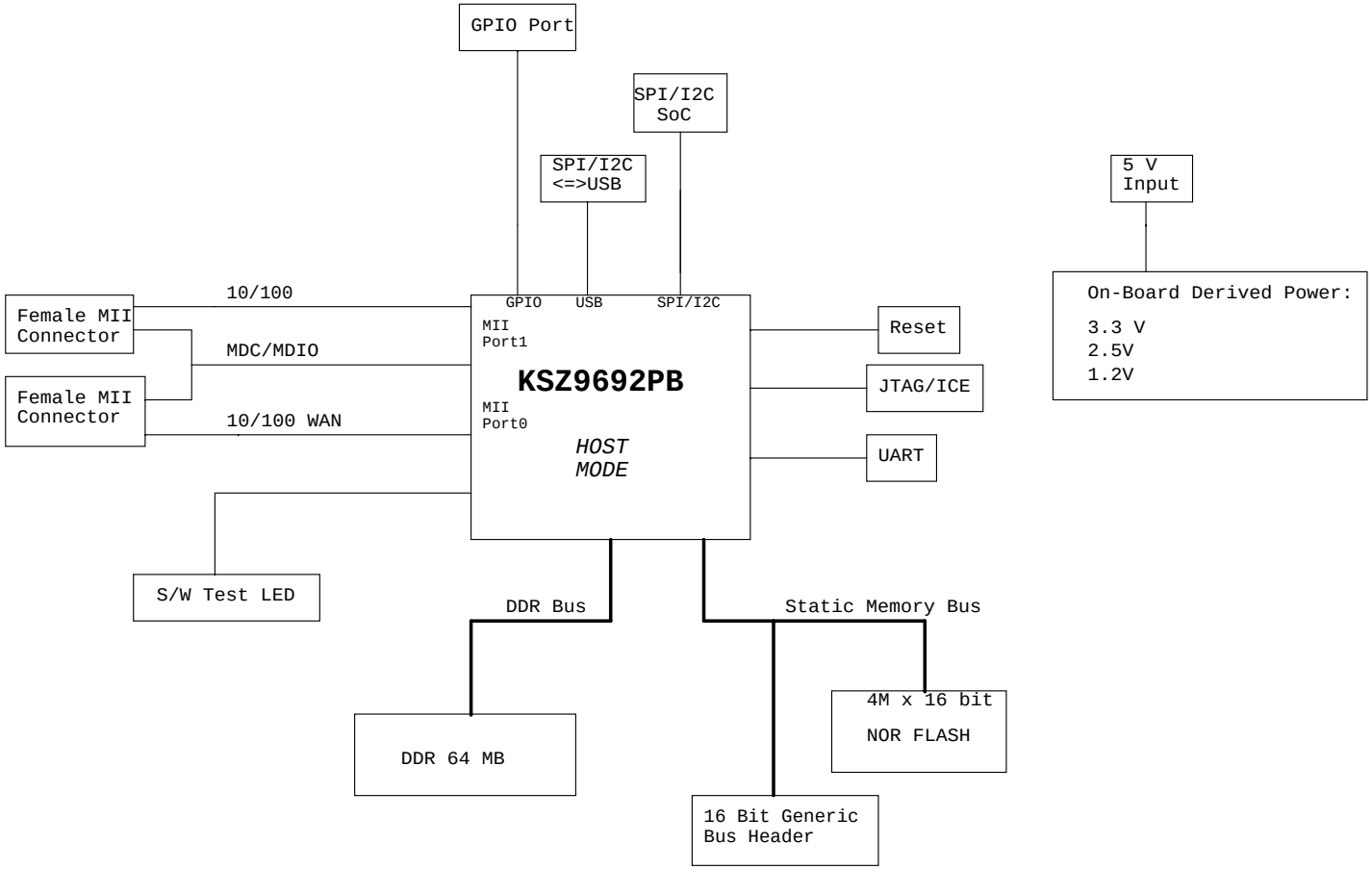
SoC 2 MII Board

REVISION HISTORY

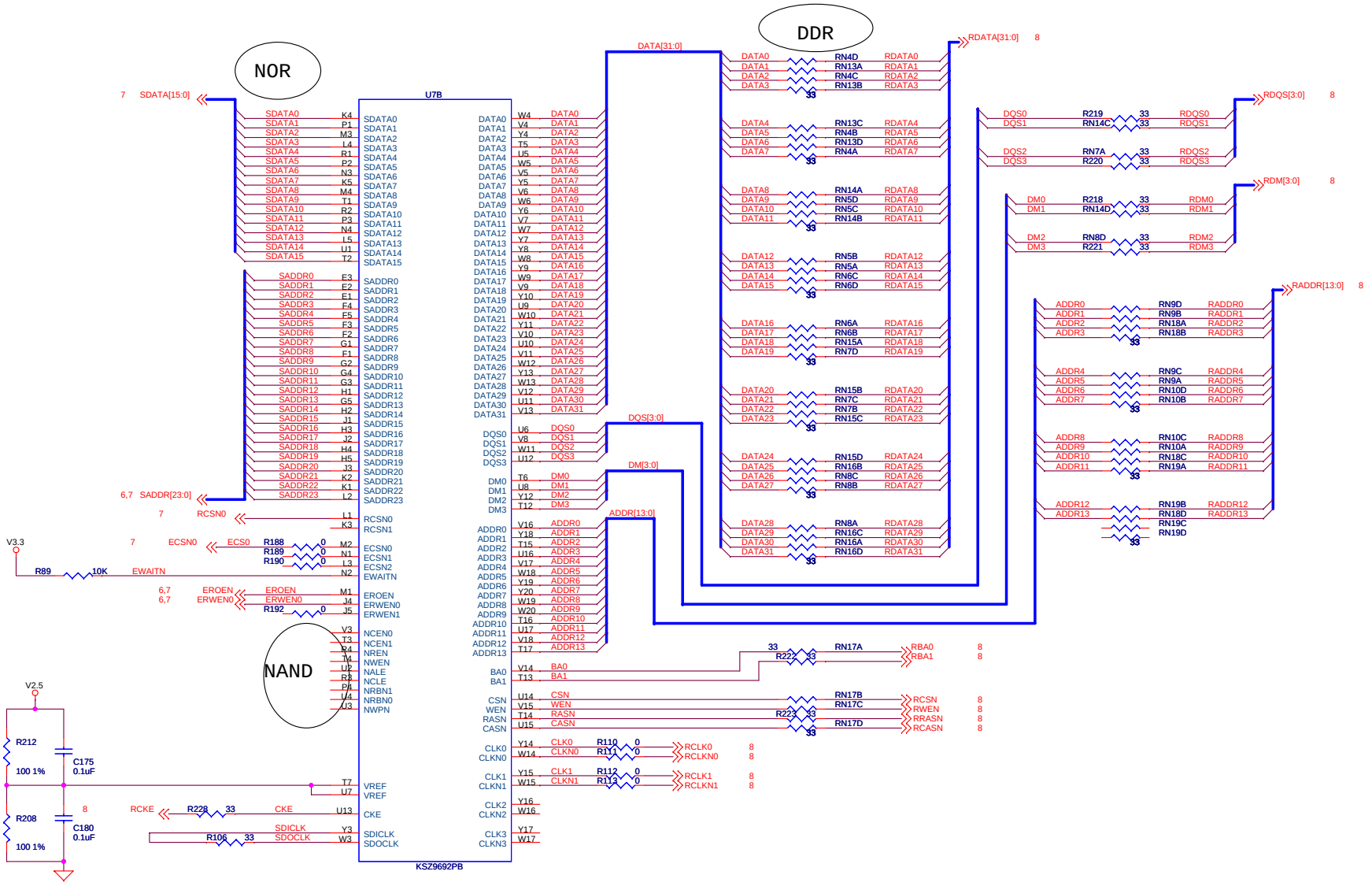
DATE:	DESCRIPTION	REVISION
08/16/10	Initial	1.0
01/31/11	Pull up Pin EROEN make WRSTO active low. Invert the WRSTO before it generates the G_RESETN.	1.1
01/31/11	Change RGMII interface(U20) to MII interface (J5) Change the RN18D, RN19A, RN11 and RN12 connections	2.0
03/05/12	Disconnect the U2_TXD and RTSN in UART port	

MICREL SEMICONDUCTOR		
Title: SoC 2 MII Board		
Size: Custom	Document Number: Revision History	Rev: 1.0
Date: Monday, March 05, 2012	Sheet 1 of 20	

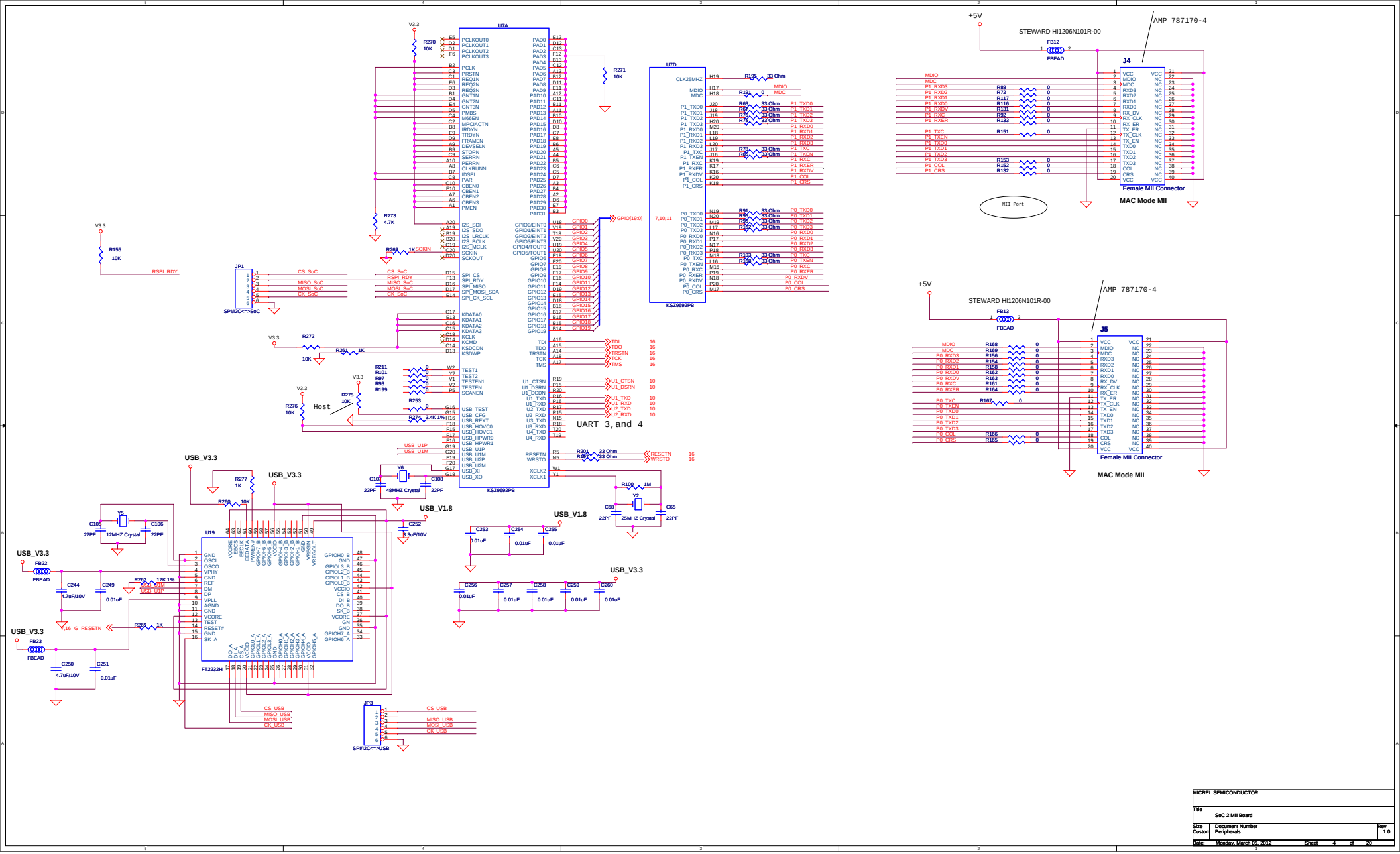


MICREL SEMICONDUCTOR		
Title: SoC 2 MII Board		
Size: Custom	Document Number: Block Diagram	Rev: 1.0
Date: Monday, March 05, 2012	Sheet 2 of 20	

Note: Support DDR 32-bit data width.



MICREL SEMICONDUCTOR			
Title: SoC 2 MII Board			
Size: Custom	Document Number: Memory Bus		Rev: 1.0
Date: Monday, March 05, 2012	Sheet 3 of 20		

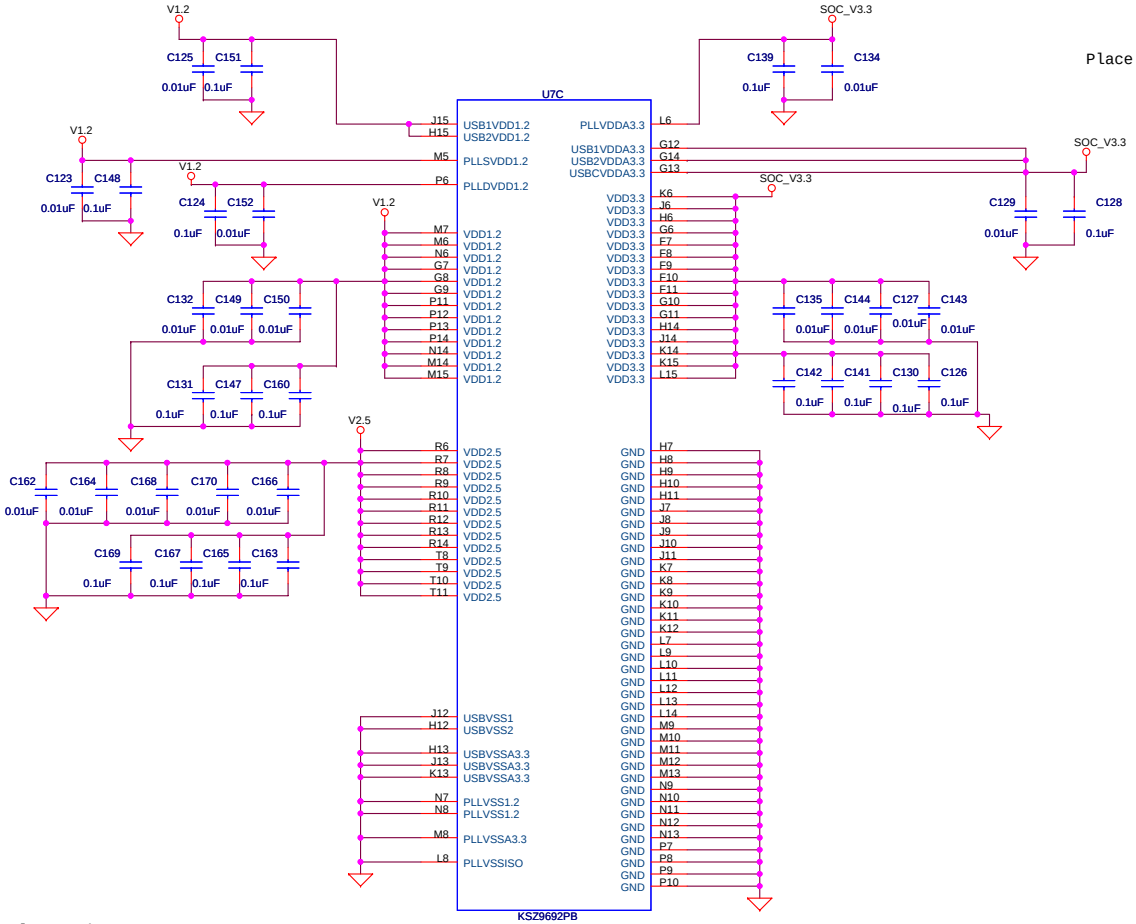

U7A
KSZ9692PB
U7D
KSZ9692PB
STEWARD HI1206N101R-00
AMP 787170-4
J4
Female MII Connector
MAC Mode MII
MII Port
J5
Female MII Connector
MAC Mode MII
UART 3,and 4
Host
U19
FT2232H
JP1
SPMI2C<=>SoC
JP3
SPUI2C<=>USB
MICREL SEMICONDUCTOR
SoC 2 MII Board
Monday, March 05, 2012

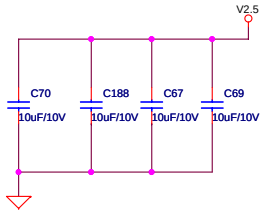
Place V1.2 bypass caps next to BGA power pins

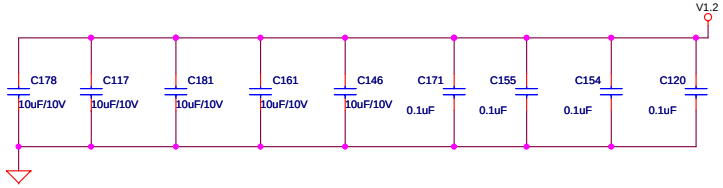
Place SOC_V3.3 bypass caps next to BGA power pins

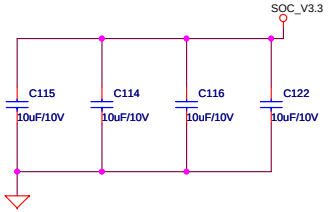
Place V2.5 bypass caps next to BGA power pins

Place caps close to the group of respective voltage pins



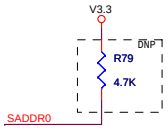






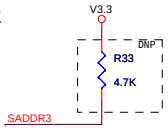
MICREL SEMICONDUCTOR		
Title: SoC 2 MII Board		
Size: Custom	Document Number: KSZ9692PB Power	Rev: 1.0
Date: Monday, March 05, 2012	Sheet 5 of 20	

Not Support NAND Boot



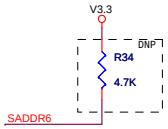
Internal Pull-Down: NAND boot device small page size 512 byte (default)

External Pull-Up: NAND boot device small page size 528 byte



Internal Pull-Down: NAND boot device small block size (default)

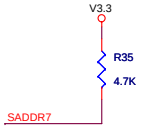
External Pull-Up: NAND boot device large block size



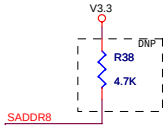
Internal Pull-Down: NAND FLASH device does not support automatic page crossing (default)

External Pull-Up: NAND FLASH device supports automatic page crossing

Not Support NAND Boot

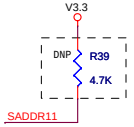


External Pull-Up: 16-bit boot device



Internal Pull-Down: boot from NOR device (default)

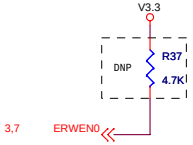
External Pull-Up: boot from NAND device



Port 1 Set to MII

Internal Pull-Down: MII mode (Default)

External Pull-Up: RGMII mode

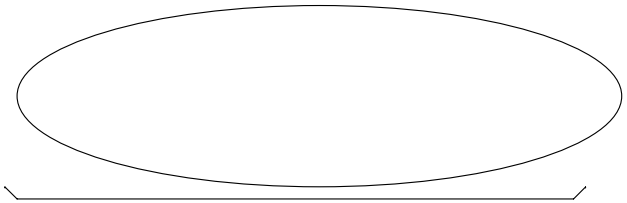


Port 0 Set to MII

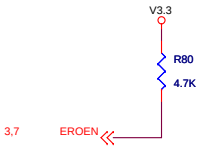
Internal Pull-Down: MII mode (default)

External Pull-Up: RGMII mode

NAND



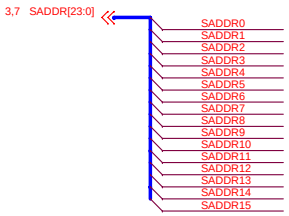
NAND boot device size:128Mbit (default)



For Globe Rest at page 7 (NOR), page 12 (WAN LAN), at Page 11 (Generate RESET signal)

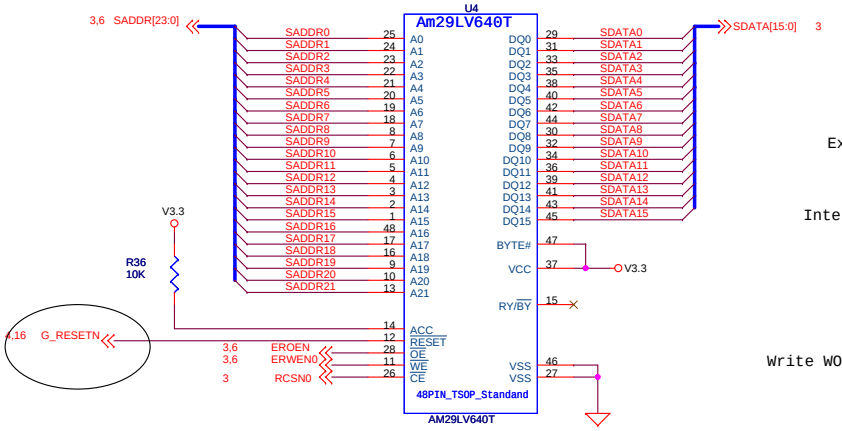
External Pull-Up: WRSTO is active low

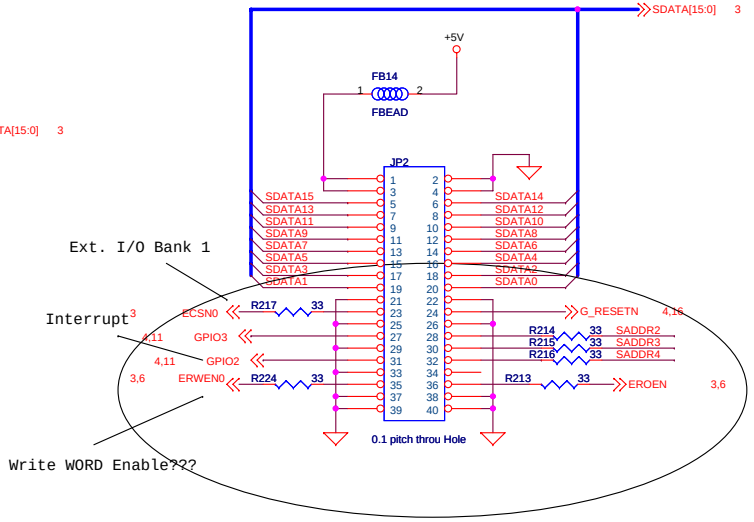
Pull-Down: WRSTO is active High (Default)

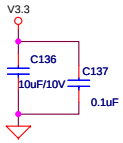


MICREL SEMICONDUCTOR		
Title: SoC 2 MII Board		
Size: Custom	Document Number: Strap In Options	Rev: 1.0
Date: Monday, March 05, 2012	Sheet 6 of 20	

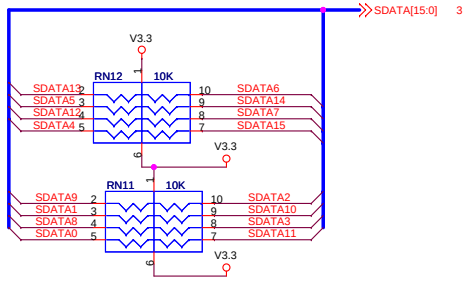
Boot NOR Flash





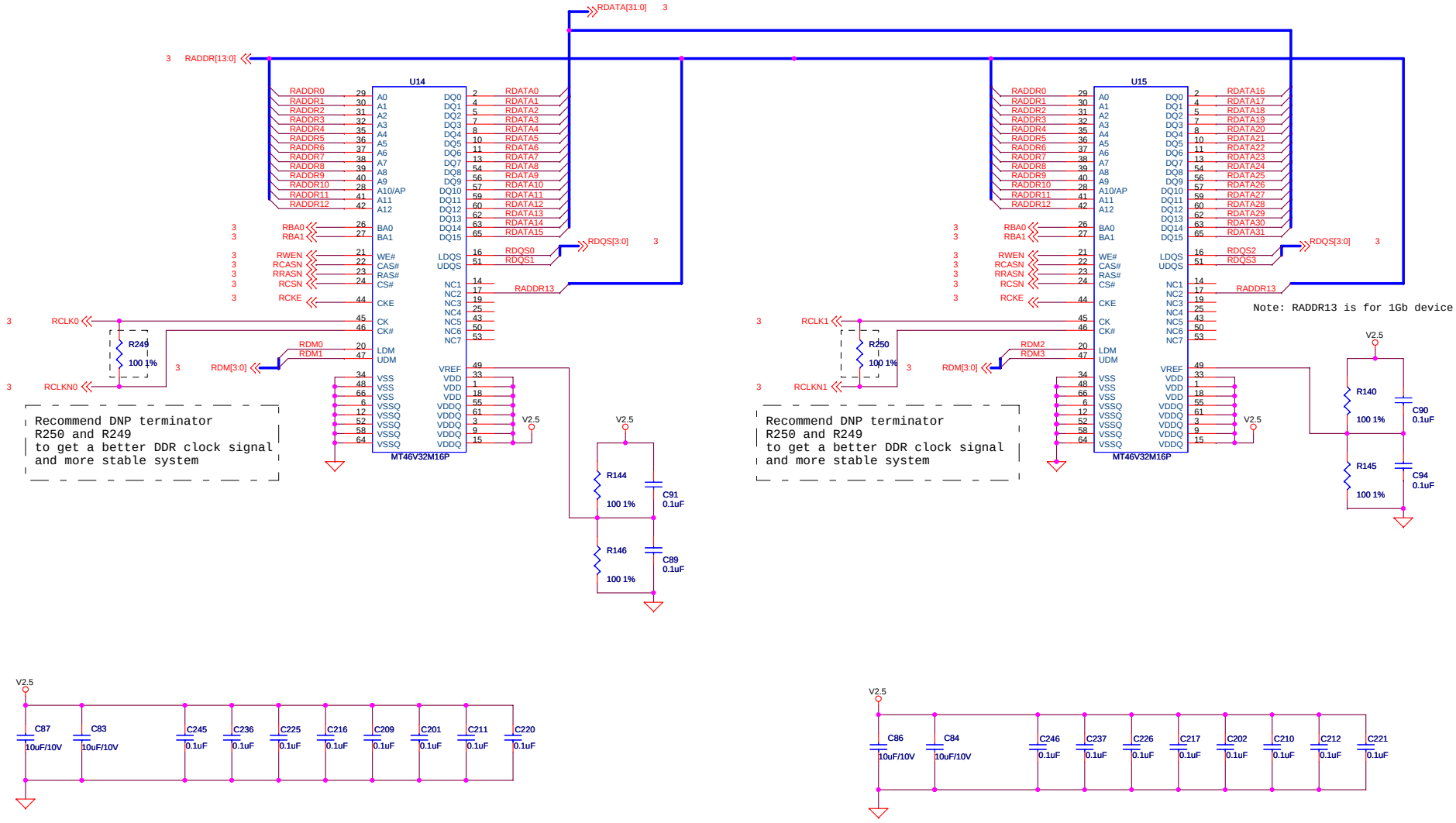


Static memory data bus pullup

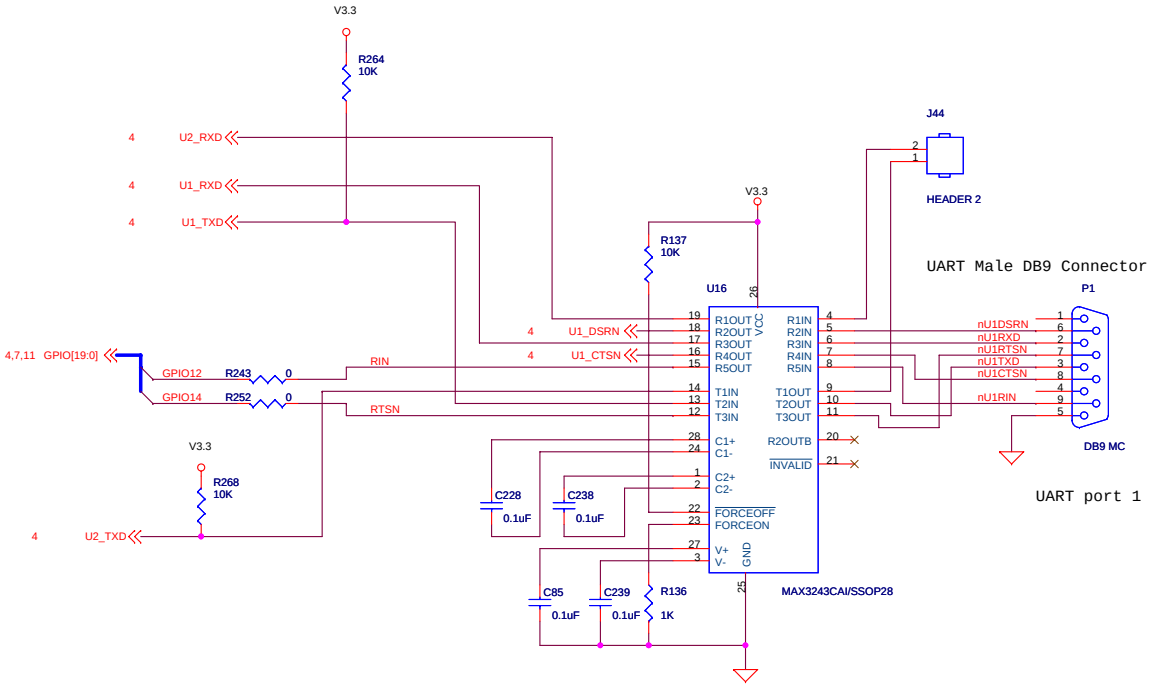


MICREL SEMICONDUCTOR		
Title: SoC 2 MII Board		
Size: Custom	Document Number: NOR Flash	Rev: 1.0
Date: Monday, March 05, 2012	Sheet 7 of 20	

Note: Support DDR 32-bit data width



MICREL SEMICONDUCTOR		
Title: SoC 2 MII Board		
Size: Custom	Document Number: DDR Memory	Rev: 1.0
Date: Monday, March 05, 2012	Sheet 8 of 20	



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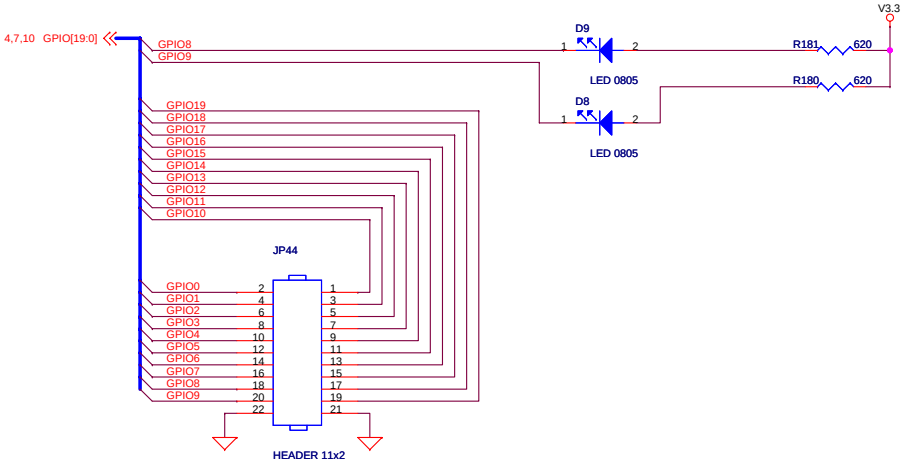
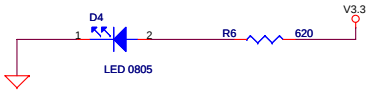
Title: SoC 2 MII Board		
Size: Custom	Document Number: UART	Rev: 1.0
Date: Monday, March 05, 2012	Sheet 10 of 20	

Programmable GPIO LED Indicators

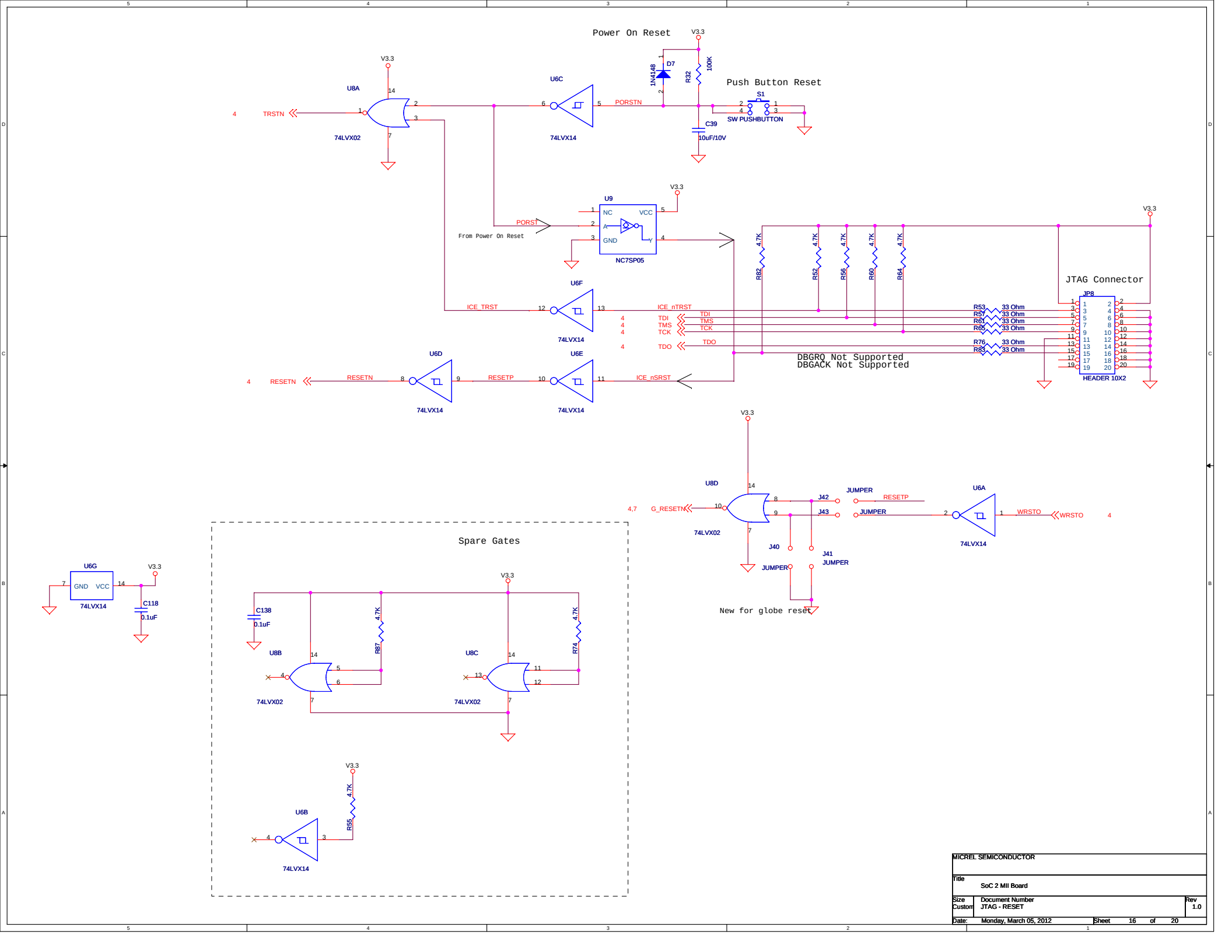


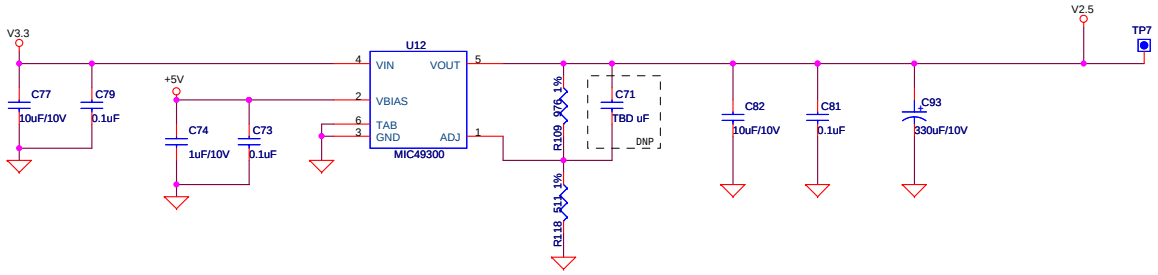
User Programmable GPIO

3.3V POWER LED



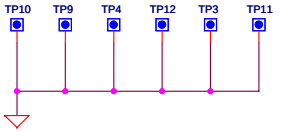
MICREL SEMICONDUCTOR		
Title: SoC 2 MII Board		
Size: Custom	Document Number: GPIO-LED	Rev: 1.0
Date: Monday, March 05, 2012	Sheet 11 of 20	


Power On Reset
Push Button Reset
SW PUSHBUTTON
From Power On Reset
JTAG Connector
HEADER 10X2
DBGRQ Not Supported
DBGACK Not Supported
Spare Gates
New for globe reset
MICREL SEMICONDUCTOR
SoC 2 MII Board
JTAG - RESET
Monday, March 05, 2012

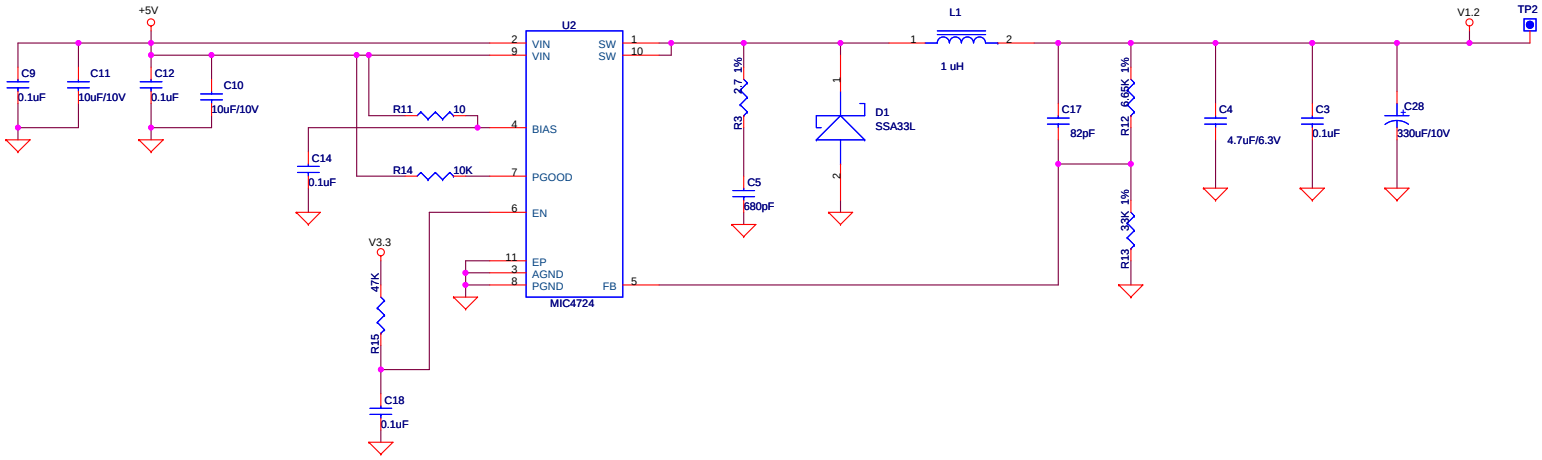


Note: V2.5 must be adjusted to 2.6V for Micron DDR device MT46V32M16-5B. See Micron Electrical Specification.
For DDR devices that require 2.5V, install 1K in R109, 562 ohm in R118

Ground Test Points

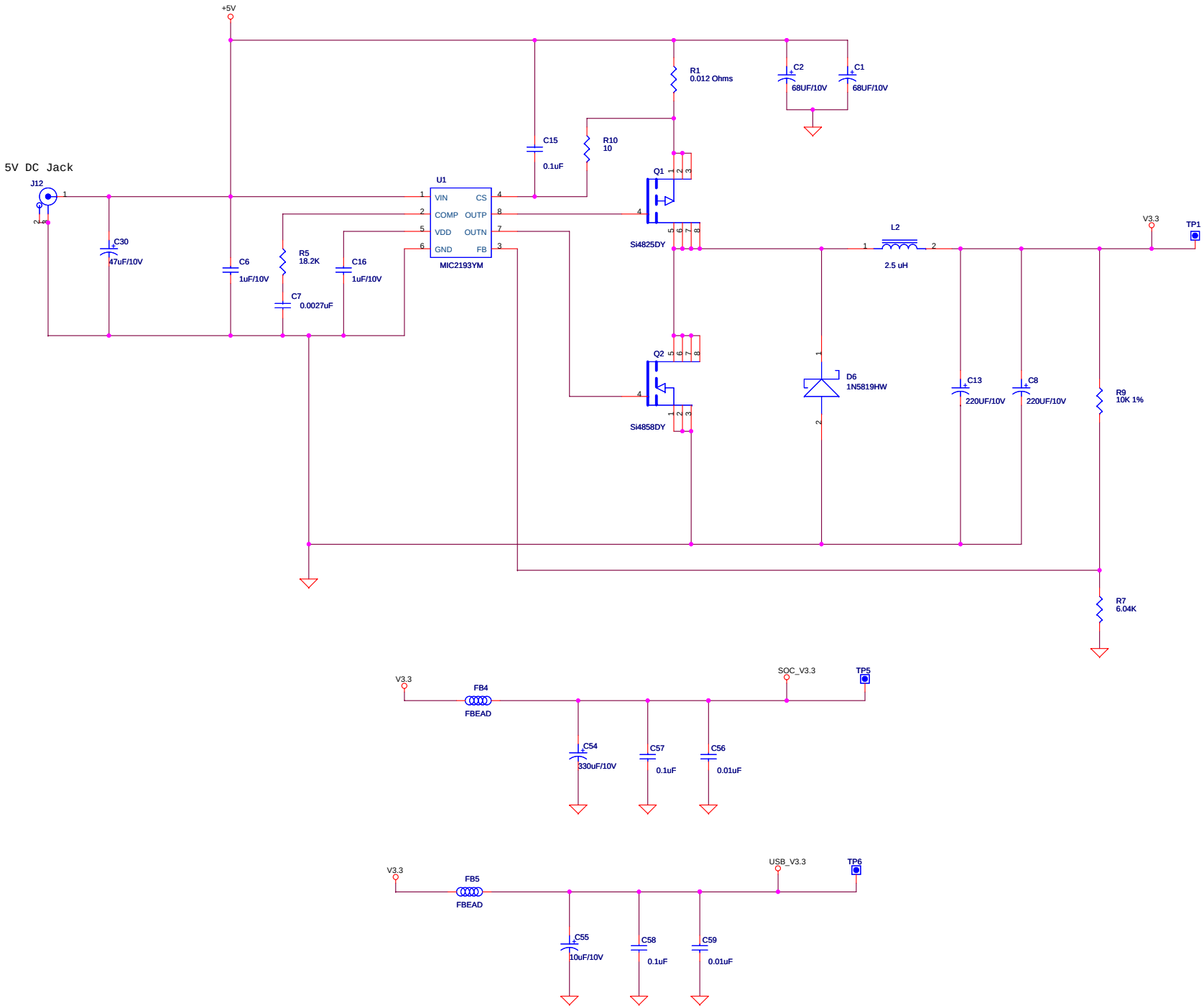


MICREL SEMICONDUCTOR		
Title: SoC 2 MII Board		
Size: Custom	Document Number: DDR Power	Rev: 1.0
Date: Monday, March 05, 2012	Sheet 17 of 20	



Note: RC added to EN control to enforce power sequencing

MICREL SEMICONDUCTOR		
Title: SoC 2 MII Board		
Size: Custom	Document Number: 1.2V Power	Rev: 1.0
Date: Monday, March 05, 2012	Sheet 18 of 20	



MICREL SEMICONDUCTOR		
Title: SoC 2 MII Board		
Size: Custom	Document Number: 3.3V Power	Rev: 1.0
Date: Monday, March 05, 2012	Sheet 19 of 20	