**Subject**: PCB Layout Guidelines for KSZ9692PB Evaluation Board Rev2
**Document Revision**: 2
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The KSZ9692PB is a high performance SoC that integrates many high speed interfaces. A successful board design requires very careful PCB component placement and routing. This document provides general guidelines for PCB layout.

**PCB Layer Stack-up:**
For controlled signal impedance, six layer PCB is recommended with following stack-up:

Layer 1 – Top component and Signal
Layer 2 - GND
Layer 3 - Signal
Layer 4 - Signal
Layer 5 - Power
Layer 6 – Bottom component and Signal

Signal impedance specification is 50 ohm for single-ended clocks & signals and 100 ohm for differential clocks & signals.

**DDR Interface**
DDR interface with its requirements of small setup and hold times, clean power and reference voltages, tight trace matching and I/O (SSTL-2) signaling presents the board designer with great challenge. It is recommended the DDR layout to be supervised by a senior design engineer with prior embedded DDR layout experience.

**DDR Placement Checklist**
- Place series termination resistor networks and resistors near KSZ9692PB
- Place differential clock terminations near DDR device clock input pins
- Place feedback clock series termination resistor near SDOCLK pin of KSZ9692PB
- Place DDR devices near KSZ9692PB to reduces signal traces

**DDR Signals Grouping**
The DDR Memory controller consists of 72 signals. These signals can be divided into the following signal groups for the purpose of this design guide:

- Clocks
- Data
- Address/Command
- Control
- Feedback clock
- Power

| Group | Signal Name | Description |
|---|---|---|
| Clocks | CLK[3:0] | DDR differential clock |
| | CLKN[3:0] | DDR differential clock (complement) |
| Data | DATA[31:0] | 32 bit data bus |
| | DQS[3:0] | Data strobe signals |
| | DM[3:0] | Data Mask Signals |
| Address/Command | ADDR[13:0] | 14 bit address |
| | BA[1:0] | Bank Address |
| | RASN | Row address command |
| | CASN | Column address command |
| | WEN | Write Enable |
| Control | CSN | Chip Select |
| | CKE | Clock Enable |
| Feedback Clock | SDOCLK | PLL De-skew output |
| | SDICLK | PLL De-skew input |
| Power | VREF | Voltage reference for differential receivers |
| | 2.5V | DDR Power Supply |

**DDR Routing Guideline**

Groups are to be routed in the order of priority:

Data
Data group is 2x clock rate and most critical. Route this group first. Match trace length on every line within 20 mils.
Do not share series termination resistor networks with non-data group.
Route this group over GND plane for lowest return current and improved signal integrity.
Route this group as short as possible
Route this group on same layer
Route this group 20 mils distance away from other DDR groups
Route this group 20 mils distance away from non DDR groups

Address and Commands and Controls
Route this group as split-T to DDR devices
Route this group 20 mils distance away from non DDR groups
Match trace length for every line within 20 mils.

Clocks
Route differential clocks CLK[3:0]/ CLKN[3:0] to exact matching length
Route this group over GND plane for lowest return current and improved signal integrity.
Route this group 20 mils distance away from other DDR groups
Route this group 20 mils distance away from non DDR groups
Serpentine isolation spacing minimum 20 mils
Route differential clocks to same length of Address, Command and Control signals

Feedback Clock
Route SDOCLK to SDICLK to same length as differential clocks CLK[3:0]/ CLKN[3:0].

**Power Supply Bypass Capacitor Requirement**

2.5V Bypass
Place minimum five 0.1uF X5R caps directly on KSZ9692PB 2.5V BGA pins
Place minimum five 0.01uF X5R caps directly on KSZ9692PB 2.5V BGA pins
Place minimum four 10uF X5R ceramic caps near KSZ9692PB package

1.2V Bypass
Place minimum six 0.1uF X5R caps directly on KSZ9692PB 1.2V BGA pins
Place minimum six 0.01uF X5R caps directly on KSZ9692PB 1.2V BGA pins
Place minimum four 10uF X5R ceramic cap near KSZ9692PB package

3.3V Bypass
Place minimum six 0.1uF X5R caps directly on KSZ9692PB 3.3V BGA pins
Place minimum six 0.01uF X5R caps directly on KSZ9692PB 3.3V BGA pins
Place minimum four 10uF X5R ceramic cap near KSZ9692PB package

VREF Bypass

Place VREF resistor dividers and bypass caps next to KSZ9692PB BGA VREF pins T7 & U7. Use power trace or power plane shape to make the connection.

DDR Memory Device Bypass
Place minimum six 0.1uF X5R caps near each DDR device 2.5V power pins
Place minimum two 10uF X5R ceramic cap near each DDR device

DDR Memory Device VREF Bypass
Place VREF resistor dividers and bypass caps next to each DDR device VREF pin. Use power trace to make the connection.

**USB Interface**
Route data pairs differentially to port1 and port2.
Route data pairs over GND plane for lowest return current and improved signal integrity
Route data pairs directly from KSZ9692PB BGA pins to USB connector on same layer (no layer jumping)
Route data pairs 25 mils away from other signals.

**GMAC Port0 (WAN port)**
Place P0_TxD[3:0], P0_TxC, P0_TxCTL series termination resistors near KSZ9692PB BGA pins
Route P0_TxD[3:0], P0_TxC, P0_TxCTL of same length from KSZ9692PB BGA pins to Gig PHY
Keep distance of 20 mils from this group to other signals
Route this group over solid GND plane
Route on same layer

Place P0_RxD[3:0], P0_RxC, P0_RxCTL series termination resistors near Gig PHY.
Route P0_RxD[3:0], P0_RxC, P0_RxCTL of same length from Gig PHY to KSZ9692PB BGA pins
Keep distance of 20 mils from this group to other signals
Route this group over solid GND plane
Route on same layer

Routing of transmit and receive groups are independent of each other.

Note: For designs that implement Micrel KSZ9021RL as Gig PHY, thermal consideration must be given to its heat dissipation. KSZ9021RL integrates a LDO controller to drive an external power MOSFET to supply its 1.2V core. The MOSFET can generate as much as 1.2 watt. To dissipate this amount of heat, it is necessary to connect drain of MOSFET to a copper mounting pad as large as possible. For a detailed discussion of MOSFET heat handling strategy, Fairchild Semiconductor application note AN1028 is recommended.

**GMAC Port1 (LAN port)**
Place P1_TxD[3:0], P1_TxC, P1_TxCTL series termination resistors near KSZ9692PB BGA pins

Route P1_TxD[3:0], P1_TxC, P1_TxCTL of same length from KSZ9692PB BGA pins to Gig PHY
Keep distance of 20 mils from this group to other signals
Route this group over solid GND plane
Route on same layer

Place P1_RxD[3:0], P1_RxC, P1_RxCTL series termination resistors near Gig PHY.
Route P1_RxD[3:0], P1_RxC, P1_RxCTL of same length from Gig PHY to KSZ9692PB BGA pins
Keep distance of 20 mils from this group to other signals
Route this group over solid GND plane
Route on same layer

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**PCI**
Place PCLKOUT[3:0]  series terminations near KSZ9692PB BGA pins
Place PCI pull-up resistors at end of bussed signals.
Route PCI clocks PCLKOUT[3:0] of same length.
Place bulk and bypass capacitors near 5V and 3.3V power pins of PCI and MiniPCI connectors pins.

**I2S**
Apply standard TTL routing guidelines for signals.

**SPI/I2C**
Apply standard TTL routing guidelines for signals.

**SD/SDIO**
Place SD Pull-up resistors near SD/SDIO card.
Apply standard TTL routing guidelines for signals.

**Static Memory**
Apply standard TTL routing guidelines for NOR Flash and NAND Flash.
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