RENESAS

Renesas Microcomputer

32-bit Microcontrollers

V850

See your creations come to life
through the unsurpassed
performance of V850 microcontrollers.

Renesas Electronics
www.renesas.com

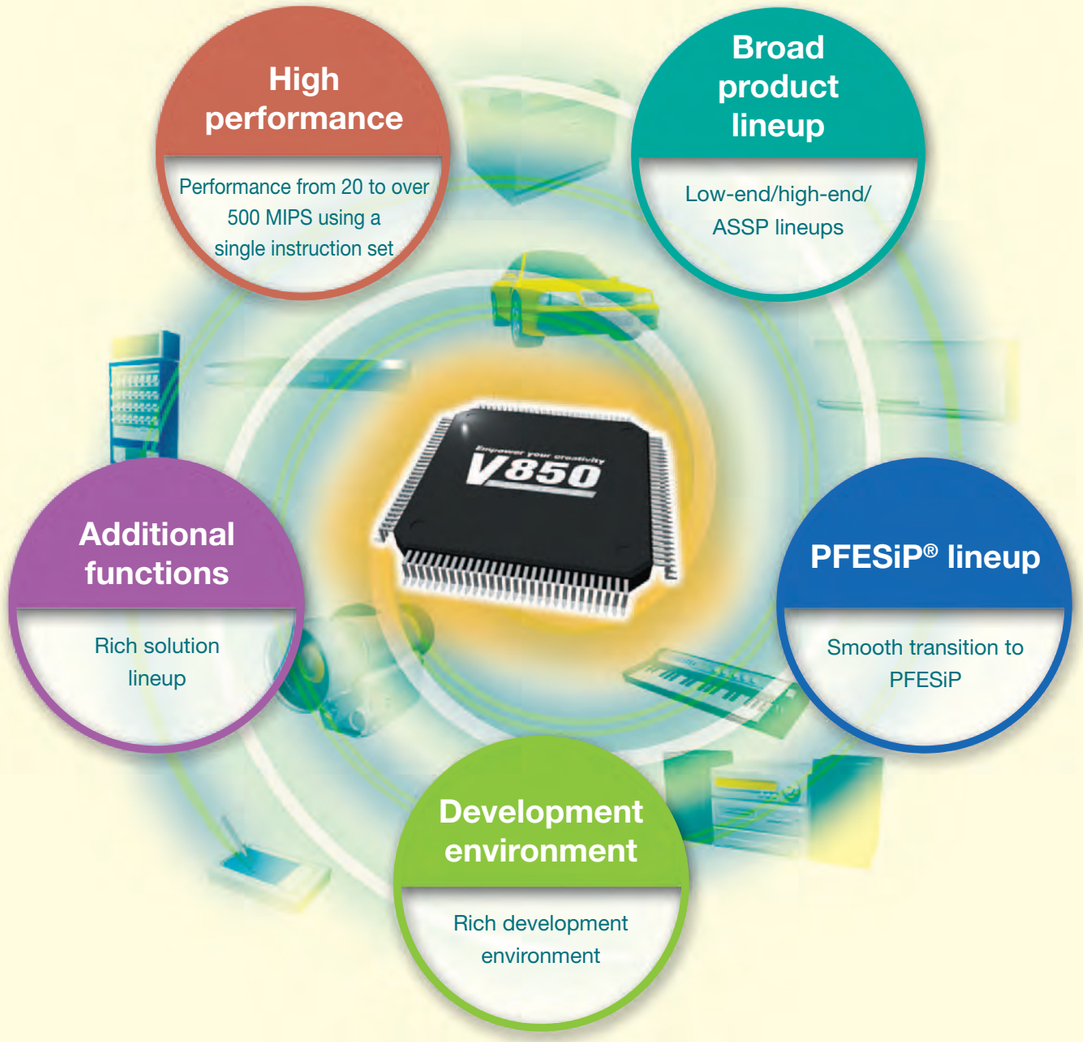
2011.09

Empower your creativity

V850

Embedded Controller

The V850 high-performance microcontrollers answer many different application system needs. They realize extremely low power consumption and low noise while offering high performance and a wide array of functions.
The broad V850 product lineup provides the best solution for your next-generation system.



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V850 Product Lineup

An expanding lineup of continuously evolving V850 microcontrollers

High-end lineup

V850E2M CPU
200 MHz @ 512 MIPS

V850E2 CPU
200 MHz @ 432 MIPS

V850E1 CPU
150 MHz @ 323 MIPS

High performance: On-chip MEMC/DMAC

- Frequency: 33 to 200 MHz
- Parallel pipeline processing (V850E2, V850E2M)
- Memory size: ROM: ROMless to 2048 KB
  RAM: 4 to 200 KB
- Package: 100 to 304 pins (QFP & FBGA)

ASSP lineup

Inverter control
DVC control
Car infotainment control
Network support
Dashboard control

- Frequency: 13 to 160 MHz
- Memory size: ROM: ROMless to 2048 KB
  RAM: 4 to 192 KB
- Package: 64 to 256 pins (QFP & FBGA)

Low-end lineup

V850ES CPU
50 MHz @ 103 MIPS

V850 CPU
20 MHz @ 23 MIPS

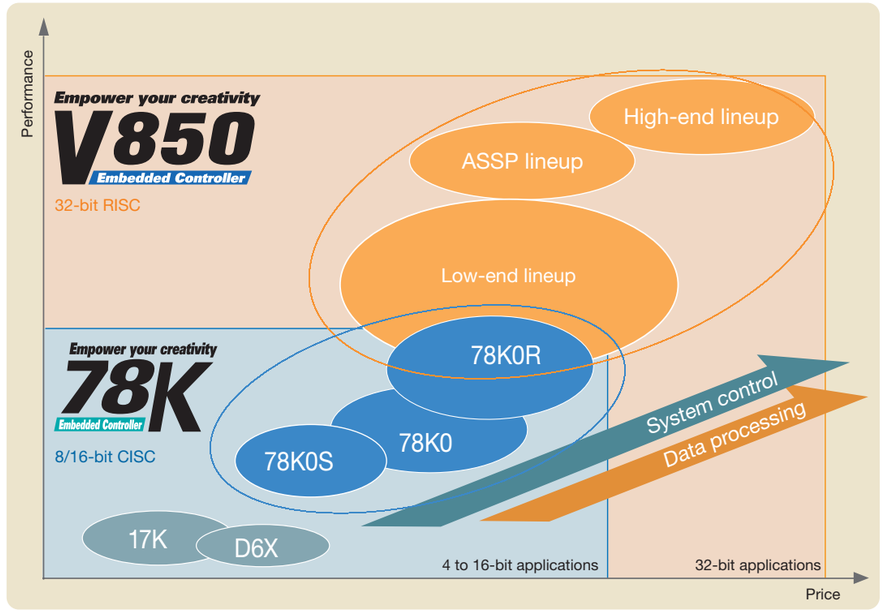
High cost-performance

- Frequency: 16 to 50 MHz
- Memory size: ROM: ROMless to 1024 KB
  RAM: 4 to 124 KB
- Package: 40 to 144 pins (QFN & QFP & FBGA)

Upward compatible instruction sets

Standard lineup | Field-specific lineup

Renesas Electronics 78K and V850 Microcontroller Roadmap



Application Examples

The V850 microcontrollers are suitable for many application fields and raise the commercial value of your system.

Automotive	Engines, car infotainment, dashboards, power steering, ABS
Audio	Portable audio, component stereo systems, home theater
Portable devices	PDAs, IC recorders
Cameras	DVC, DSC, SLR cameras
Computer peripherals	LBP, PPC, MFP, inkjet printers, scanners, fax machines
Home appliances	Air conditioners, refrigerators, washing machines, microwave ovens
Industrial equipment	Industrial motors, control equipment, vending machines, power meters
Video and recording equipment	Blu-ray players, Blu-ray recorders, industrial cameras
Other	Electronic instruments, electric bidets, toys, learning devices, remote controllers, etc.

5 Keys of V850

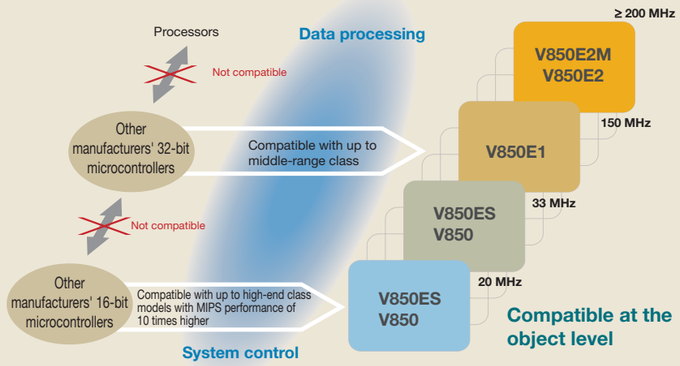
5 reasons why you should choose a V850 microcontroller

High performance

Performance of 20 to over 500 MIPS using a single instruction set

High performance

- Compared to 8-bit or 16-bit microcontrollers, V850 microcontrollers offer a MIPS performance that is at least 10 times higher for the same frequency, and 2 to 3 times higher at the actual application level (based on Renesas Electronics evaluation).
- V850 microcontrollers can operate at frequencies 1/2 to 1/3 those of 8-bit or 16-bit microcontrollers, lowering the system power consumption.
- The V850 CPU, V850ES CPU, V850E1 CPU, V850E2 CPU, and V850E2M CPU are compatible at the object level.

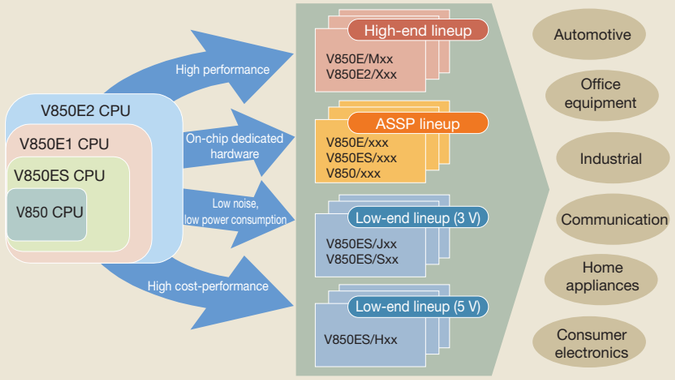


Product lineup

Low-end/High-end/ASSP lineups

Product lineup

- Low-end lineup: General-purpose microcontrollers for the 16- to 32-bit market designed for high cost-performance
- High-end lineup: Designed for high performance and include an on-chip memory controller and DMAC
- ASSP lineup: Field-specific product lineup, that includes on-chip dedicated hardware

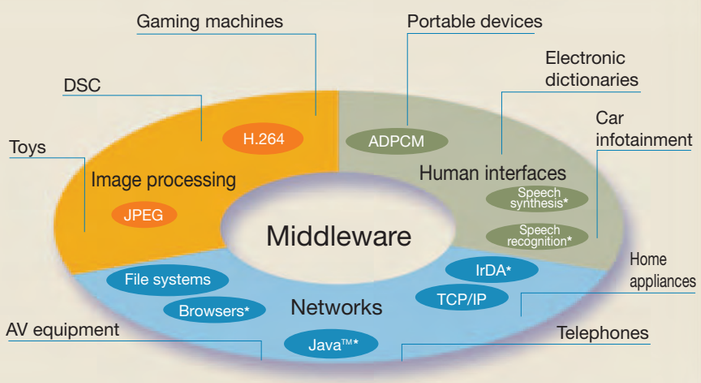


Additional functions

Rich solution lineup

Additional functions

- V850 microcontrollers add value to your system because you can add functions to an existing system by using middleware
- By using V850 and middleware, you no longer need a lot of peripheral ICs which reduces your development time and system costs



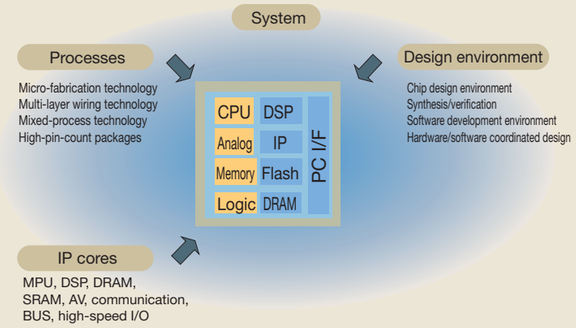
* Middleware from a partner company is used.

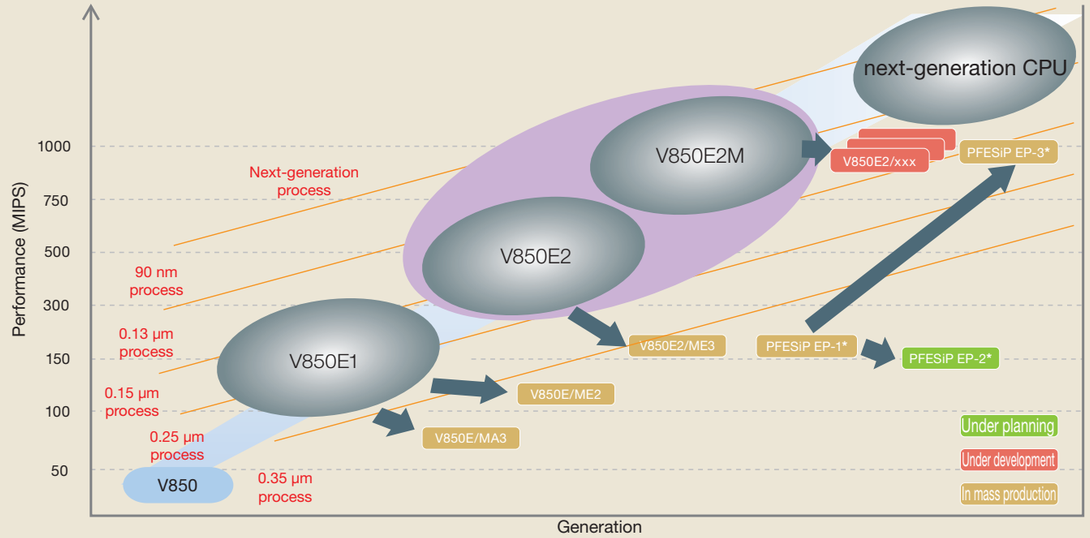
PFESiP® Roadmap

Smooth transition to PFESiPs

System LSI

- V850 microcontrollers are also being actively used as ASIC CPU cores, helping you transition smoothly to PFESiP development.
- The following elements essential for PFESiPs are provided when you need them:
  <1> Leading-edge process technology
  <2> High-performance CPU cores
  <3> Rich lineup of IP cores
  <4> Top-down design environment
  <5> Flexible application design





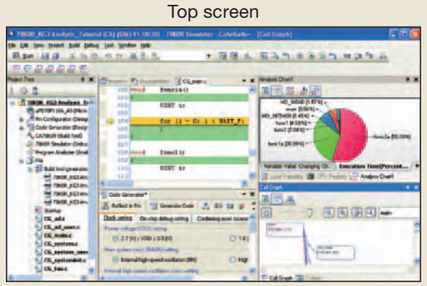
* PFESiP EP-1, PFESiP EP-2, and PFESiP EP-3 are custom microcontrollers that integrate a V850 microcontroller and logic LSI.

Development environment

Rich development environment lineup

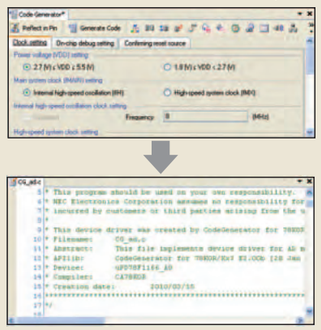
Development environment

Top screen



Code generated easily

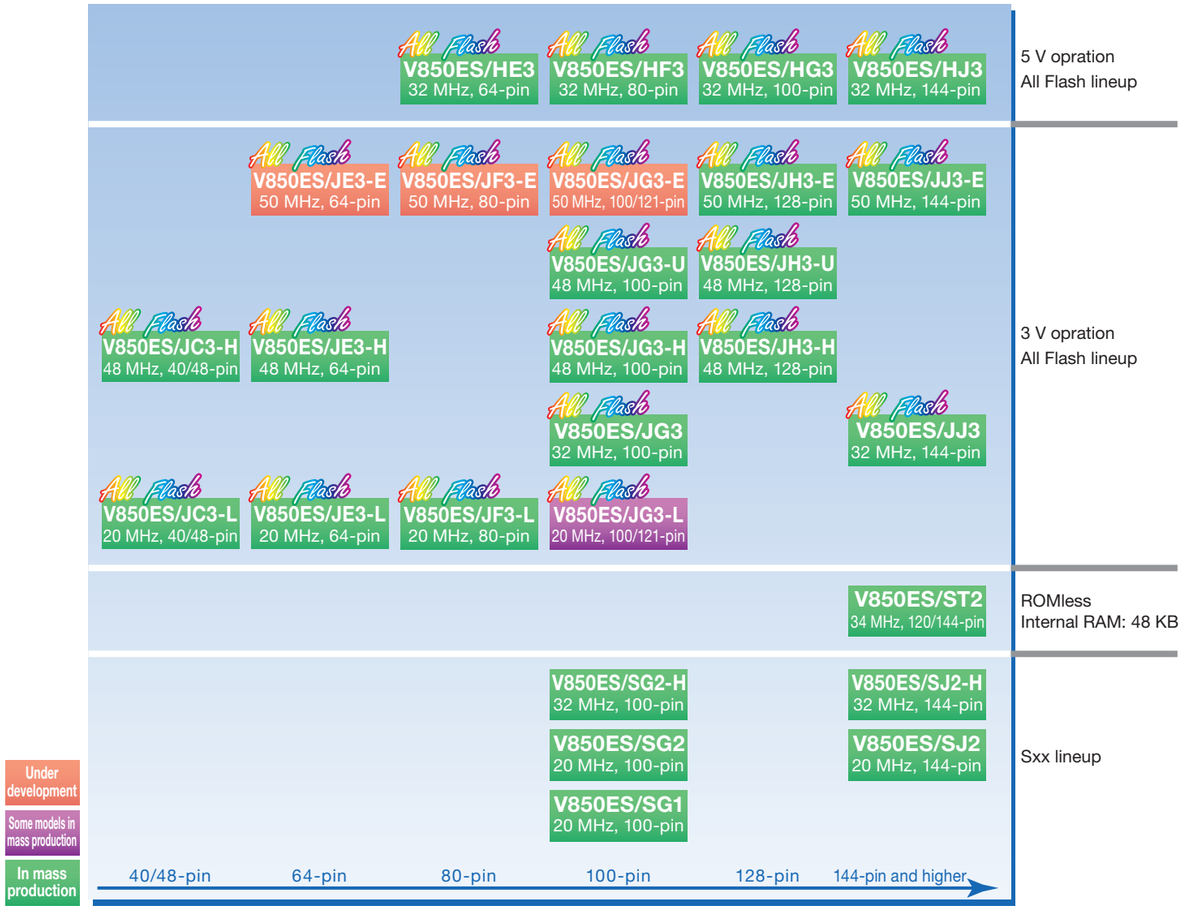
CubeSuite automatically generates source code (a device driver program) to control the microcontroller peripherals (such as the timers, UART, and A/D converter).



- Renesas Electronics has released the CubeSuite+ integrated development platform, an easy-to-use and convenient development environment. CubeSuite+ can be used to compile and debug programs, manage pin layouts, generate code for microcontroller peripherals, and execute high-speed building.
- Use CubeSuite+ in combination with an on-chip debugging emulator with a flash programming function (such as the E1) to create an environment for fast system development.

Product Lineup

Low-End Lineup



Remark See Product Specification List (pp. 46 to 55) for details about the product specifications.

Features

V850ES/HE3, HF3, HG3, HJ3

- All Flash products
- 69 MIPS @ 32 MHz, 66 MIPS @ 32 MHz (μPD70F3757 only), 3.7 to 5.5 V operation (A/D converter: 4.0 to 5.5 V)
- ROM/RAM: 128 KB/8 KB to 512 KB/32 KB
- On-chip multi-channel A/D converter, POC, LVI, DMAC, on-chip debugger, 3-phase inverter control, and SSCG*
- 64-pin LQFP (HE3), 80-pin LQFP (HF3), 100-pin LQFP (HG3), 144-pin LQFP (HJ3)

* Spread spectrum frequency synthesizer clock generator

V850ES/JE3-E, JF3-E, JG3-E, JH3-E, JJ3-E

- All Flash products
- 103 MIPS @ 50 MHz, 2.85 to 3.6 V operation (A/D converter, USB controller: 3.0 to 3.6 V)
- ROM/RAM: 64 KB/32 KB* to 512 KB/124 KB**
- USB controller: USB 2.0 function (full-speed) × 1 ch, Ethernet controller × 1 ch
- 64-pin WQFN (JE3-E), 80-pin LQFP (JF3-E), 100-pin LQFP/121-pin FBGA (JG3-E), 128-pin LQFP (JH3-E), 144-pin LQFP (JJ3-E)

* Includes 16 KB of data-only RAM.
** Includes 64 KB of data-only RAM.

V850ES/JC3-H, JE3-H, JG3-H, JH3-H, JG3-U, JH3-U

- All Flash products
- 98 MIPS @ 48 MHz, 2.85 to 3.6 V operation (A/D converter, USB controller: 3.0 to 3.6 V)
- ROM/RAM: 16 KB/8 KB to 512 KB/56 KB*
- USB controller: USB 2.0 function (full-speed) × 1 ch, USB 2.0 host (full-speed) × 1 ch (JG3-U, JH3-U only)
- 40-pin WQFN (JC3-H), 48-pin LQFP/WQFN (JC3-H), 64-pin LQFP/WQFN (JE3-H), 64-pin FBGA (μPD70F3824), 100-pin LQFP (JG3-H, JG3-U), 128-pin LQFP (JH3-H, JH3-U)

* Includes 8 KB of data-only RAM.

V850ES/JG3, JJ3

- All Flash products
- 69 MIPS @ 32 MHz, 2.85 to 3.6 V operation (A/D converter: 3.0 to 3.6 V)
- ROM/RAM: 384 KB/32 KB, 512 KB/40 KB, 768 KB/60 KB, 1024 KB/60 KB
- On-chip multi-channel serial interface, LVI, clock monitor, DMAC, and on-chip debugger
- 5 V withstand voltage ports incorporated, and 5 V output is possible by setting N-ch open-drain output
- 100-pin LQFP (JG3), 144-pin LQFP (JJ3)

V850ES/JC3-L, JE3-L, JF3-L, JG3-L

- All Flash products
- 43 MIPS @ 20 MHz, 2.0 to 3.6 V operation (JG3-L*), 2.2 to 3.6 V operation (JC3-L, JE3-L, JF3-L)
- ROM/RAM: 16 KB/8 KB, 1024 KB/80 KB
- Low power operation 36 mW (3.0 V, 20 MHz)
- Function and pin compatibility with V850ES/Jx3 and can use V850ES/Jx3 development environment
- 5 V withstand voltage ports incorporated, and 5 V output is possible by setting N-ch open-drain output
- 40-pin WQFN (JC3-L), 48-pin LQFP/WQFN (JC3-L), 64-pin LQFP/FBGA/WQFN (JE3-L), 80-pin LQFP (JF3-L), 100-pin LQFP/121-pin FBGA (JG3-L)

* 2.2 V to 3.6 V operation for μPD70F3737 and μPD70F3738

V850ES/ST2

- ROMless product with large-capacity RAM
- 34 MHz, 3.0 to 3.6 V operation
- ROM/RAM: ROMless/48 KB
- 120-pin TQFP/144-pin LQFP

V850ES/SG2-H, SJ2-H

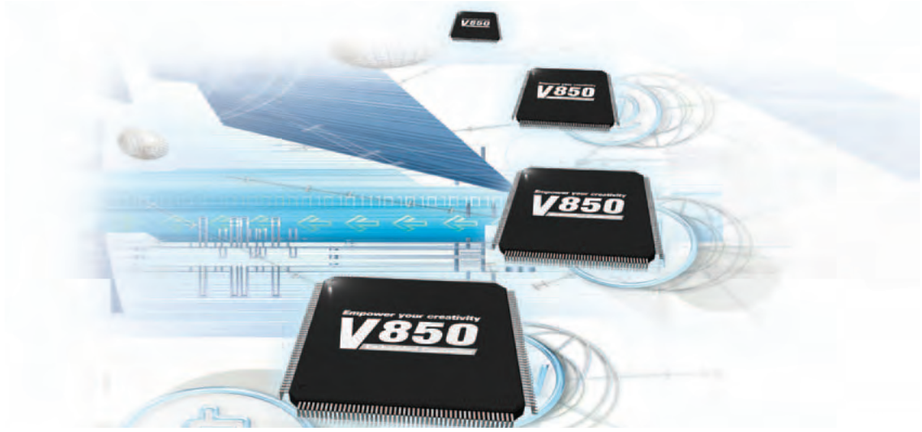
- 66 MIPS @ 32 MHz, 3.0 to 3.6 V operation
- ROM/RAM: 512 KB/40 KB, 640 KB/48 KB
- On-chip multi-channel serial interface, clock monitor, CRC, DMAC, and on-chip debugger
- 5 V withstand voltage ports incorporated, and 5 V output is possible by setting N-ch open-drain output
- 100-pin LQFP (SG2-H), 144-pin LQFP (SJ2-H)

V850ES/SG2, SJ2

- 43 MIPS @ 20 MHz, 2.85 to 3.6 V operation (A/D converter: 3.0 to 3.6 V)
- ROM/RAM: 256 KB/24 KB, 384 KB/32 KB, 512 KB/40 KB, 640 KB/48 KB
- On-chip multi-channel serial interface, LVI, clock monitor, CRC, DMAC, and on-chip debugger
- 5 V withstand voltage ports incorporated, and 5 V output is possible by setting N-ch open-drain output
- 100-pin LQFP (SG2), 100-pin QFP (SG2 (ROM: 256 KB/384 KB versions only)), 144-pin LQFP (SJ2)

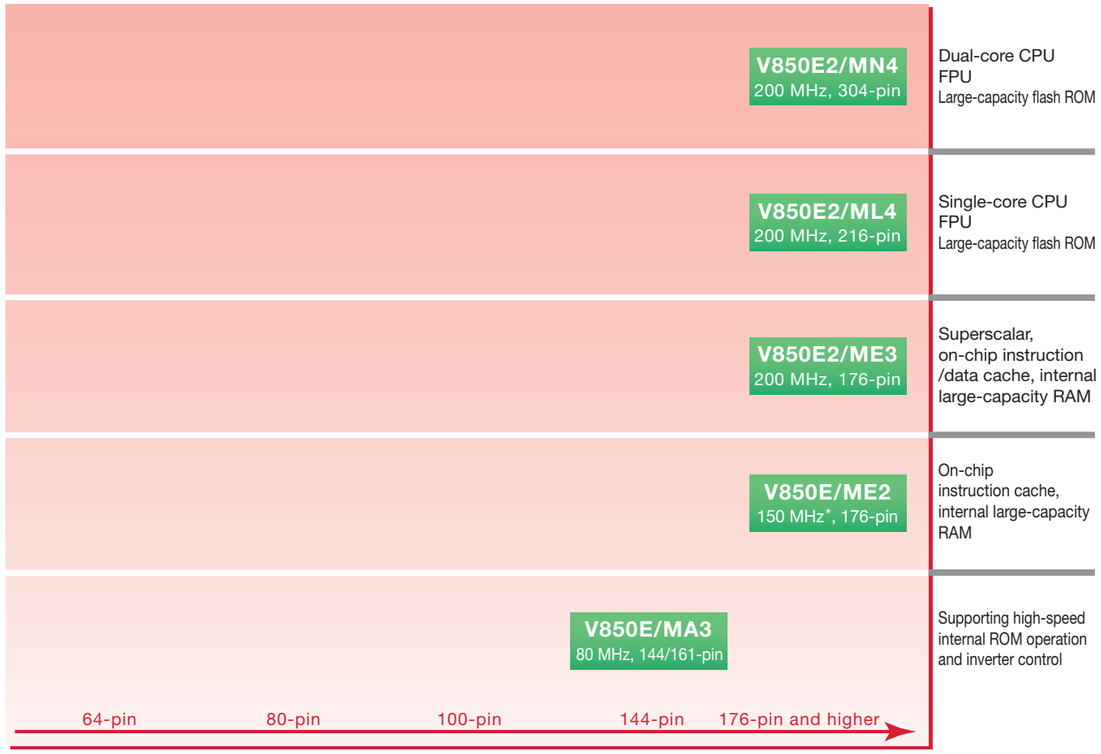
V850ES/SG1

- Part of V850ES/SG2 lineup
- 43 MIPS @ 20 MHz, 2.85 to 3.6 V operation (A/D converter: 3.0 to 3.6 V)
- ROM/RAM: 256 KB/12 KB
- On-chip clock monitor
- 5 V withstand voltage ports incorporated, and 5 V output is possible by setting N-ch open-drain output
- 100-pin LQFP/100-pin QFP



Product Lineup

High-End Lineup



* Products that can operate at 66, 100, 133, and 150 MHz are available.

Remark See Product Specification List (pp. 56 and 57) for details about the product specifications.

Features

V850E2/MN4

- Ultra-high-speed dual-core CPU
- 512 MIPS @ 200 MHz, internal 1.1 V to 1.3 V/ external 3.0 V to 3.6 V operation
- ROM/RAM: 2 MB/128 KB, 1 MB/128 KB, 1 MB/64 KB
- USB (Host, Function), Ethernet controller, DMAC, and CAN
- 304-pin FBGA

V850E2/ML4

- Ultra-high-speed single-core CPU
- 512 MIPS @ 200 MHz, internal 1.1 V to 1.3 V/ external 3.0 V to 3.6 V operation
- ROM/RAM: 768 KB/128 KB,* 1 MB/128 KB*
- USB (Host, Function), Ethernet controller, DMAC, and CAN
- 216-pin LQFP

* Includes 64 KB of expanded internal RAM.

V850E/ME2, V850E2/ME3

- Real-time control with internal large-capacity RAM
- 323 MIPS @ 150 MHz (ME2), 432 MIPS @ 200 MHz (ME3), internal 1.5 V/external 3.3 V operation
- ROM/RAM: ROMless/128 KB + 16 KB (ME2), ROMless/168 KB + 32 KB (ME3)
- On-chip SSCG*, USB (function), SDRAM interface, DMAC, 8 KB instruction cache, 8 KB data cache (ME3 only), and on-chip debugger
- 176-pin LQFP (ME2), 176-pin QFP (ME3)

* Spread spectrum frequency synthesizer clock generator

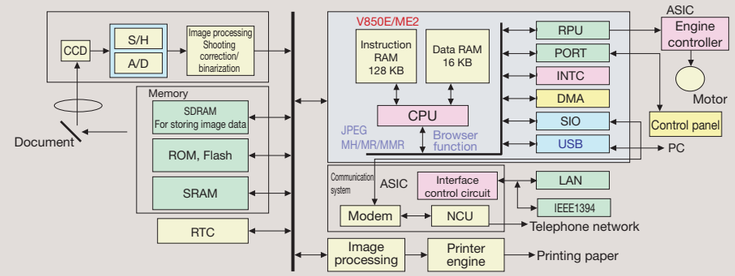
V850E/MA3

- Over 100 MIPS single-chip microcontroller
- 158 MIPS @ 80 MHz, internal 2.5 V/external 3.3 V operation
- ROM/RAM: 256 KB/8 KB, 256 KB/16 KB, 256 KB/32 KB, 512 KB/16 KB, 512 KB/32 KB
- On-chip SDRAM interface, motor control, DMAC, D/A converter, and on-chip debugger
- 144-pin LQFP/161-pin FBGA

Application examples

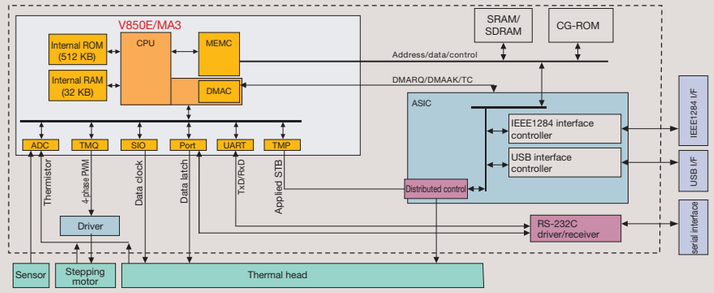
■ MFP (Multifunction printer)

Multi Function Printer
V850E/ME2



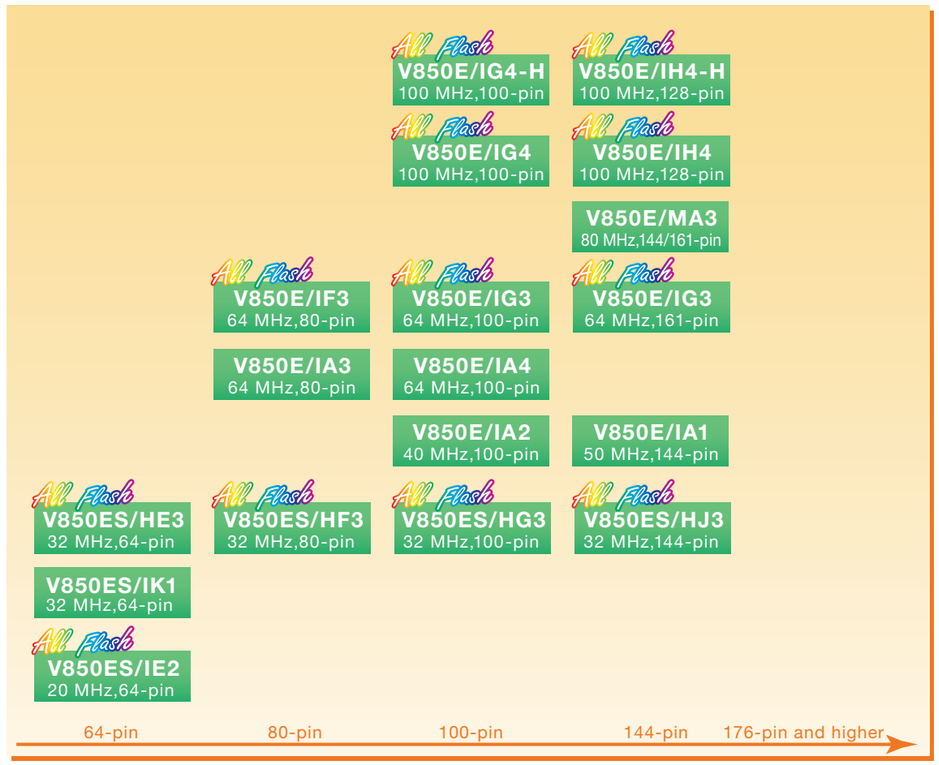
■ Thermal printer

Thermal Printer
V850E/MA3



Product Lineup

ASSP Lineup (Inverter Control, etc.)



Remark See Product Specification List (pp. 58 to 62) for details about the product specifications.

Features

V850E/IG4, IH4, IG4-H, IH4-H

- All Flash products, for inverter control
- 197 MIPS @ 100 MHz, 1.5 V, 5.0 V, or 3.3 V operation (IG4-H and IH4-H only)
- ROM/RAM: 256 KB/24 KB, 384 KB/24 KB, 480 KB/24 KB
- On-chip USB controller (USB 2.0 peripheral (full-speed)) × 1 ch (IG4-H and IH4-H only), PWM timer for 3-phase inverter control × 2 ch (1 ch in the IG4-H), 2-phase encoder timer × 2 ch, six operational amplifiers, 12 comparators, two 12-bit A/D converters, one 10-bit A/D converter, DMAC, on-chip debugger (can be used with MINICUBE® and MINICUBE2), POC, LVI, and clock monitor
- 100-pin LQFP (IG4, IG4-H), 128-pin LQFP (IH4, IH4-H)

V850E/MA3

- For inverter control
- 158 MIPS @ 80 MHz, internal 2.5 V/external 3.3 V operation
- ROM/RAM: 256 KB/8 KB, 256 KB/16 KB, 256 KB/32 KB, 512 KB/16 KB, 512 KB/32 KB
- On-chip SDRAM interface, 3-phase inverter control PWM timer, 2-phase encoder timer, DMAC, D/A converter, and on-chip debugger
- 144-pin LQFP/161-pin FBGA

V850E/IF3, IG3

- All Flash products, for inverter control
- 131 MIPS @ 64 MHz, 3.5 to 5.5 V operation (A/D converter: 4.0 to 5.5 V)
- ROM/RAM: 128 KB/8 KB, 256 KB/12 KB
- On-chip 3-phase inverter control PWM timers (2 ch), 2-phase encoder timers (2 ch) (IF3: 1 ch), four operational amplifiers, eight comparators, two 12-bit A/D converters, one 10-bit A/D converter, DMAC, on-chip debugger (IF3: can be used with MINICUBE2, IG3: can be used with MINICUBE® and MINICUBE2), POC, LVI, clock monitor, and 5 V single power supply
- 80-pin LQFP (IF3), 100-pin LQFP (IG3), 161-pin FBGA (μPD70F3454)

V850E/IA3, IA4

- For inverter control
- 126 MIPS @ 64 MHz, internal 2.5 V/external 5 V operation
- ROM/RAM: 128 KB/6 KB, 256 KB/12 KB
- On-chip 3-phase inverter control PWM timers (2 ch) (IA3: 1 ch), 2-phase encoder timers (2 ch) (IA3: 1 ch), six operational amplifiers (5 in the IA3), six comparators (5 in the IA3), three A/D converters, DMAC, on-chip debugger (can be used with MINICUBE2), and clock monitor
- 80-pin QFP (IA3), 100-pin LQFP/100-pin QFP (IA4)

V850E/IA1, IA2

- For inverter control
- 103 MIPS @ 50 MHz, internal 3.0 to 3.6 V/external 4.5 to 5.5 V operation (IA1), 82 MIPS @ 40 MHz, 4.5 to 5.5 V operation (when using on-chip regulator) (IA2)
- ROM/RAM: 128 KB/6 KB (IA2), 256 KB/10 KB (IA1)
- On-chip 3-phase inverter control PWM timers (2 ch), 2-phase encoder timers (2 ch) (IA2: 1 ch), two A/D converters, and DMAC
- 100-pin LQFP/100-pin QFP (IA2), 144-pin LQFP (IA1)

V850ES/HE3, HF3, HG3, HJ3

- All Flash products
- 69 MIPS @ 32 MHz, 66 MIPS @ 32 MHz (μPD70F3757 only), 3.7 to 5.5 V operation (A/D converter: 4.0 to 5.5 V)
- ROM/RAM: 128 KB/8 KB to 512 KB/32 KB
- On-chip 3-phase inverter control PWM timer, multi-channel A/D converter, POC, LVI, DMAC, on-chip debugger, inverter control, and SSCG*
- 64-pin LQFP (HE3), 80-pin LQFP (HF3), 100-pin LQFP (HG3), 144-pin LQFP (HJ3)

* Spread spectrum frequency synthesizer clock generator

V850ES/IK1

- For inverter control
- 63 MIPS @ 32 MHz, 3.5 to 5.5 V operation (A/D converter: 4.5 to 5.5 V)
- ROM/RAM: 64 KB/4 KB, 128 KB/6 KB
- On-chip 3-phase inverter control PWM timer, two A/D converters, POC, LVI, and clock monitor
- On-chip debugger (can be used with MINICUBE2)
- 64-pin LQFP

V850ES/IE2

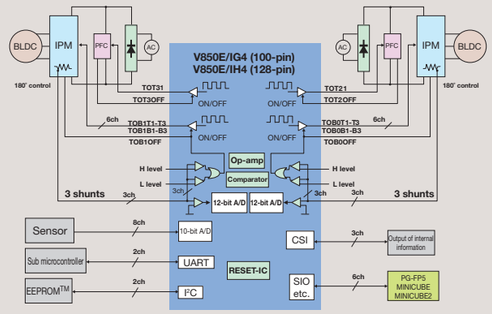
- All Flash products, for inverter control
- 39 MIPS @ 20 MHz, 3.5 to 5.5 V operation (A/D converter: 4.5 to 5.5 V)
- ROM/RAM: 64 KB/6 KB, 128 KB/6 KB
- On-chip 3-phase inverter control PWM timer, two A/D converters, POC, LVI, and clock monitor
- On-chip debugger (can be used with MINICUBE2)
- 64-pin LQFP

Application examples

■ 180° control for two motors

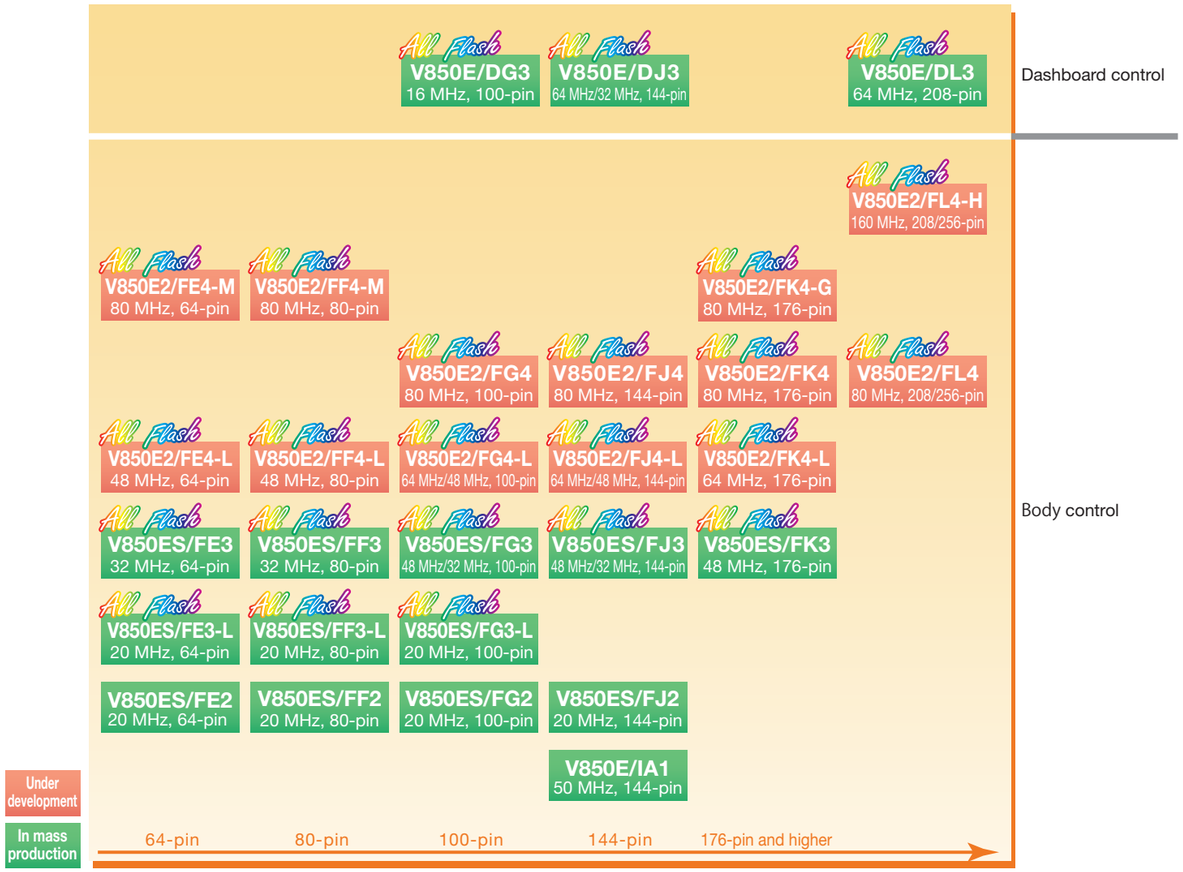
180° Control for Two Motors

V850E/IG4,IH4



Product Lineup

ASSP Lineup (Dashboard Control, Body Control)



Remark See Product Specification List (pp. 63 to 72) for details about the product specifications.

Features

V850E/DG3, DJ3, DL3

- All Flash products, for automotive electronics (dashboard control applications)
- 126 MIPS @ 64 MHz (DJ3, DL3), 69 MIPS @ 32 MHz (DJ3), 34 MIPS @16 MHz (DG3), 3.2 to 5.5 V operation (A/D converter: 3.5 to 5.5 V)
- ROM/RAM: 128 KB/6 KB to 2048 KB/84 KB
- On-chip CAN (2 ch max.) and LIN-compatible UART (2 ch)
- On-chip meter driver, voltage comparator (DJ3, DL3 only), sound generator, POC, clock monitor, DMAC (DJ3, DL3 only), and SSCG*
- 100-pin LQFP (DG3), 144-pin LQFP (DJ3), 208-pin LQFP (DL3)

* Spread spectrum frequency synthesizer clock generator

V850E2/FL4-H

- All Flash products, for automotive electronics (body control applications)
- 324 MIPS @ 160 MHz, 3.0 to 5.5 V operation
- ROM/RAM: 2 MB/144 KB
- On-chip CAN (6 ch) and LIN-compatible UART (12 ch max.)
- On-chip multi-channel A/D converter, motor control, POC, LVI, clock monitor, DMAC, and on-chip debugger
- Random number generator
- FlexRay controller: 2 ch × 1 unit
- 208-pin QFP, 256-pin BGA

V850E2/FE4-M, FF4-M

- All Flash products, for automotive electronics (body control applications)
- 205 MIPS @ 80 MHz, 3.0 to 5.5 V operation
- ROM/RAM: 256 KB/32 KB to 512 KB/48 KB
- On-chip CAN (1 ch) and LIN-compatible UART (3 ch max.)
- On-chip multi-channel A/D converter, motor control, POC, LVI, clock monitor, DMAC, on-chip debugger, and random number generator
- 64-pin LQFP (FE4-M), 80-pin LQFP (FF4-M)

V850E2/FK4-G

- All Flash products, for automotive electronics (body control applications)
- 3.0 to 5.5 V operation
- ROM/RAM: 1024 KB/128 KB
- On-chip CAN (6 ch) and LIN-compatible UART (5 ch)
- On-chip multi-channel A/D converter, POC, LVI, clock monitor, DMAC, on-chip debugger, and random number generator
- FlexRay controller: 2 ch × 1 unit
- 176-pin LQFP

V850E2/FG4, FJ4, FK4, FL4

- All Flash products, for automotive electronics (body control applications)
- 162 MIPS @ 80 MHz, 3.0 to 5.5 V operation
- ROM/RAM: 512 KB/32 KB to 2 MB/144 KB
- On-chip CAN (5 ch max.) and LIN-compatible UART (12 ch max.)
- On-chip multi-channel A/D converter, motor control, POC, LVI, clock monitor, DMAC, on-chip debugger, and random number generator
- FlexRay controller: 2 ch × 1 unit (μPD70F4000 to μPD70F4012 only)
- 100-pin LQFP (FG4), 144-pin LQFP (FJ4), 176-pin LQFP (FK4), 208-pin QFP (FL4), 256-pin BGA (FL4)

V850E2/FE4-L, FF4-L, FG4-L, FJ4-L, FK4-L

- All Flash products, for automotive electronics (body control applications)
- 109 MIPS @ 64 MHz, 82 MIPS @ 48 MHz, 3.0 to 5.5 V operation
- ROM/RAM: 256 KB/24 KB to 1.5 MB/96 KB
- On-chip CAN (2 ch max.) and LIN-compatible UART (5 ch max.)
- On-chip multi-channel A/D converter, POC, LVI, clock monitor, and on-chip debugger
- 64-pin LQFP (FE4-L), 80-pin LQFP (FF4-L), 100-pin LQFP (FG4-L), 144-pin LQFP (FJ4-L), 176-pin LQFP (FK4-L)

V850ES/FE3, FF3, FG3, FJ3, FK3

- All Flash products, for automotive electronics (body control applications)
- 98 MIPS @ 48 MHz, 69 MIPS @ 32 MHz, 3.3 to 5.5 V operation (A/D converter: 4.0 to 5.5 V)
- ROM/RAM: 128 KB/8 KB to 1024 KB/60 KB
- On-chip CAN (5 ch max.) and LIN-compatible UART (8 ch max.)
- On-chip multi-channel A/D converter, motor control, POC, LVI, clock monitor, DMAC, on-chip debugger, and SSCG*
- 64-pin LQFP (FE3), 80-pin LQFP (FF3), 100-pin LQFP (FG3), 144-pin LQFP (FJ3), 176-pin LQFP (FK3)

* Spread spectrum frequency synthesizer clock generator

V850ES/FE3-L, FF3-L, FG3-L

- All Flash products, for automotive electronics (body control applications)
- 43 MIPS @ 20 MHz, 3.3 to 5.5 V operation (A/D converter: 4.0 to 5.5 V)
- ROM/RAM: 64 KB/6 KB to 256 KB/16 KB
- On-chip CAN (1 ch) and LIN-compatible UART (3 ch max.)
- On-chip multi-channel A/D converter, POC, LVI, clock monitor, and on-chip debugger
- 64-pin LQFP (FE3-L), 80-pin LQFP (FF3-L), 100-pin LQFP (FG3-L)

V850ES/FE2, FF2, FG2, FJ2

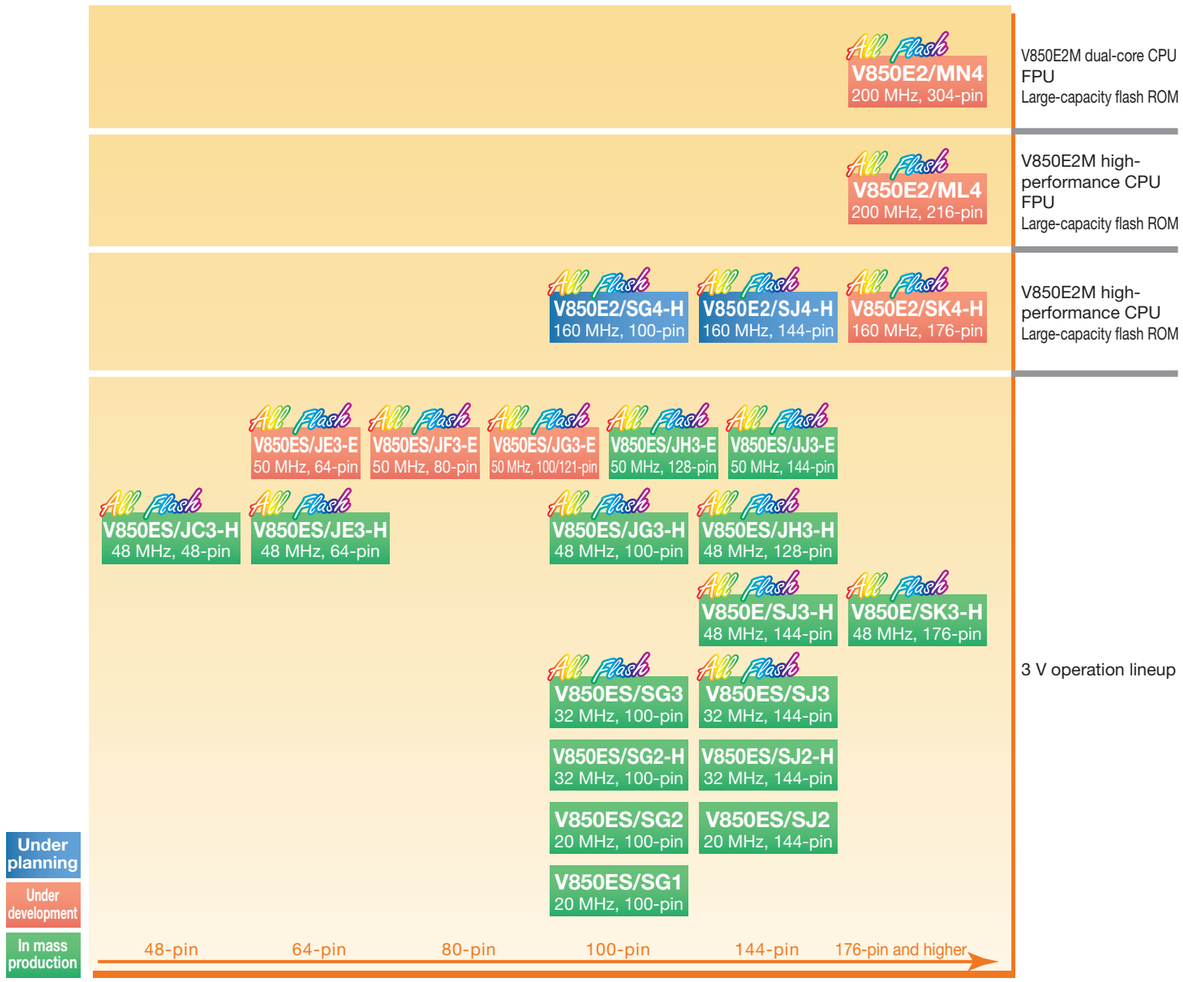
- For automotive electronics (body control applications)
- 43 MIPS @ 20 MHz, 3.5 to 5.5 V operation (A/D converter: 4.0 to 5.5 V)
- ROM/RAM: 64 KB/4 KB to 512 KB/20 KB
- On-chip CAN (4 ch max.) and LIN-compatible UART (4 ch max.)
- On-chip multi-channel A/D converter, POC, LVI, DMAC, and on-chip debugger
- 64-pin LQFP (FE2), 80-pin TQFP (FF2), 100-pin LQFP (FG2), 144-pin LQFP (FJ2)

V850E/IA1

- For automotive electronics (body control applications)
- 103 MIPS @ 50 MHz, internal 3.0 to 3.6 V/ external 4.5 to 5.5 V operation
- ROM/RAM: 256 KB/10 KB
- On-chip CAN (1 ch)
- On-chip 3-phase inverter control PWM timer, 2-phase encoder timer, two A/D converters, and DMAC
- 144-pin LQFP

Product Lineup

ASSP Lineup (CAN)



Remark See Product Specification List (pp. 73 to 79) for details about the product specifications.

Features

V850E2/MN4

- All flash products, for general-purpose applications
- 512 MIPS @ 200 MHz, internal 1.1 to 1.3 V/ external 3.0 to 3.6 V operation
- ROM/RAM: 2 MB/128 MB, 1 MB/128 KB, 1 MB/64 KB
- On-chip CAN (2 ch)
- USB (Host, Function), Ethernet controller, and DMAC
- Ultra-high-speed dual-core CPU
- 304-pin FBGA

V850E2/ML4

- All flash products, for general-purpose applications
- 512 MIPS @ 200 MHz, internal 1.1 V to 1.3 V/ external 3.0 V to 3.6 V operation
- ROM/RAM: 768 KB/128 KB*, 1 MB/128 KB*
- On-chip CAN (1 ch)
- USB (Host, Function), Ethernet controller, and DMAC
- 216-pin LQFP

* Includes 64 KB of expanded internal RAM.

V850E2/SG4-H,SJ4-H,SK4-H

- All Flash products, for car infotainment systems
- 325 MIPS @ 160 MHz, internal 1.1 to 1.3 V/ external 3.0 to 3.6 V operation
- ROM/RAM: 1 MB/96 KB to 2 MB/192 KB
- On-chip CAN (2 ch max.), IEBus (1 ch), LVI, DMAC, on-chip debugger, and Ethernet controller (V850E2/SK4-H only)
- 100-pin LQFP (SG4-H), 144-pin LQFP (SJ4-H), 176-pin LQFP (SK4-H)

V850ES/JE3-E, JF3-E, JG3-E, JH3-E, JJ3-E

- All Flash products, for general-purpose applications
- 103 MIPS @ 50 MHz, 2.85 to 3.6 V operation (A/D converter, USB controller: 3.0 to 3.6 V)
- ROM/RAM: 256 KB/64 KB* to 512 KB/124 KB**
- CAN × 1 ch, UART supporting LIN x max 3 ch (JE3-E) to 8 ch (JJ3-E)
- USB controller: USB 2.0 function (full-speed) × 1 ch
- Ethernet controller × 1 ch
- 64-pin LQFP/WQFN (JE3-E), 64-pin FBGA (μPD70F3824), 80-pin LQFP (JF3-E), 100-pin LQFP/121-pin FBGA (JG3-E), 128-pin LQFP (JH3-E), 144-pin LQFP (JJ3-E)

* Includes 16 KB of data-only RAM.
** Includes 64 KB of data-only RAM.

V850ES/JC3-H, JE3-H, JG3-H, JH3-H

- All flash products, for general-purpose applications
- 98 MIPS @ 48 MHz, 2.85 to 3.6 V operation (A/D converter, USB controller: 3.0 to 3.6 V)
- ROM/RAM: 256 KB/24 KB to 256 KB/40 KB*
- On-chip CAN (1 ch) and LIN-compatible UART (4 ch or 5 ch max.)
- USB controller: USB 2.0 function (full-speed) × 1 ch
- 48-pin LQFP/WQFN (JC3-H), 64-pin LQFP/FBGA/WQFN (JE3-H), 100-pin LQFP (JG3-H), 128-pin LQFP (JH3-H)

* Includes 8 KB of data-only RAM.

V850E/SJ3-H, SK3-H

- All flash products, for car infotainment systems
- 95 MIPS @ 48 MHz, 2.85 to 3.6 V operation (A/D converter: 3.0 to 3.6 V)
- ROM/RAM: 512 KB/60 KB (SJ3-H only), 768 KB/76 KB* (SJ3-H only), 1024 KB/76 KB*, 1280 KB/92 KB**, 1536 KB/92 KB**
- On-chip CAN (2 ch max.), UART (8 ch max. (including two UART channels with FIFO buffers)), IEBus (1 ch), multi-channel serial interface, LVI, clock monitor, CRC, DMAC, real-time counter, SSCG***, and on-chip debugger
- 5 V withstand-voltage ports incorporated, and 5 V output is possible by setting N-ch open-drain output
- 144-pin LQFP (SJ3-H), 176-pin LQFP (SK3-H)

* Includes 16 KB of expanded internal RAM.
** Includes 32 KB of expanded internal RAM.
*** Spread spectrum frequency synthesizer clock generator

V850ES/SG3, SJ3

- All Flash products, for car infotainment systems
- 69 MIPS @ 32 MHz, 2.85 to 3.6 V operation (A/D converter: 3.0 to 3.6 V)
- ROM/RAM: 256 KB/24 KB to 1024 KB/60 KB
- On-chip CAN (2 ch max.), LIN-compatible UART (4 ch max.), IEBus (1 ch), multi-channel serial interface, LVI, clock monitor, CRC, DMAC, and on-chip debugger
- 5 V withstand-voltage ports incorporated, and 5 V output is possible by setting N-ch open-drain output
- 100-pin LQFP (SG3), 144-pin LQFP (SJ3)

V850ES/SG2, SJ2, SG2-H, SJ2-H

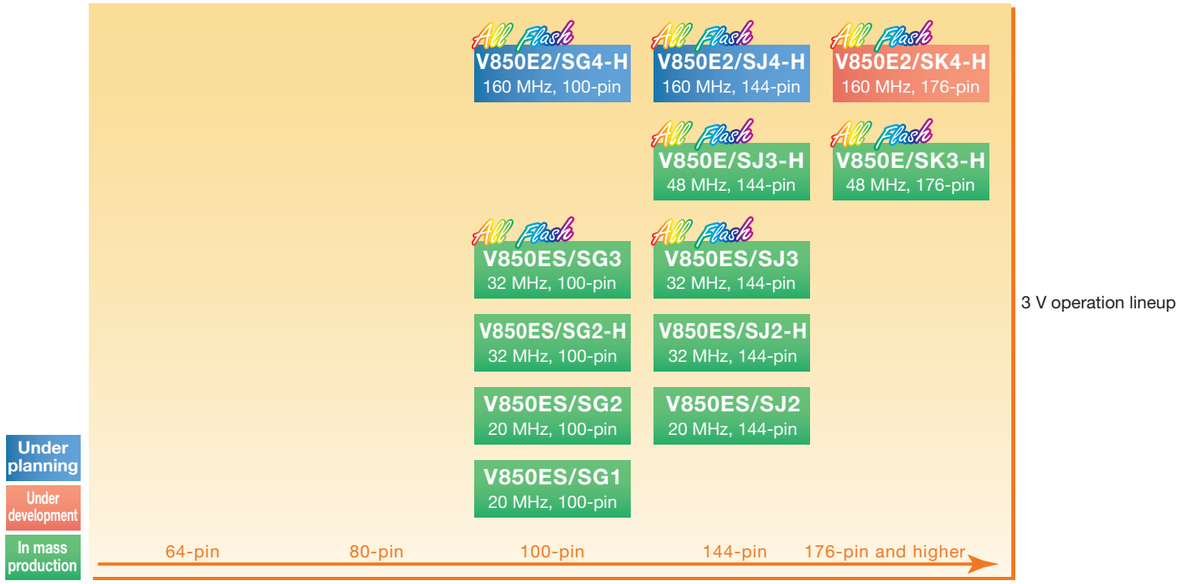
- For car infotainment systems
- 43 MIPS @ 20 MHz, 2.85 to 3.6 V operation (A/D converter: 3.0 to 3.6 V) (SG2, SJ2)
  66 MIPS @ 32 MHz, 3.0 to 3.6 V operation (SG2-H, SJ2-H)
- ROM/RAM: 256 KB/24 KB (SG2, SJ2 only), 384 KB/32 KB (SG2, SJ2 only), 512 KB/40 KB, 640 KB/48 KB
- On-chip CAN (2 ch max.), LIN-compatible UART (4 ch max.), multi-channel serial interface, LVI (SG2, SJ2 only), clock monitor, CRC, DMAC, and on-chip debugger
- 5 V withstand-voltage ports incorporated, and 5 V output is possible by setting N-ch open-drain output
- 100-pin LQFP (SG2, SG2-H), 144-pin LQFP (SJ2, SJ2-H)

V850ES/SG1

- For car infotainment systems
- 43 MIPS @ 20 MHz, 2.85 to 3.6 V operation (A/D converter: 3.0 to 3.6 V)
- ROM/RAM: 128 KB/8 KB
- On-chip CAN (1 ch), clock monitor, and DMAC
- 5 V withstand-voltage ports incorporated, and 5 V output is possible by setting N-ch open-drain output
- 100-pin LQFP

Product Lineup

ASSP Lineup (Car Audio/Vehicle Navigation Control)



Remark See Product Specification List (pp. 80 to 83) for details about the product specifications.

Features

V850E2/SG4-H, SJ4-H, SK4-H

- All Flash products, for car infotainment systems
- 325 MIPS @ 160 MHz, internal 1.1 to 1.3 V/external 3.0 to 3.6 V
- ROM/RAM: 1 MB/96 KB to 2 MB/192 KB
- On-chip LIN-compatible UART (5 ch max.), IEBus (1 ch), LVI, DMAC, on-chip debugger, and Ethernet controller (V850E2/SK4-H only)
- 100-pin LQFP (SG4-H), 144-pin LQFP (SJ4-H), 176-pin LQFP (SK4-H)

V850E/SJ3-H, SK3-H

- All flash products, for car infotainment systems
- 95 MIPS @ 48 MHz, 2.85 to 3.6 V operation (A/D converter: 3.0 to 3.6 V)
- ROM/RAM: 512 KB/60 KB (SJ3-H only), 768 KB/76 KB* (SJ3-H only), 1024 KB/76 KB*, 1280 KB/92 KB**, 1536 KB/92 KB**
- On-chip UART (8 ch max. (including two UART channels with FIFO)), IEBus (1 ch), multi-channel serial interface, LVI, clock monitor, CRC, DMAC, real-time counter, SSCG***, and on-chip debugger
- 5 V withstand-voltage ports incorporated, and 5 V output is possible by setting N-ch open-drain output
- 144-pin LQFP (SJ3-H), 176-pin LQFP (SK3-H)

* Includes 16 KB of expanded internal RAM.
** Includes 32 KB of expanded internal RAM.
*** Spread spectrum frequency synthesizer clock generator

V850ES/SG3, SJ3

- All Flash products, for car infotainment systems
- 69 MIPS @ 32 MHz, 2.85 to 3.6 V operation (A/D converter: 3.0 to 3.6 V)
- ROM/RAM: 256 KB/24 KB to 1024 KB/60 KB
- On-chip LIN-compatible UART (4 ch max.), IEBus (1 ch), multi-channel serial interface, LVI, clock monitor, CRC, DMAC, and on-chip debugger
- 5 V withstand-voltage ports incorporated, and 5 V output is possible by setting N-ch open-drain output
- 100-pin LQFP (SG3), 144-pin LQFP (SJ3)

V850ES/SG2-H, SJ2-H

- For car infotainment systems
- 66 MIPS @ 32 MHz, 3.0 to 3.6 V operation
- ROM/RAM: 512 KB/40 KB, 640 KB/48 KB
- On-chip LIN-compatible UART (4 ch max.), IEBus (1 ch), multi-channel serial interface, clock monitor, CRC, DMAC, and on-chip debugger
- 5 V withstand-voltage ports incorporated, and 5 V output is possible by setting N-ch open-drain output
- 100-pin LQFP (SG2-H), 144-pin LQFP (SJ2-H)

V850ES/SG2, SJ2

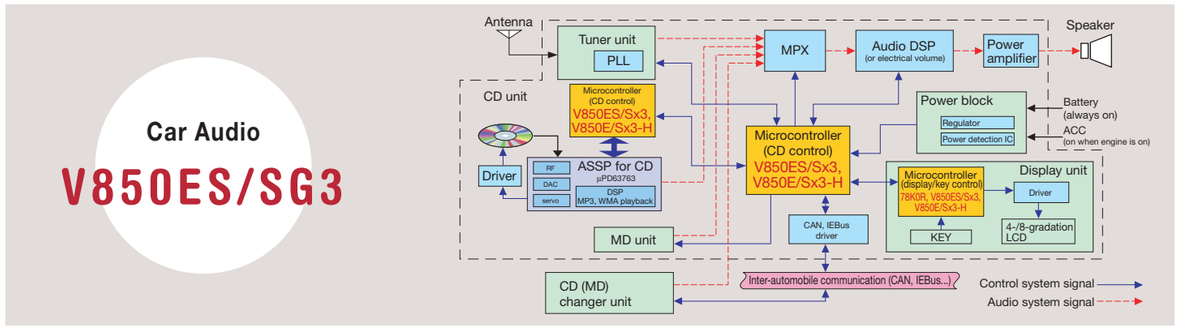
- For car infotainment systems
- 43 MIPS @ 20 MHz, 2.85 to 3.6 V operation (A/D converter: 3.0 to 3.6 V)
- ROM/RAM: 256 KB/24 KB, 384 KB/32 KB, 512 KB/40 KB, 640 KB/48 KB
- On-chip LIN-compatible UART (4 ch max.), IEBus (1 ch), multi-channel serial interface, LVI, clock monitor, CRC, DMAC, and on-chip debugger
- 5 V withstand-voltage ports incorporated, and 5 V output is possible by setting N-ch open-drain output
- 100-pin LQFP (SG2), 100-pin QFP (SG2 (ROM: 256 KB/384 KB versions only)), 144-pin LQFP (SJ2)

V850ES/SG1

- For car infotainment systems
- 43 MIPS @ 20 MHz, 2.85 to 3.6 V operation (A/D converter: 3.0 to 3.6 V)
- ROM/RAM: 256 KB/12 KB
- On-chip IEBus (1 ch) and clock monitor
- 5 V withstand-voltage ports incorporated, and 5 V output is possible by setting N-ch open-drain output
- 100-pin LQFP, 100-pin QFP

Application examples

■ Car audio



Product Lineup

Memory Lineup

Flash memory version | Mask ROM version | Mask ROM/flash memory version

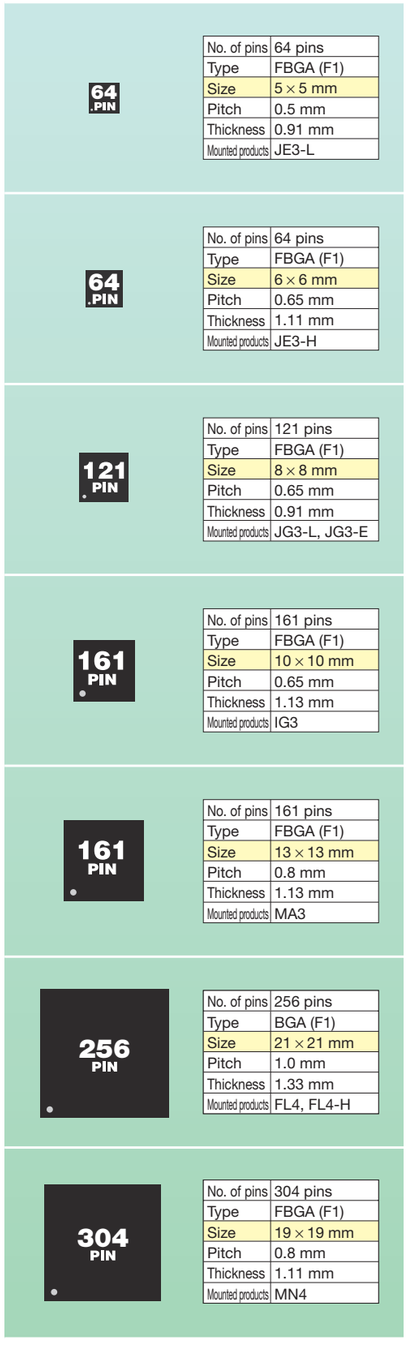
ROM size (bytes)	4 K	6 K	8 K	10 K	12 K	16 K	20 K	24 K	28 K	32 K	40 K	48 K	56 K	60 K	64 K	76 K	80 to 84 K	92 to 96 K	112 K	124 to 128 K	144 K	192 K
2048 K																	DJ3-64*1			MN4	FK4 FL4 FL4-H	SK4-H
1536 K																		SJ3-H*5 SK3-H*5 FJ4-L FK4-L	FJ4 FL4 FL4-H	SG4-H SJ4-H SK4-H		
1280 K																		SJ3-H*5 SK3-H*5				
1024 K						DJ3-64*1						FJ3-48*1		SJ3 SG3 JJ3 JG3 DL3 FK3	MN4 FG4-L FJ4-L FK4-L	SJ3-H*6 SK3-H*6	FG4 FJ4 FK4 JG3-L	SG4-H SJ4-H		MN4 ML4*7 FK4-G		
768 K									FJ3-48*1			FG4-L FK4-L FJ4-L FK3		SJ3 JJ3 SG3 JG3	FG4 FJ4 FK4	SJ3-H*6	JG3-L			ML4*7		
640 K												SJ2-H SJ2 SG2-H SG2 SJ3 SG3										
512 K				MA3	FJ2 DJ3-32*1	DJ3-64*1			JJ3 SG3 JG3 SJ2-H JG3-L SG2-H SJ2 SG2 SJ3	MA3 FJ3-48*1 FE4-L FG3-48*1 FF4-L HJ3 FG4-L FJ4-L FK3		FG4 FE4-M FJ4 FF4-M	JG3-H*2 JH3-H*2 JG3-U*2 JH3-U*2	SJ3-H			JH3-E*3 JJ3-E*3			JH3-E*4 JJ3-E*4		
480 K						IG4 IG4-H IH4 IH4-H																	
384 K				FG2 DJ3-32*1		FJ3-48*1 IH4 FG3-48*1 IG4-H IG4 IH4-H	FE4-L FF4-L FG4-L FJ4-L	JJ3 SG3 JG3 SJ2 JG3-L SG2 SJ3	FE4-M FF4-M JG3-L			JG3-H*2 JH3-H*2	JG3-U*2 JH3-U*2			JH3-E*3					JH3-E*4		
376 K					FJ2																		
256 K			MA3	IA1	FJ2 FG2 FF2 DJ3-32*1 DG3 SG1 IG3 IF3 IA4 IA3	MA3 FJ3-32*1 FG3-32*1 FF3 FE3 FG3-L FF3-L FE3-L JC3-L JE3-L JG3-L HJ3 HG3 HF3		SG3 SG2 FE4-L FF4-L FG4-L FJ4-L JE3-H JC3-H IG4 IH4 IG4-H IH4-H		MA3 FE4-M FF4-M	JG3-H*2 JH3-H*2 JG3-L			JG3-E*2 JF3-E*2 JE3-E*2	JH3-E*3						
192 K					FG3-L FF3-L FE3-L																		
128 K		FE2 FF2 FG2 DG3 IK1 IA4 IA3 IA2 IE2	SA2 FG3-32*1 FF3 FE3 HE3 JG3-L JF3-L JE3-L JC3-L IG3 IF3 FE3-L FF3-L FG3-L SG1		FF2			JE3-H JC3-H				JG3-E*3 JF3-E*3 JE3-E*3											
96 K		FE3-L FF3-L																				
64 K	IK1 FE2	IE2 FE3-L FF3-L	JE3-L JC3-L					JE3-H JC3-H		JG3-E*3 JF3-E*3 JE3-E*3												
32 K			JE3-L JC3-L			JE3-H JC3-H																
16 K			JE3-H JC3-H JE3-L JC3-L																			
ROM less						ME2 Instruction RAM: 128 KB				ME3 Instruction RAM: 168 KB		ST2										

RAM size (bytes)

*1. -32: 32 MHz product, -48: 48 MHz product, -64: 64 MHz product *2. Includes 8 KB of data-only RAM. *3. Includes 16 KB of data-only RAM. *4. Includes 64 KB of data-only RAM.
*5. Includes 32 KB of expanded internal RAM. *6. Includes 16 KB of expanded internal RAM. *7. Includes 64 KB of expanded internal RAM.

Product Lineup

Package Lineup



No. of pins	64 pins
Type	FBGA (F1)
Size	5 × 5 mm
Pitch	0.5 mm
Thickness	0.91 mm
Mounted products	JE3-L

No. of pins	64 pins
Type	FBGA (F1)
Size	6 × 6 mm
Pitch	0.65 mm
Thickness	1.11 mm
Mounted products	JE3-H

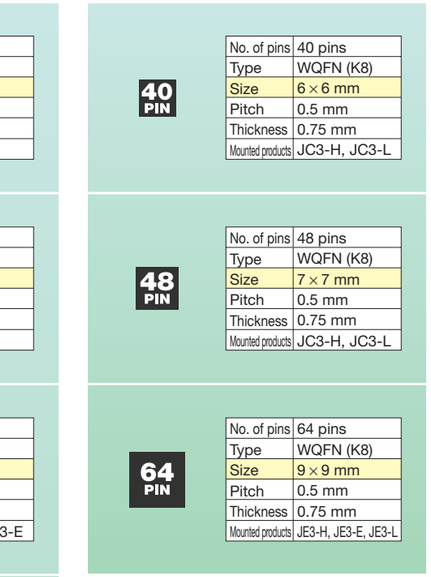
No. of pins	121 pins
Type	FBGA (F1)
Size	8 × 8 mm
Pitch	0.65 mm
Thickness	0.91 mm
Mounted products	JG3-L, JG3-E

No. of pins	161 pins
Type	FBGA (F1)
Size	10 × 10 mm
Pitch	0.65 mm
Thickness	1.13 mm
Mounted products	IG3

No. of pins	161 pins
Type	FBGA (F1)
Size	13 × 13 mm
Pitch	0.8 mm
Thickness	1.13 mm
Mounted products	MA3

No. of pins	256 pins
Type	BGA (F1)
Size	21 × 21 mm
Pitch	1.0 mm
Thickness	1.33 mm
Mounted products	FL4, FL4-H

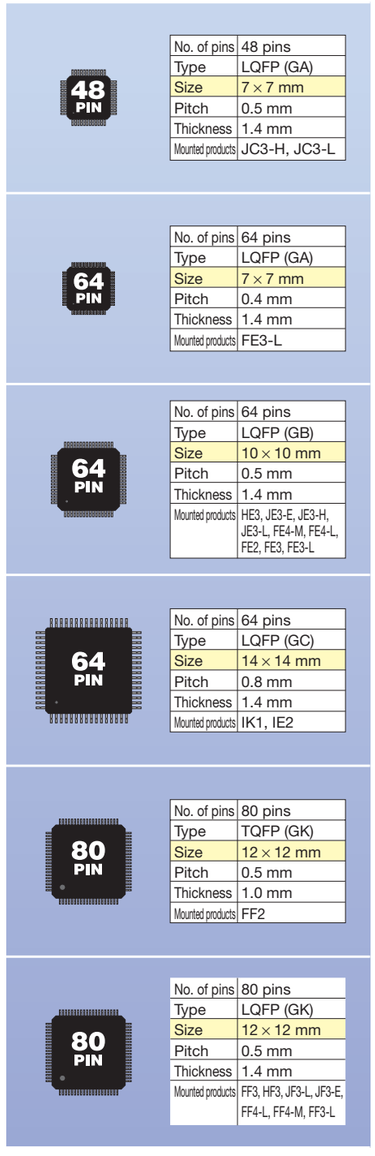
No. of pins	304 pins
Type	FBGA (F1)
Size	19 × 19 mm
Pitch	0.8 mm
Thickness	1.11 mm
Mounted products	MN4



No. of pins	40 pins
Type	WQFN (K8)
Size	6 × 6 mm
Pitch	0.5 mm
Thickness	0.75 mm
Mounted products	JC3-H, JC3-L

No. of pins	48 pins
Type	WQFN (K8)
Size	7 × 7 mm
Pitch	0.5 mm
Thickness	0.75 mm
Mounted products	JC3-H, JC3-L

No. of pins	64 pins
Type	WQFN (K8)
Size	9 × 9 mm
Pitch	0.5 mm
Thickness	0.75 mm
Mounted products	JE3-H, JE3-E, JE3-L



No. of pins	48 pins
Type	LQFP (GA)
Size	7 × 7 mm
Pitch	0.5 mm
Thickness	1.4 mm
Mounted products	JC3-H, JC3-L

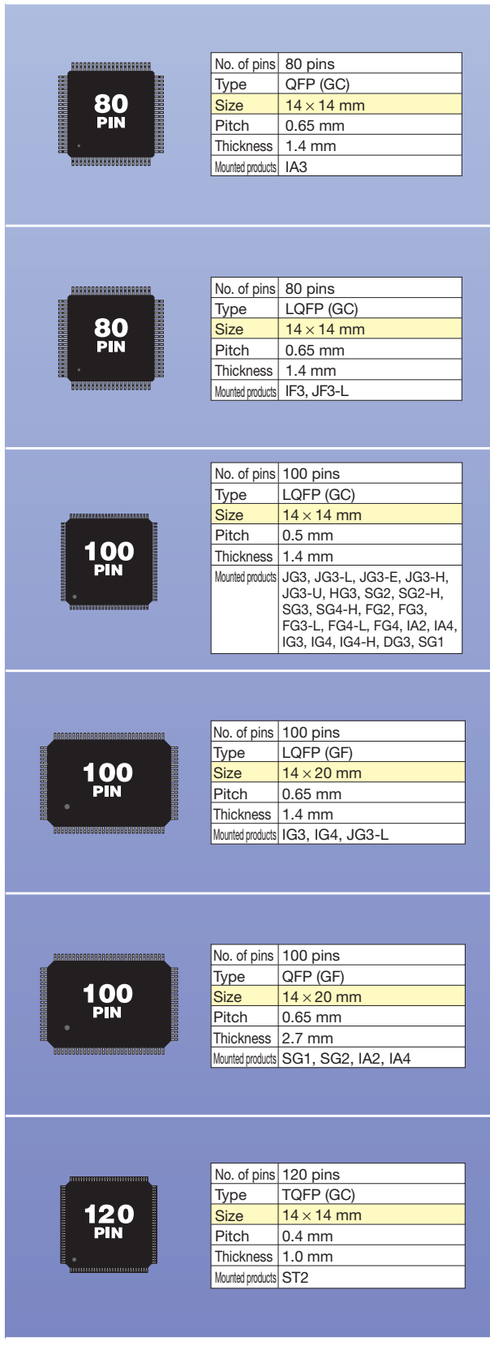
No. of pins	64 pins
Type	LQFP (GA)
Size	7 × 7 mm
Pitch	0.4 mm
Thickness	1.4 mm
Mounted products	FE3-L

No. of pins	64 pins
Type	LQFP (GB)
Size	10 × 10 mm
Pitch	0.5 mm
Thickness	1.4 mm
Mounted products	HE3, JE3-E, JE3-H, JE3-L, FE4-M, FE4-L, FE2, FE3, FE3-L

No. of pins	64 pins
Type	LQFP (GC)
Size	14 × 14 mm
Pitch	0.8 mm
Thickness	1.4 mm
Mounted products	IK1, IE2

No. of pins	80 pins
Type	TQFP (GK)
Size	12 × 12 mm
Pitch	0.5 mm
Thickness	1.0 mm
Mounted products	FF2

No. of pins	80 pins
Type	LQFP (GK)
Size	12 × 12 mm
Pitch	0.5 mm
Thickness	1.4 mm
Mounted products	FF3, HF3, JF3-L, JF3-E, FF4-L, FF4-M, FF3-L



No. of pins	80 pins
Type	QFP (GC)
Size	14 × 14 mm
Pitch	0.65 mm
Thickness	1.4 mm
Mounted products	IA3

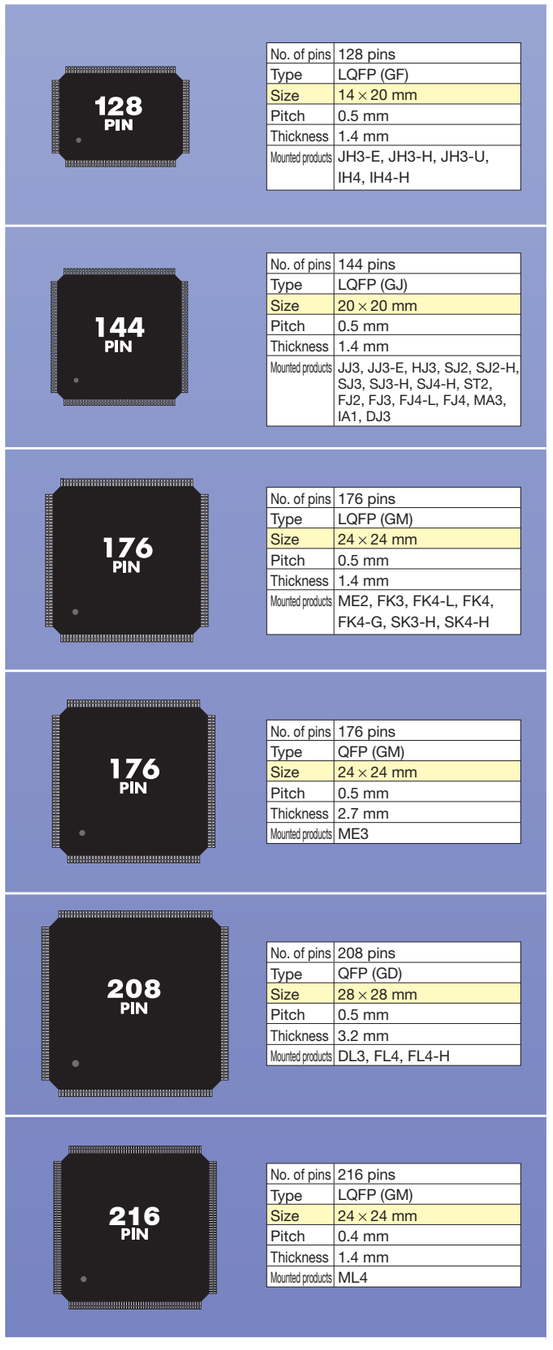
No. of pins	80 pins
Type	LQFP (GC)
Size	14 × 14 mm
Pitch	0.65 mm
Thickness	1.4 mm
Mounted products	IF3, JF3-L

No. of pins	100 pins
Type	LQFP (GC)
Size	14 × 14 mm
Pitch	0.5 mm
Thickness	1.4 mm
Mounted products	JG3, JG3-L, JG3-E, JG3-H, JG3-U, HG3, SG2, SG2-H, SG3, SG4-H, FG2, FG3, FG3-L, FG4-L, FG4, IA2, IA4, IG3, IG4, IG4-H, DG3, SG1

No. of pins	100 pins
Type	LQFP (GF)
Size	14 × 20 mm
Pitch	0.65 mm
Thickness	1.4 mm
Mounted products	IG3, IG4, JG3-L

No. of pins	100 pins
Type	QFP (GF)
Size	14 × 20 mm
Pitch	0.65 mm
Thickness	2.7 mm
Mounted products	SG1, SG2, IA2, IA4

No. of pins	120 pins
Type	TQFP (GC)
Size	14 × 14 mm
Pitch	0.4 mm
Thickness	1.0 mm
Mounted products	ST2



No. of pins	128 pins
Type	LQFP (GF)
Size	14 × 20 mm
Pitch	0.5 mm
Thickness	1.4 mm
Mounted products	JH3-E, JH3-H, JH3-U, IH4, IH4-H

No. of pins	144 pins
Type	LQFP (GJ)
Size	20 × 20 mm
Pitch	0.5 mm
Thickness	1.4 mm
Mounted products	JJ3, JJ3-E, HJ3, SJ2, SJ2-H, SJ3, SJ3-H, SJ4-H, ST2, FJ2, FJ3, FJ4-L, FJ4, MA3, IA1, DJ3

No. of pins	176 pins
Type	LQFP (GM)
Size	24 × 24 mm
Pitch	0.5 mm
Thickness	1.4 mm
Mounted products	ME2, FK3, FK4-L, FK4, FK4-G, SK3-H, SK4-H

No. of pins	176 pins
Type	QFP (GM)
Size	24 × 24 mm
Pitch	0.5 mm
Thickness	2.7 mm
Mounted products	ME3

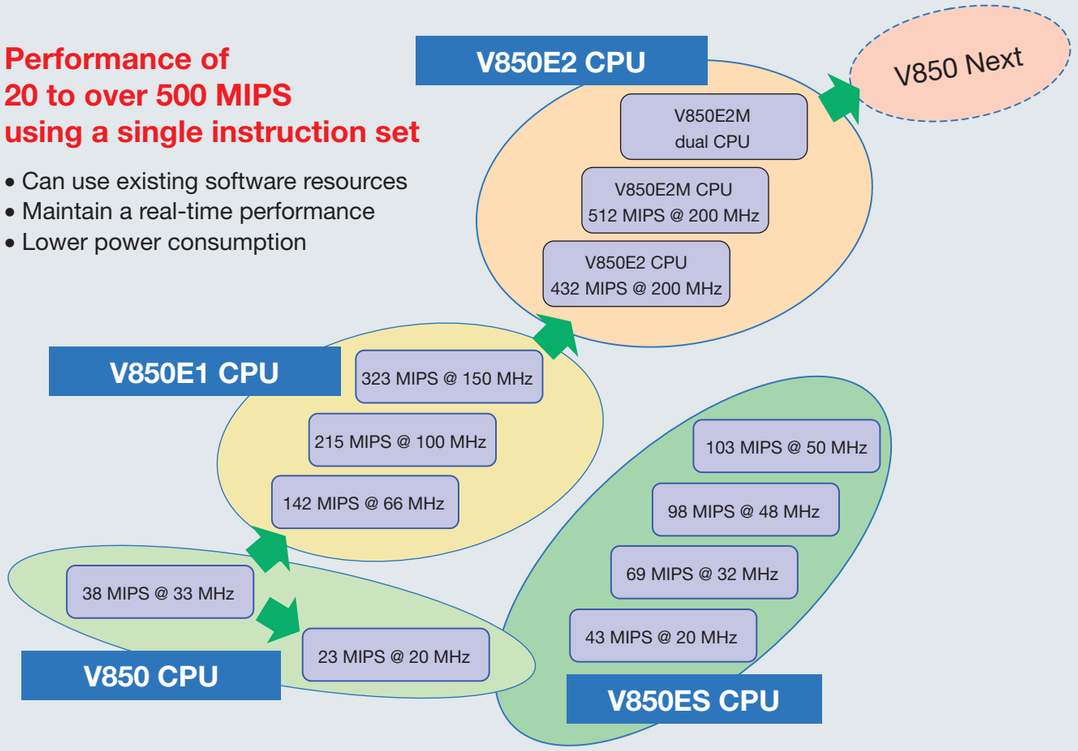
No. of pins	208 pins
Type	QFP (GD)
Size	28 × 28 mm
Pitch	0.5 mm
Thickness	3.2 mm
Mounted products	DL3, FL4, FL4-H

No. of pins	216 pins
Type	LQFP (GM)
Size	24 × 24 mm
Pitch	0.4 mm
Thickness	1.4 mm
Mounted products	ML4

CPU Roadmap

Performance of 20 to over 500 MIPS using a single instruction set

- Can use existing software resources
- Maintain a real-time performance
- Lower power consumption



CPU Comparison

CPU / Characteristics	V850	V850ES	V850E1	V850E2	V850E2M
Maximum operating frequency	20/33 MHz	20/32/48/50 MHz	66 ⇒ 100 ⇒ 150 MHz	200 MHz	200 MHz
Instructions	47	80	80	89	98
Maximum program memory space	16 MB	16 MB	64 MB	512 MB (internal 128 MB)	4 GB
Maximum data memory space	16 MB	16 MB	256 MB	4 GB	4 GB
Higher performance	5-stage pipeline Harvard architecture	Improved pipeline • Non-blocking load/store instructions - Parallel instruction execution (instruction execution in internal ROM) • Addition of branching/load pipe • Shift to 3-operand manipulations in 1 slot		• 7-stage pipeline Simultaneous execution of 2 instructions	Optimized instruction execution Enhanced ability to execute 2 instructions simultaneously Can be used with a single-precision or double-precision high-speed FPU
High code efficiency	2-byte instructions CISC instructions	Addition of C language compatible instructions (Switch instruction, Callt instruction, data conversion instruction, Prepare/Dispose instruction)		32-bit relative branch instruction 3-operand instruction Sum-of-products instruction Bit search instruction	Expanded displacement of LD and ST instructions
Multiplier	16 × 16 bits ⇒ 32 bit operation	16 × 16 bits ⇒ 32-bit operation 32 × 32 bits ⇒ 64-bit operation (32-bit multiply instruction support)	16 × 16 bits ⇒ 32-bit operation 32 × 32 bits ⇒ 64-bit operation		
Interrupt responsiveness	11 to 18 clocks	4 to 10 clocks		–	

PFESiP Roadmap

PFESiP (Platform for Embedded System in a Package) is a new ASIC solution providing Gate Array quickly, cost-effectively, and safely with expanded functionality, by developing Gate Array and general-purpose function chips into SiPs, which are pre-verified and lined up as masters.

EP-3 overview

The EP-3, built around the V850E2M core, is the second in the EP (Embedded Processor) series of general-function chips incorporating a microcontroller. The EP-3 combines in a single package a Renesas 32-bit microcontroller and ASIC chips such as gate arrays or cell-based ICs. This platform makes it easy to create customized microcontroller products.
The EP-3 delivers better CPU performance than the EP-1 and operates at a high speed of 266 MHz. It supports high-speed USB functions and adds new communication interface functions such as Ethernet and CAN. The optimal bus, memory, and DMAC configuration helps to eliminate internal bus bottlenecks.

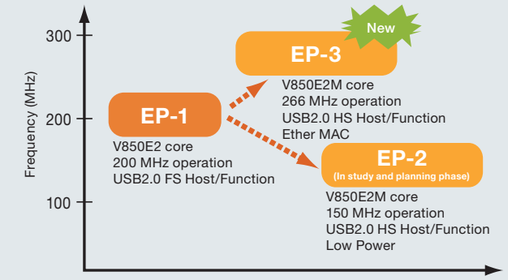
EP-3 Features

- ○ V850E2M CPU core, max. 266 MHz operation
- ○ Programmable logic (requires masking)
  Logic capacity: 160,000 to 1 million gates (EA-9HD/CB-12)
- ○ Multi-layer system bus
- ○ Memory bus: Entirely discrete external bus and SiP internal bus
- ○ Internal instruction RAM: Max. 512 KB
- ○ Work RAM: 64 KB × 2
- ○ Internal DMA controller with descriptor function
- ○ Internal serial flash memory controller
- ○ USB 2.0 HS ports: Host 1 ch, Function 1 ch
- ○ Ethernet: Internal 10/100 EtherMAC
- ○ Power supply voltage: Internal 1.0 V, I/O 3.3 V (1.5 V with CB-12 user logic)
- ○ Low-heat-resistance PBGA package
  550-pin (25 × 30 mm), 1 mm ball pitch
  544-pin (27 × 27 mm), 1 mm ball pitch

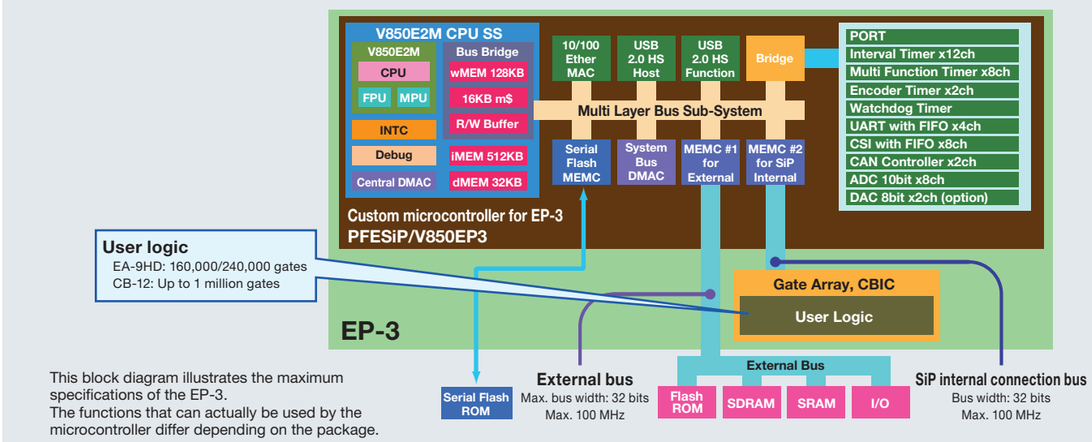
EP Series applications

- ○ Factory automation and industrial equipment
  Servers, inverters, PLC equipment, measuring devices, machine tools, vending machines, security cameras, etc.
- ○ Office equipment and consumer products
  Thermal/dot matrix printers, video/photo printers, card reader/writers, barcode readers, etc.

PFESiP [EP Series] Roadmap (V850 Core)



EP-3 block diagram



This block diagram illustrates the maximum specifications of the EP-3.
The functions that can actually be used by the microcontroller differ depending on the package.

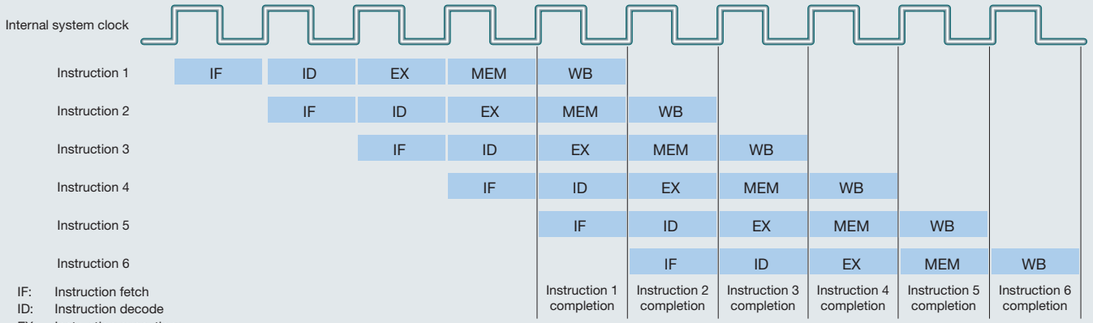
V850 Architecture

The V850 microcontrollers are single-chip RISC microcontrollers that use an architecture optimized for embedding, and have the following features:

- 5-stage pipeline processing
- Harvard architecture
- 32 general-purpose registers
- Simple addressing
- 2-byte basic instruction set
- Support of CISC-like instructions
- Multi-status flags
- DSP
- 32-bit barrel shifter

5-stage pipeline processing

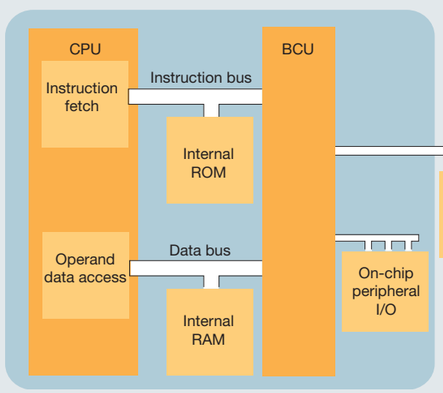
The V850 microcontrollers use a 5-stage pipeline structure (5 stages from instruction fetch to writeback) that supports simultaneous processing of 5 instructions, thus enabling the execution of almost all instructions in just one clock cycle.



IF: Instruction fetch
ID: Instruction decode
EX: Instruction execution
MEM: Memory access to target address
WB: Write execution result to register

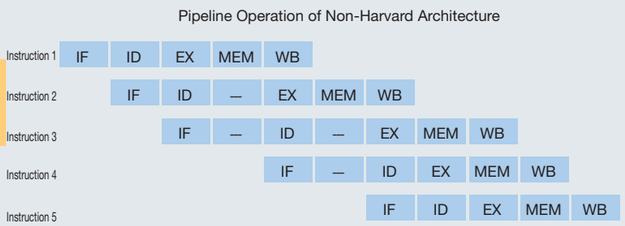
Harvard architecture

The V850 microcontrollers use Harvard architecture, which is designed so that the instruction bus and data bus can operate independently from each other, thereby preventing pipeline operation problems and ensuring efficient instruction execution.



In the case of an architecture other than Harvard architecture, the MEM stage of instruction 1 and the IF stage of instruction 4, and the MEM stage of instruction 2 and the IF stage of instruction 5 conflict, causing bus waits. This in turn causes the pipeline operation to become disordered and lowers the instruction execution speed.

Pipeline Operation of Non-Harvard Architecture

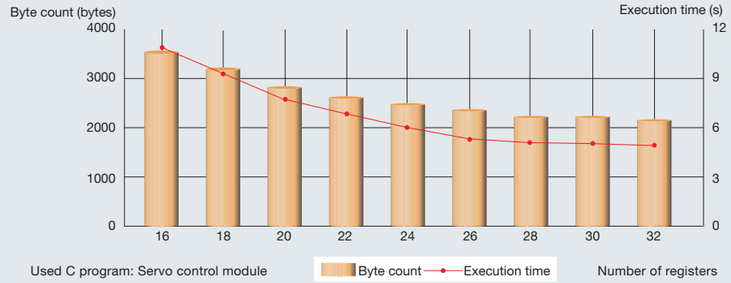


—: Idles inserted due to bus wait

32 general-purpose registers

The V850 microcontrollers have 32 general-purpose registers. Along with a hardware environment that is ideal for program execution, the development environment, including compilers, exploits these 32 registers to achieve program generation with superior code efficiency and execution performance.

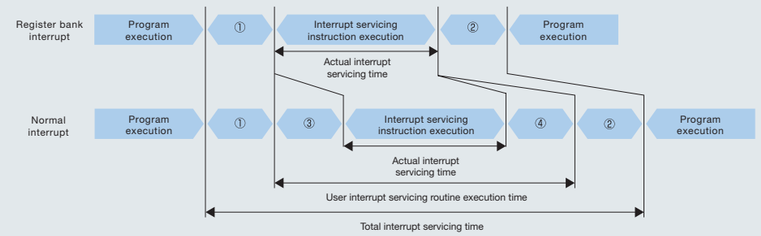
Comparison of Performance/Object Efficiency According to Number of Registers



For example, looking at the program execution time and code size changes when the number of registers used by the compiler is changed using the servo control module, we can see that the larger the number of registers, the better the program execution speed and the smaller the code size. However, from about 26 registers, the improvement in terms of execution speed and code size becomes smaller, and in the neighborhood of 32 registers, there are no more changes. This is why the V850 microcontrollers have been provided with 32 registers as a strict minimum requirement.

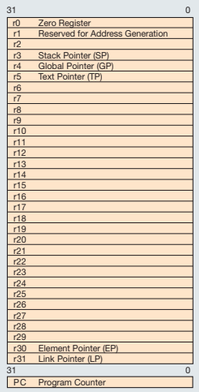
Software register bank

The number of registers can be selected from 22, 26, or 32 as a compiler option to efficiently execute application programs. Unused registers can be used as a software register bank for which backup and restore processing is not required during interrupt servicing or task switching, which increases the processing speed.



① Save the program counter, etc., to a backup register.
② Execute the interrupt restore instruction. Restore the program counter value, etc., from the backup register.
③ Save general-purpose registers to the stack.
④ Restore general-purpose registers from the stack.

General-purpose register configuration



Name	Application	Operation
r0	Zero register	Always holds "0"
r1	Assembler reservation	Used as working register for address generation
r2	Address/data variable register (If real-time OS being used does not use r2)	
r3	Stack pointer	Used for stack frame generation during function call
r4	Global pointer	Used when accessing global variables in the data area
r5	Text pointer	Used as register for specifying the beginning of the text area (program code allocation)
r6-r29	Address/data variable register	
r30	Element pointer	Used as base pointer for address generation during memory access
r31	Link pointer	Used during function call by compiler
PC	Program counter	Holds instruction addresses during program execution

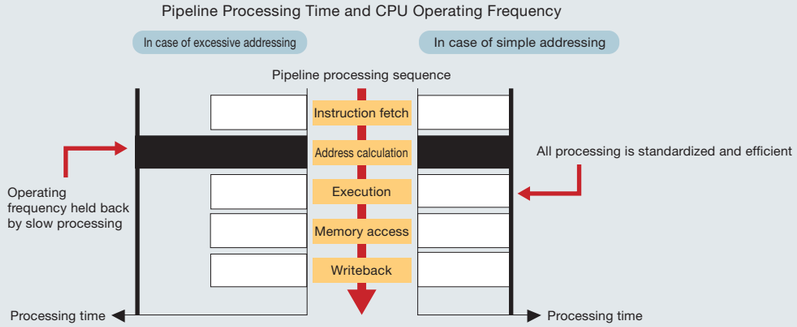
System register configuration

	No.	System Register Name	Operand Specification LDSR	Operand Specification STSR	Application
	0	EIPC	○	○	Register for saving status during interrupt
	1	EIPSW	○	○	
	2	FEPC	○	○	Register for saving status during NMI
	3	FEPSW	○	○	
	4	ECR	×	○	Interrupt source register
	5	PSW	○	○	Program status word
Supported by other than V850 CPU products	16	CTPC	○	○	Register for saving status during CALLT execution
	17	CTPSW	○	○	
	18	DBPC	○	○	Register for saving status during exception/debug trap
	19	DBPSW	○	○	
	20	CTBP	○	○	CALLT base pointer
	6-15, 21-31	Reserved	×	×	

×: Access prohibited
○: Access enabled
LDSR: Instruction to load general-purpose register contents to system register
STSR: Instruction to store system register contents to general-purpose register

Simple addressing

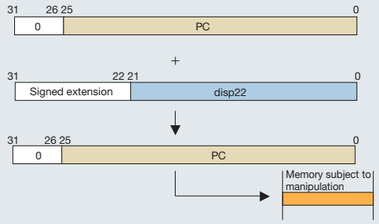
The increased amount of address calculations in the CPU in the case of complex addressing causes disturbances in the pipeline. As a result, address calculation becomes a bottleneck for pipeline processing making it difficult to raise the frequency and increase the performance. The V850 microcontrollers avoid this problem by supporting only simple addressing.



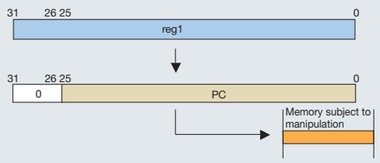
Addressing modes

● Instruction addresses

• Relative addressing (PC dependent)
Add 9 signed bits or 22 signed bits of data of the instruction code to the program counter.



• Register addressing (register indirect)
Transfer the contents of the general-purpose register specified by the instruction (reg1) to the program counter (PC).

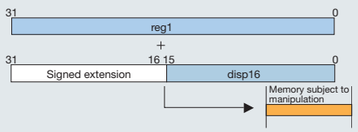


● Operand addresses

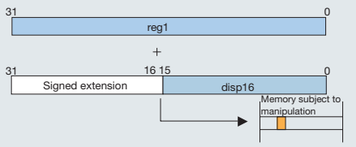
• Register addressing
Addressing that accesses the general-purpose register specified by the general-purpose specification field or a system register as an operand.

• Immediate addressing
Addressing of 5-bit data or 16-bit data for manipulation in the instruction code.

• Based addressing
Addressing that accesses memory, with the sum of the contents of the general-purpose register (reg1) and 16-bit displacement (disp16) used as the operand address.



• Bit addressing
Addressing that accesses 1 bit of 1 byte of the memory space, with the sum of the contents of the general-purpose register (reg1) and 16-bit displacement (disp16) that has been sign extended to word length used as the operand address.

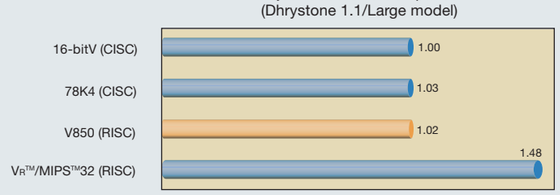


2-byte basic instruction set

The V850 microcontrollers employ a 2-byte instruction code to perform basic processing to enable compact program development equivalent to 16-bit CISC microcontrollers.

- Improved object efficiency through ROMization programming
  Application of 2-byte instructions to all basic processing, consisting of load, store, arithmetic/logic operations, and branching.
- To realize ease of use, restrictions on 16-bit fixed-length instructions are partially removed through the incorporation of 32-bit instructions.
- Bit manipulation instructions, etc., are available.

Object Code Size Comparison
(Dhrystone 1.1/Large model)



CISC-like instructions for embedding (bit manipulation instructions)

The V850 microcontrollers support bit manipulation instructions ideal for manipulating the flags in I/O registers, which play a large role in embedding control.

- Improvement of operability of memory mapped I/O devices for control applications
- Manipulation of any 1 bit of byte data in the memory space
- Provision of test (tst1)/set (set1)/clear (clr1)/invert (not1) instructions
- Effective for reducing object size and execution time since flags can be manipulated in 1-bit units using 1 instruction

Example: Setting bit 6 of ASIM00 register to 1

Item \ Bit Manipulation Instruction	When Used	When Not Used	
Coding example	set1 6, ASIM00[r0]	ld.b ASIM00[r0], r20 ori 0x0040, r20, r20 st.b r20, ASIM00[r0]	add -4, sp st.w r20, 0[sp]] Save r20 ld.b ASIM00[r0], r20 ori 0x0040, r20, r20 st.b r20, ASIM00[r0] ld.w 0[sp], r20 add 4, sp] Restore r20
Object size	4 bytes	12 bytes	24 bytes
Execution time	4 clock cycles	4 clock cycles	8 clock cycles

Multi-status flags

In the V850 microcontrollers, calculation results are reflected in registers as status flags. As a result, the delay branching that can occur in the RISC microcontrollers of other manufacturers does not occur and programs can be coded with the same feel as CISC microcontrollers.

- Easy coding using an assembler
- Improved object efficiency and execution speed

ZERO: Zero processing
PLUS: Positive processing
MINUS: Negative processing

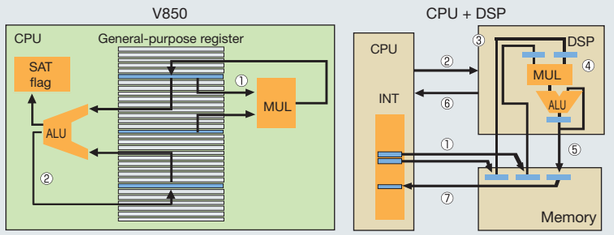
Example: Program that branches to positive/negative/zero according to register contents

CISC Microcontroller	V850	Other Manufacturers' RISC Microcontroller
cmp ax, 0 jz ZERO jgt PLUS jmp MINUS	cmp 0, r10 bz ZERO bgt PLUS br MINUS	cmp/eq #0, r10 bt ZERO cmp/pl r10 bt PLUS bra MINUS nop ;For delay branching

DSP function

The V850 microcontrollers provide a DSP function for executing high-speed multiplication and product-sum operations indispensable for digital signal processing such as image and speech processing.

- Direct data handling via general-purpose registers
- Realization of digital signal processing through general-purpose CPU
- High-speed 16-bit (V850, V850ES CPU) and 32-bit (V850E1 CPU) multiply/sum-of-products operations
  (Multiply: 1 to 2 clocks, sum-of-products: 3 clocks)
- Effective for filter operations and matrix operations for feedback calculations in speed, position, and other servo control.

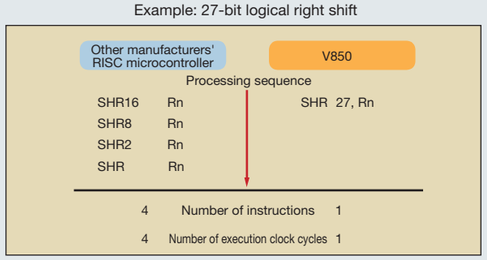


32-bit barrel shifter

The V850 microcontrollers can realize bit manipulations frequently used during signed data and image data processing using 1 instruction per clock cycle.

- Shifting of any number of bits (0 to 31) executable in 1 instruction per clock cycle
  Improved execution speed and object efficiency
  Effective for extracting arbitrary bit lengths of image data and signed data (extracting code during MH/MR/MMR encoding, etc.)

Example: 27-bit logical right shift



V850E1, V850ES Architecture

The V850E1 and V850ES CPUs achieve high performance and higher code efficiency through the implementation of the following improvements to the V850 CPU.

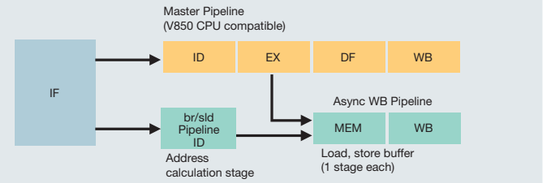
Non-blocking load/store
- Improved bus use efficiency
- Shorter interrupt insensitivity period

Addition of branch/load pipes
- 2-clock branching
- Parallel execution of instructions

Shift to 3-operand manipulations in 1 slot
- Improved absolute performance
- Example: Synchronous processing of mov + add

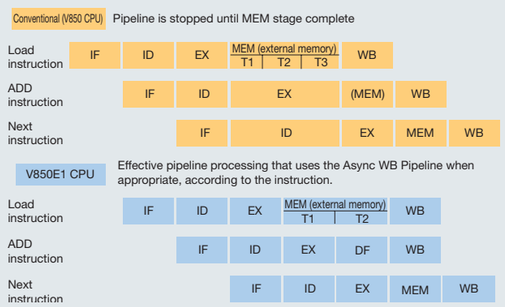
Addition of high-level language-compatible instructions
- Improved code efficiency
- 10 to 15% improvement in object efficiency when C compiler used

● Pipeline configuration



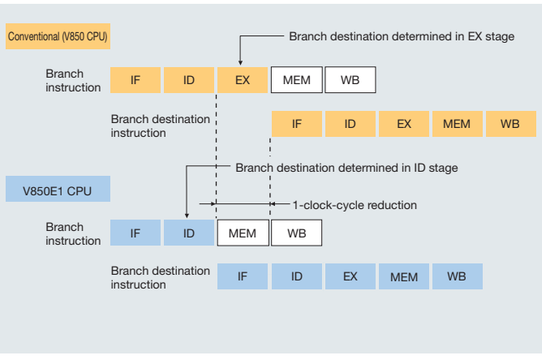
IF (Instruction fetch): Fetches instructions and increments the fetch pointer.
ID (Instruction decode): Decodes instructions, creates immediate data, and reads registers.
EX (ALU, multiplier, barrel shifter execution): Executes decoded instructions.
MEM (Memory access): Accesses memory of corresponding addresses.
WB (Writeback): Writes execution results to registers.
DF (Data fetch): Transfers execution data to WB stage.

● Non-blocking load/store

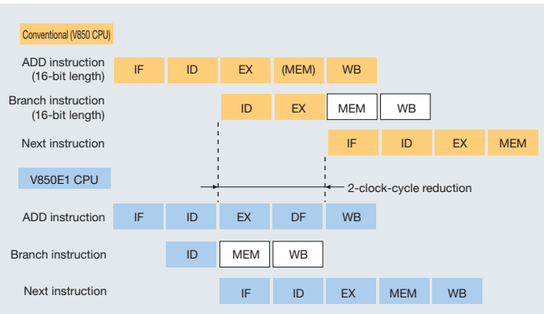


● Addition of branch/load pipes

• Pipeline operation with branch instruction

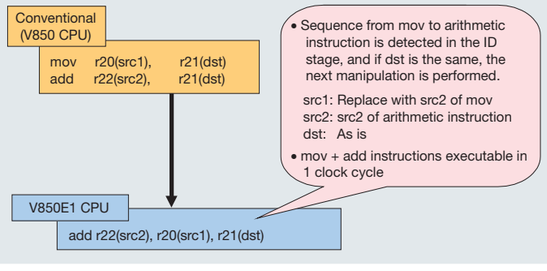


• Parallel instruction execution (when executed by internal ROM)



* The next branch instruction code is also fetched due to the internal 32-bit bus.

● Shift to 3-operand manipulations in 1 slot



● Addition of high-level language compatible instructions

The V850E1 and V850ES CPUs have enhanced the instruction set of the V850 CPU as follows.

◆ switch (2 bytes)
- C language switch statement processing converted into instruction

◆ callt (2 bytes)/ctret (4 bytes)
- Table-reference branching
- Reducing size of call code that frequently appears

◆ Data conversion instructions (2 bytes)
- char, short type cast executed using 1 instruction
- sxh, sxb, zxb, and zxh instructions

◆ prepare/dispose (4 bytes)
- Function start/end processing executed using 1 instruction

◆ unsigned Load
- Reduction of unsigned manipulation code

◆ mov imm32, reg (6 bytes/2 clock cycles)
- Reduction of address setting code

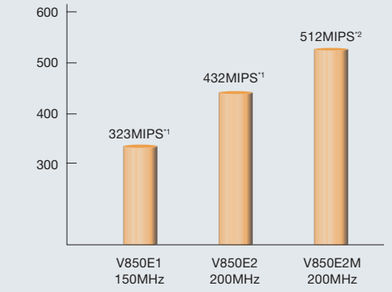
◆ mul/mulu (4 bytes)
- Reduction of array address calculation
- Improvement of sum-of-products performance

◆ Other
- Bit manipulation (register indirect bit specification)
- cmov (conditional move), divide (div/divu/divhu)
- sasf, endian conversion

V850E2, V850E2M Architecture

V850E2, V850E2M CPU features

◆ V850E2M high-performance CPU core: 512 MIPS @ 200 MHz
Improved internal architecture for performance 1.6 times that the of the E1 and 1.2 that of the E2



◆ Backward instruction compatibility with V850E1, V850ES and V850E2 CPUs at object level

◆ 7-stage pipeline
- Execution cycle optimization (V850E2M)
  Eliminates flag hazards and speeds up conditional branching.

◆ Improved interrupt functions

	V850E1	V850E2	V850E2M
Channels	117	117	256
Priority	8 levels	8 levels	16 levels

◆ Processor protection functions (V850E2M)
- System register protection
- Memory protection
- Peripheral device protection
- Timing monitoring

The above four functions detect or inhibit illegal use of system resources and improper monopolization of CPU execution time.

◆ Support of expanding application software sizes
- Address space (program/data) expansion
- Strengthened cache memory support

V850E2, V850E2M CPU main added functions

◆ High-speed division instructions (V850E2M)
- Variable-step division instructions added for high-speed calculation.

◆ Single-precision and double-precision floating-point instructions (V850E2M)
- Compliant with IEEE 754-1985

◆ 32-bit relative branch instruction
- Support of program space expansion
- Long-distance branching performance, elimination of code efficiency losses

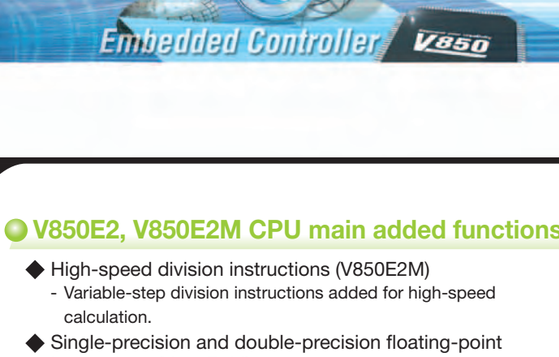
◆ 3-operand instructions (addition of target operations)
- Higher speed processing of operations such as multiplex add/subtract (64-bit operation, saturate operation) and bit shift.

◆ Sum-of-products instruction
- Higher speed 32-bit sum-of-products operation
  (32 × 32 + 64 → 64 bits)

◆ Bit search instruction
- Bit row change point search for run length measurement, contributing to increased speed of conversion from integers to floating-point values, etc.

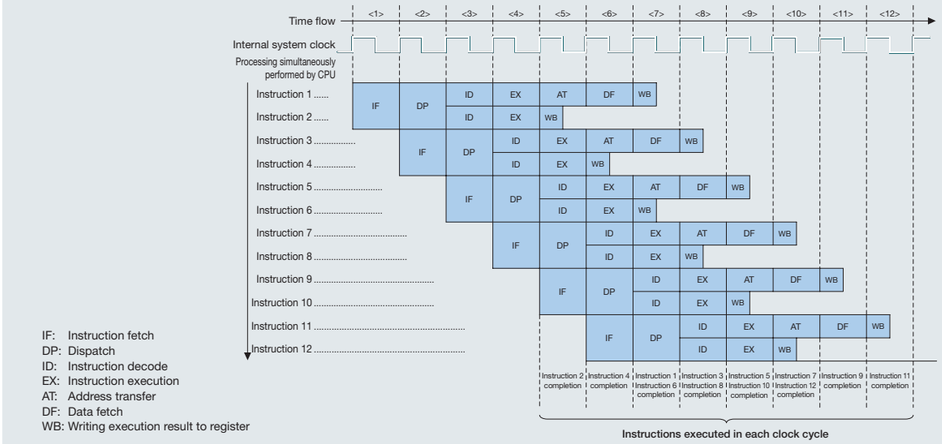
V850E2, V850E2M CPU pipeline configuration

2 instructions can be executed by simultaneously using 2 instruction execution units



V850E2, V850E2M CPU pipeline operation

Execution of up to 2 instructions/clock possible (dependent on instruction sequence)



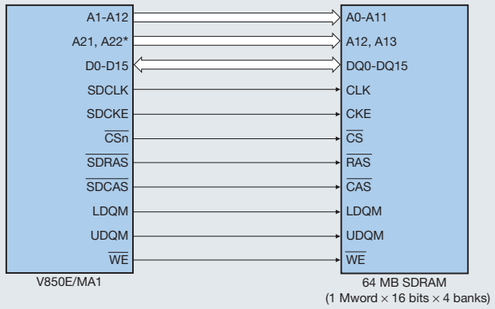
IF: Instruction fetch
DP: Dispatch
ID: Instruction decode
EX: Instruction execution
AT: Address transfer
DF: Data fetch
WB: Writing execution result to register

Memory Access

SDRAM controller

Products: V850E/MA3, ME2, V850E2/ME3

- SDRAM connectable without external circuit
- CAS latency: 2, 3 supported
- CBR (automatic) refresh: Self refresh supported

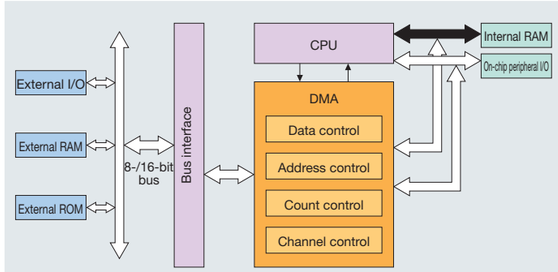


* The address signal used differs depending on the SDRAM product.

DMA controller (provided in V850E, V850ES products)

Products: V850E/MA3, IA1, IA2, IA3, IA4, IF3, IG3, Ix4, Ix4-H, ME2, DJ3, DL3, Sx3-H, V850ES/Sx2, Sx2-H, Sx3, FG2, FJ2, Fx3, Jx3, Jx3-E, Jx3-L, Jx3-H, Jx3-U, Hx3 V850E2/MN4, ML4, ME3, Fx4-L, Fx4, Fx4-M, Fx4-G, Fx4-H, Sx4-H

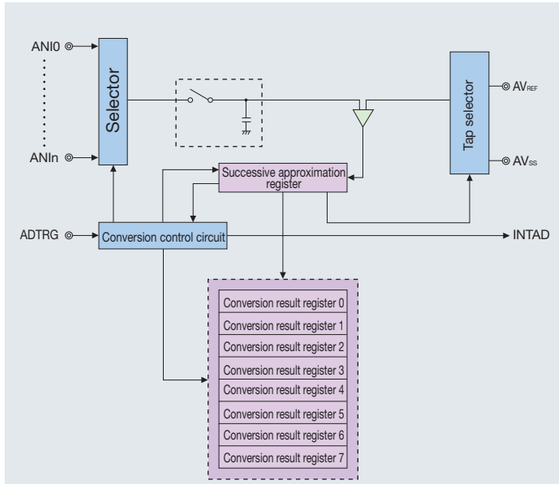
- Transfer targets: Memory-peripheral I/O, memory-memory
- Transfer mode: Single, single step (some products only), block transfer (some products only)
- Transfer units: 8/16 bits (8/16/32 bits for V850E/DL3, Ix4, Ix4-H)
  : 8/16/32 bits (V850E2/Fx4-L, Fx4-G)
  : 8/16/32/128 bits (V850E2/MN4, Fx4, Fx4-M, Fx4-H, Sx4-H)
- Transfer type: 1-cycle transfer (some products only), 2-cycle transfer
- Number of transfers: 65536 max.



10-bit A/D converter (multi-stage buffer type)

Products: V850E/MA3, ME2, IA1, IA2 V850ES/Jx3, Hx3, etc.

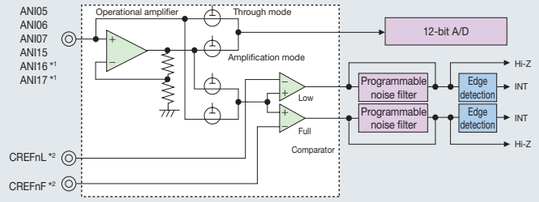
- Conversion startable by software or hardware
- Select/scan mode switching possible



Operational amplifier, comparator

Products: V850E/IF3, IG3, Ix4, Ix4-H

- Input voltage settable in range of 2.5 times to 10 times
- Overcurrent detectable at positive and negative sides
- Timer output pin settable to high impedance after detection of overcurrent



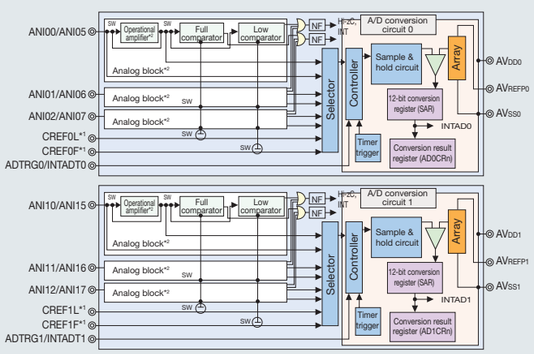
*1. These pins are not included in the V850E/IF3.
*2. In the V850E/Ix4 and Ix4-H, the comparator reference voltage is generated by the on-chip D/A converter.

Analog Circuits

12-bit multifunction A/D converter

Products: V850E/IF3, IG3, Ix4, Ix4-H

- Simultaneous 12-bit A/D converter sampling of 2 circuits
- On-chip operational amplifier (×2.5 to ×10) for input level amplification
- On-chip overvoltage detection comparator

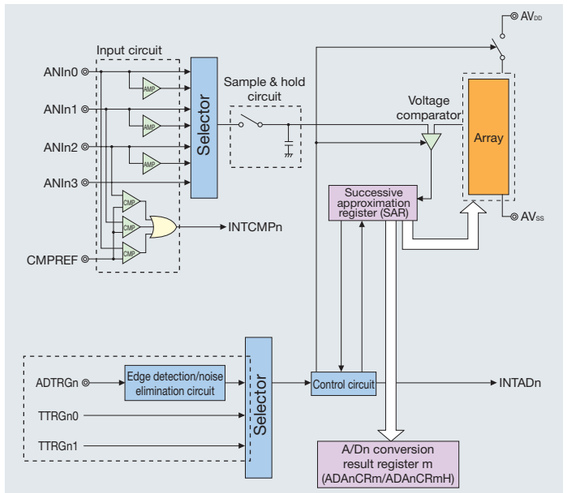


*1. In the V850E/Ix4 and Ix4-H, the comparator reference voltage is generated by the on-chip D/A converter.
*2. The V850E/IF3 and IG3 have four on-chip analog blocks.

10-bit multifunction A/D converter

Products: V850E/IA3, IA4 V850ES/IK1, IE2

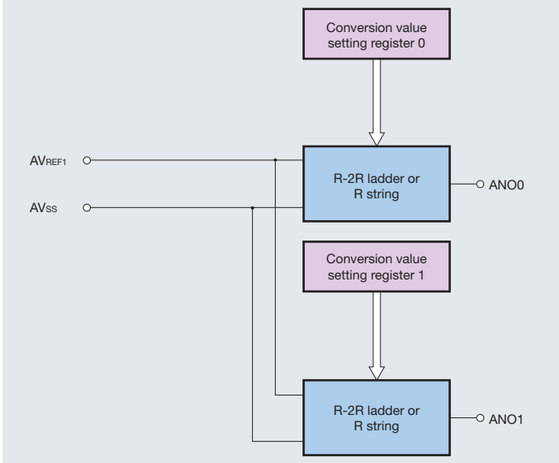
- Simultaneous 10-bit A/D converter sampling of 2 circuits
- On-chip operational amplifier (×2.5/×5) for input level amplification (IA3, IA4 only)
- On-chip overvoltage detection comparator (IA3, IA4 only)



D/A converter

Products: V850E/MA3, Sx3-H V850ES/Sx2, Sx2-H, Sx3, Jx3, Jx3-H, Jx3-L (except for the 40-pin version), Jx3-U

- R-2R ladder method
- 8-bit resolution
- Operation mode: Normal mode/real-time output mode

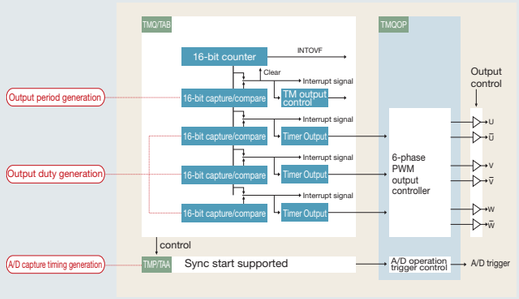


Timer/Counter

Timer configuration during inverter control

Products: V850E/IA3, IA4, IF3, IG3, Ix4, Ix4-H, MA3
V850ES/IK1, IE2, Fx3, Hx3

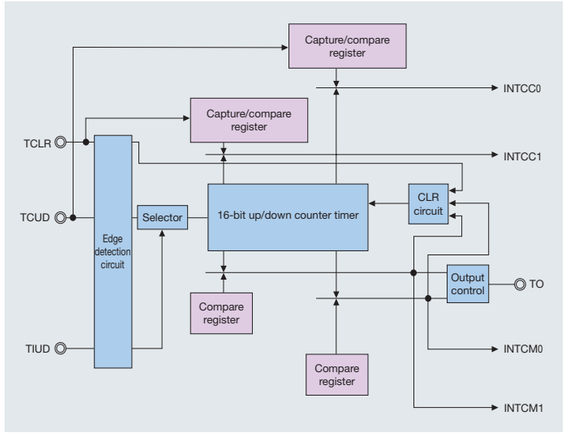
- 0% and 100% output and 6-phase PWM output with deadtime possible
- Switchable anytime/batch overwrite for compare register
- A/D converter conversion start trigger generator



Up/down counter

Products: V850E/IA1, IA2, IA3, IA4, Ix3, Ix4, Ix4-H, MA3, ME2
V850E2/ME3, V850ES/Jx3-E, Jx3-H, Jx3-U

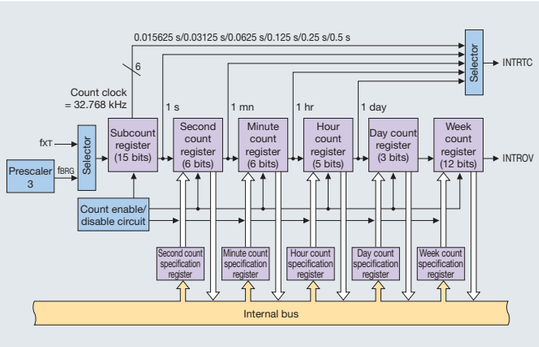
- 16-bit 2-phase encoder input possible
- Compare registers: 2
  Capture/compare registers: 2



Real-time counter

Products: V850E/Sx3-H
V850ES/SA2, SA3, Jx3-E, Jx3-H, Jx3-U

- On-chip week, day, hour, minute, second counters
- Counting up to 4095 periods
- Support of interval interrupt generation at fixed intervals selectable from: 0.015625 s, 0.03125 s, 0.0625 s, 0.125 s, 0.25 s, 0.5 s, 1 s, 1 mn, 1 hr, 1 day

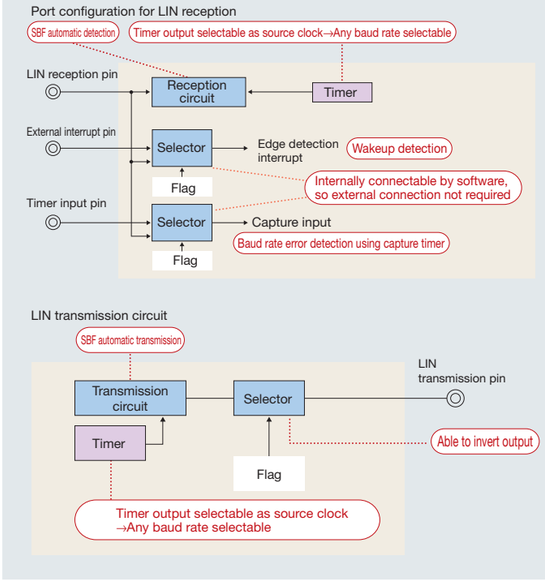


Serial Interface

LINBus

Products: V850ES/Sx2, Sx2-H, Sx3, Jx3, Jx3-E, Jx3-H, Jx3-L, Jx3-U, Hx3,
V850ES/Fx2, Fx3, Fx3-L,
V850E/Dx3

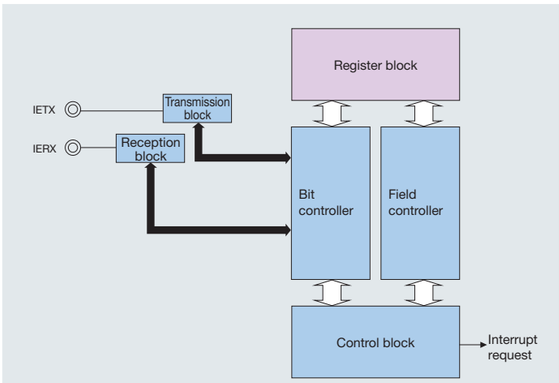
- Low-cost 1-wire network bus
- Sync break field (SBF) send/receive possible using hardware
  (Send: 13 bits ≤ SBF ≤ 20 bits; Receive: SBF ≥ 11 bits)
- Also generally usable as UART



IEBus controller

Products: V850ES/SG1, Sx2, Sx2-H, Sx3, V850E/Sx3-H,
V850E2/Sx4-H

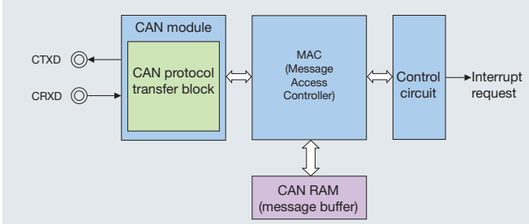
- Communication mode 1 supported
- Max. transfer bytes: 32 bytes/frame
- Max. transfer speed: Approx. 26 kbps



CAN

Products: V850E/IA1, Dx3, Sx3-H
V850ES/Sx2, Sx2-H, Sx3, Fx2, Fx3, Fx3-L, Jx3-E, Jx3-H
V850E2/Fx4-L, Fx4, Fx4-M, Fx4-H, Fx4-G, MN4, ML4, Sx4-H

- CAN protocol ver. 2.0 Part B (send/receive of standard and extended frames)
- Max. transfer rate: 1 Mbps
- 32 message buffer

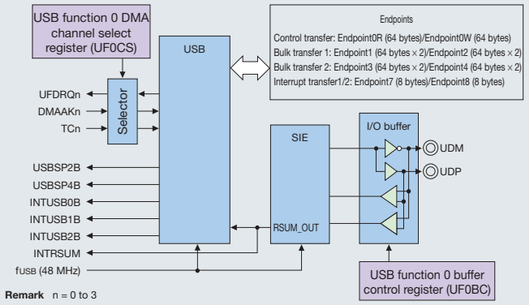


Other

USB

Products: V850E/IG4-H, IH4-H, ME2
V850E2/ME3, MN4, ML4

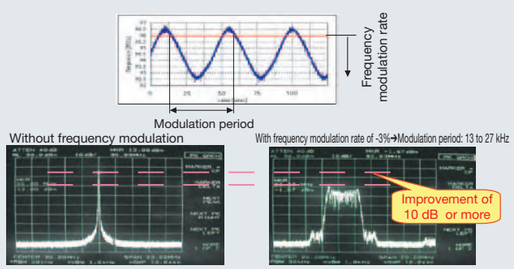
- Compliant with Universal Serial Bus Specification
- Support of 12 Mbps (full speed) transfer
- Many endpoint configurations



SSCG *(Spread spectrum frequency synthesizer clock generator)*

Products: V850E/ME2, Dx3, Sx3-H, V850ES/Hx3, Fx3
V850E2/ME3

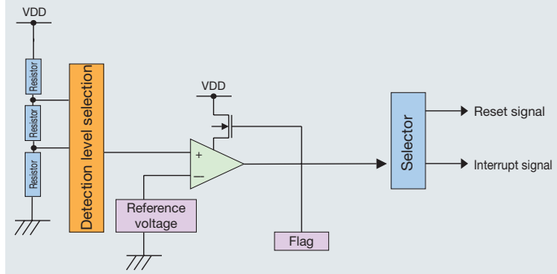
- EMI peak noise reduction through input frequency modulation
- Large reduction in noise countermeasure time and cost possible
- Frequency modulation rate and modulation period changeable by register setting



Low-voltage detector (LVI)

Products: V850E/IF3, IG3, Ix4, Ix4-H, Sx3-H
V850ES/Sx2, Sx3, Fx2, Fx3, Fx3-L, Jx3, Jx3-E, Jx3-H, Jx3-L, Jx3-U, Hx3, IK1, IE2
V850E2/Fx4-L, Fx4, Fx4-M, Fx4-H, Fx4-G, Sx4-H

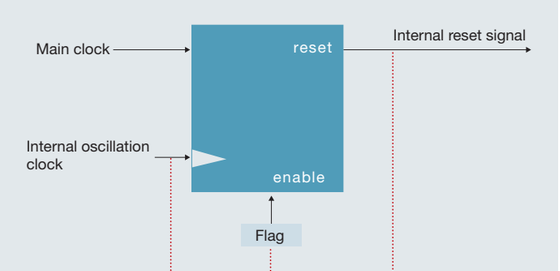
- Detection voltage level changeable by using software
- Can be used in place of reset IC, lowering system costs
- Detection voltage not changeable after mode transition (security protection)



Clock monitor

Products: V850E/IA3, IA4, IF3, IG3, Ix4, Ix4-H, Dx3, Sx3-H
V850ES/SG1, Sx2, Sx2-H, Sx3, Fx2, Fx3, Fx3-L, Jx3, Jx3-E, Jx3-H, Jx3-L, Jx3-U, Hx3, IK1, IE2
V850E2/Fx4-L, Fx4, Fx4-M, Fx4-H, Fx4-G, Sx4-H

- Monitors abnormal stops of main clock by using internal oscillator
- During abnormal stop, entire system can be set to reset status
- Prevention of damage due to system deadlock or program loop

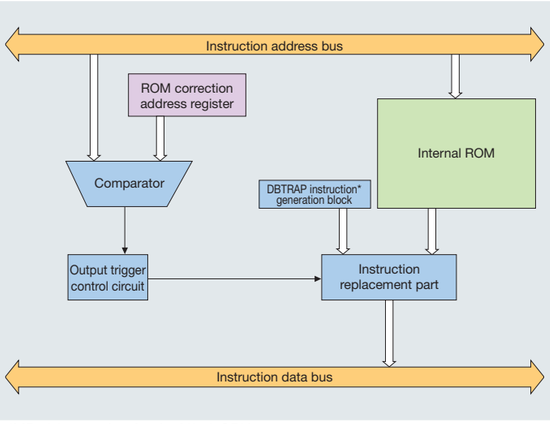


ROM correction

Products: V850E/MA3, IA3, IA4, Dx3, Sx3-H
V850ES/SG1, Sx2, Sx2-H, Sx3, IK1

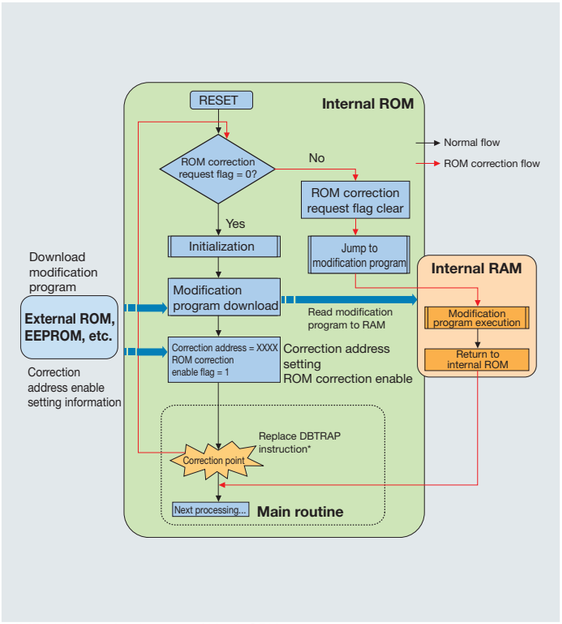
- Instructions of address to be modified inserted to replace DBTRAP instruction (JMP r0 instruction in case of V850 CPU), branching to 0060H (0000H in case of V850 CPU)
- Program modification following switch to mask ROM possible
- Modified addresses: 4 points, 8 points*

* V850E/DJ3, Sx3-H



* JMP r0 instruction for the V850 CPU

Explanation of ROM correction operation



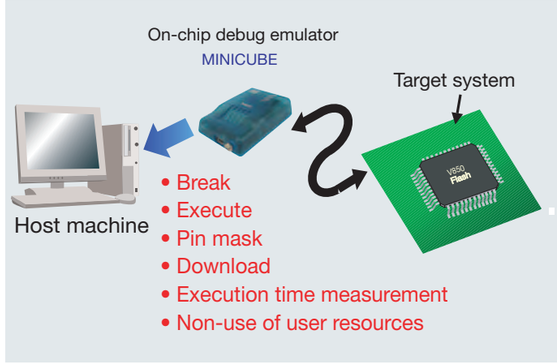
* JMP r0 instruction in case of V850 CPU

On-chip debugger

Products: V850E2/MN4, ML4, ME3*1 , Fx4-L, Fx4, Fx4-M, Fx4-H, Fx4-G, Sx4-H
V850E/ME2*2 , MA3, IA4, IG3, Ix4, Ix4-H, DJ3, DL3, Sx3-H
V850ES/Sx2, Sx2-H, Sx3, Fx2, Fx3, Fx3-L, Jx3, Jx3-E, Jx3-H, Jx3-L, Jx3-U, Hx3

- Realization of on-chip debugging of microcontroller with DCU (debug control unit)
- Compact and low-cost on-chip emulator
- Downloading
- Integrated debugger (ID850QB) supported

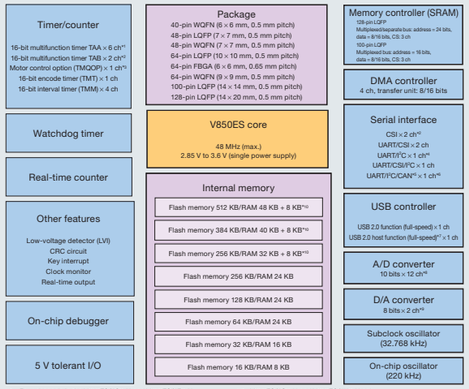
*1. Tracing is possible by using the RTE-2000-TP made by Midas Lab Co., Ltd.
*2. Tracing is possible by using the RTE-2000-TP made by Midas Lab Co., Ltd., or PARTNER-ET II, PARTNER-J made by Kyoto Micro Computer Co., Ltd.



All Flash 32-bit USB MCU (V850ES/Jx3-H, V850ES/Jx3-U)

Overview

- High-performance CPU: 98 MIPS @ 48 MHz
- USB 2.0 compliant
  Built-in USB 2.0 function (full-speed) and USB 2.0 host (full-speed)* controller
  * V850ES/JG3-U and V850ES/JH3-U only
- Extensive peripheral features
  Backward-compatible with V850ES/Jx3.
  Additional motor control capability and real-time counter available.



*1. Four channels in the V850ES/JC3-H and V850ES/JE3-H.
*2. One channel in the V850ES/JC3-H and V850ES/JE3-H.
*3. Not included in the V850ES/JC3-H.
*4. Not included in the V850ES/JC3-H and V850ES/JE3-H.
*5. μPD70F3819 (V850ES/JC3-H), 70F3825 (V850ES/JE3-H), 70F3770 (V850ES/JG3-H), and 70F3771 (V850ES/JH3-H) only
*6. Not included in the 40-pin WQFN package.
*7. V850ES/JG3-U and V850ES/JH3-U only
*8. Five channels in the 40-pin version of the V850ES/JC3-H, six channels in the 48-pin version of the V850ES/JC3-H, and ten channels in the V850ES/JE3-H.
*9. Not included in the 40-pin WQFN package. One channel in the 48-pin and 64-pin package.
*10. Data-only RAM

Overview of USB specifications

- Many USB-compliant features supported
- Products are USB certified

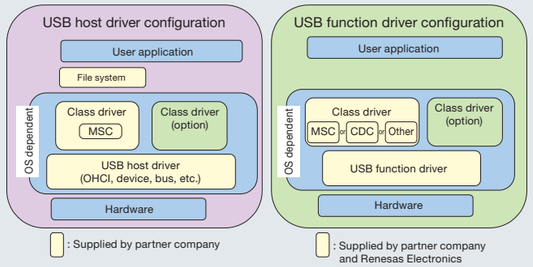
Features \ Generic Name		V850ES/Jx3-U	V850ES/Jx3-H
USB standard		USB 2.0 (full speed)	
USB function		1 ch	
USB host (OHCI)		1 ch	None
USB clock	Internal	External 6 MHz clock × Internal clock multiplied by 8 = 48 MHz	
	External	External clock input (fUSB) = 48 MHz	
USB host transfer mode		Control, Bulk, Interrupt, Isochronous	None
USB host features		PPON (USB power supply output) pin OCI (overcurrent detection input) pin	None
USB function endpoint configuration		Control × 2 (64 bytes), Bulk × 4 (64 bytes × 2), Interrupt × 1 (8 bytes)	
External USB DMA capability*		DMA request (UDMARQn), DMA acknowledge (UDMAAKn) (n = 0, 1)	

* Assuming connection of μPD720150.

USB driver

- USB function driver
  Sample code supplied by Renesas Electronics free of charge.
  Driver software provided by a partner company*.
- USB host driver
  Driver software provided by a partner company*.

* Partner companies: Tepco Uquest, Ltd., Grape Systems Inc., Ubiquitous Corporation

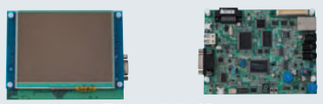


Starter kit

- Two types: one for USB host and one for USB function
- Provides development environment enabling system-level USB evaluation

Item \ USB Type	For USB Host	For USB Function
Part number	TK-850/JH3U-SP	TK-850/JG3H
Device mounted in	μPD70F3769 (V850ES/JH3-U)	μPD70F3760 (V850ES/JG3-H)
Main device features	512 KB flash memory, 48 KB + 8 KB RAM, USB 2.0 function, USB 2.0 host	256 KB flash memory, 32 KB + 8 KB RAM, USB 2.0 function
Main features included	LCD with touch panel function, Ethernet, IrDA, audio I/O, external memory (SRAM), RS-232C, expansion connectors, debug I/F	Debug I/F, 7-seg LED, DIP switch

Starter kit for USB host



TK-850/JH3U-SP
TESSERA Technology Inc.

Starter kit for USB function

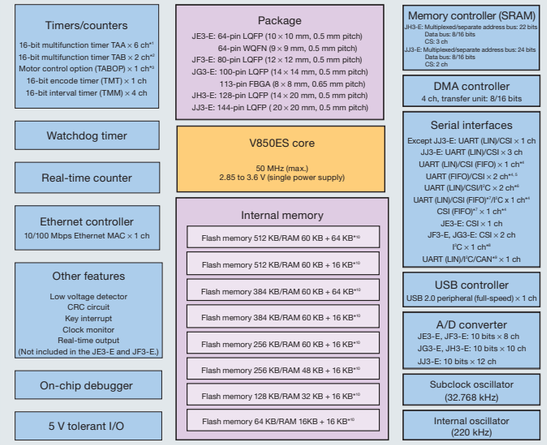
TK-850/JG3H
TESSERA Technology Inc.

All Flash 32-bit Ethernet Controller MCU (V850ES/Jx3-E)

Control your networks and systems using only the internal memory

- High-performance CPU of 103 MIPS @ 50 MHz
- Internal flash memory of up to 512 KB and RAM of up to 124 KB
- On-chip Ethernet controller
  On-chip 10/100 Mbps MAC eliminates the need to attach an external Ethernet controller

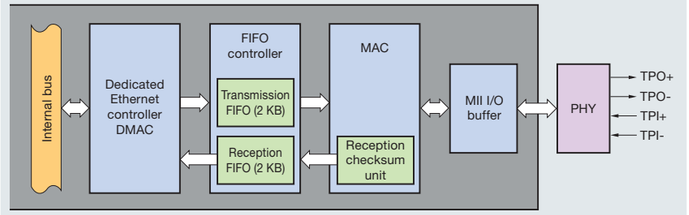
Block diagram



*1. Four channels in other than the V850ES/JH3-E and V850ES/JJ3-E.
*2. One channel in other than the V850ES/JH3-E and V850ES/JJ3-E.
*3. Not included in the V850ES/JE3-E.
*4. V850ES/JH3-E and V850ES/JJ3-E only
*5. One channel is assigned to two different pins.
*6. One channel in the V850ES/JE3-E.
*7. The same channel is assigned to two different pins.
*8. V850ES/JJ3-E only
*9. μPD70F3829 (V850ES/JE3-E), 70F3833 (V850ES/JF3-E), 70F3837 (V850ES/JG3-E), 70F3783 (V850ES/JH3-E), and 70F3786 (V850ES/JJ3-E) only
*10. Data-only RAM

On-chip Ethernet controller lets you build a low-cost system

- MAC
  - Enables IEEE802.3-compliant 10/100 Mbps full-duplex and half-duplex communication as well as flow control.
  - Uses MII as the physical layer device (PHY) interface
  - Includes an on-chip VLAN detector
- FIFO size: Transmission = 2 KB
  Reception = 2 KB
- Dedicated Ethernet controller DMAC
- On-chip reception checksum calculator compliant with RFC1071



Enhanced development environment and network software

- Evaluation kit that can be used for evaluation and development at the system level
- Network software in the form of a TCP/IP protocol stack
  Renesas Electronics provides a free TCP/IP protocol stack -- the Compact TCP/IP Library*.
  TCP/IP protocol stacks are also available from our partner companies.
  * Also includes web server and mail client software.

Evaluation kit

TK-850/JH3E+NET
(V850ES/JH3-E mounted)
Made by TESSERA Technology Inc.

TCP/IP protocol stacks provided by partner companies

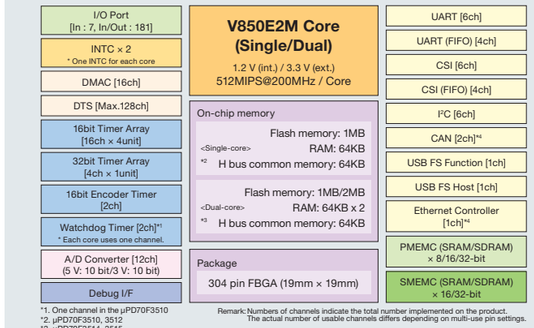
Partner	TCP/IP protocol stack
NEC Communication Systems	Qlism
Nissin Systems Co., Ltd.	USNetPlus
Zuken Elmic, Inc.	KASAGO
Data Technology Inc.	Cente
Ubiquitous Corporation	Ubiquitous TCP/IP

All Flash MCUs (V850E2/MN4) with 32-bit high-performance CPU cores

Overview of functions

- V850E2M high-performance CPU core: 512 MIPS @ 200 MHz
  Products with dual CPU cores achieve world-top-class performance of 1,024 MIPS when operating at 200 MHz.
- Large-capacity flash memory supporting high-speed access: Max. 2 MB
- Many on-chip peripheral functions
  Ethernet controller, USB Function/USB Host, and CAN

Block diagram



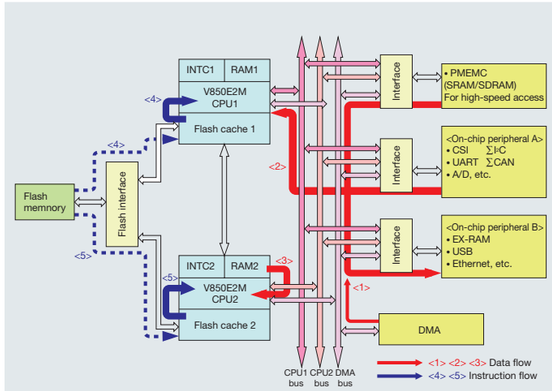
*1. One channel in the μPD70F3510
*2. μPD70F3510, 3512
*3. μPD70F3514, 3515
*4. Not included in the μPD70F3510

Remark: Numbers of channels indicate the total number implemented on the product.
The actual number of usable channels differs depending on multi-use pin settings.

Dual-Core CPUs block diagram

The V850E2/MN4 includes three high-speed internal buses to maximize the dual-core performance.
These buses allow various types of processing to be performed in parallel.
By maximizing the performance of each unit in this way, the overall performance can be dramatically improved.
Example of processing that can be performed in parallel:

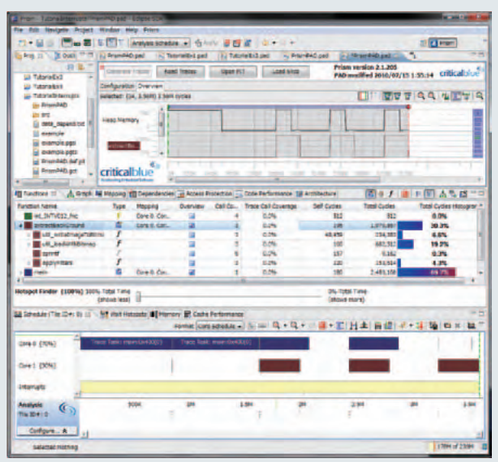
<1> Data is transferred at high speed from an external memory to an Ethernet peripheral by using DMA.
<2> CPU1 executes CAN communication protocol processing while processing other data at the same time.
<3> CPU2 processes the data from internal RAM2 while its high-performance CPU core executes high-speed calculations.
<4>, <5> CPU1 and CPU2 execute no-wait instruction fetches from the microcontroller's large-capacity flash memory using the flash cache in each core.



Rich development environment Introducing Prism*, a dynamic analysis tool for multi-core microcontrollers (V850E2/MN4)

Prism is an analysis and verification environment that provides software optimized for implementing multi-core architecture. Prism provides virtual task division, core assignment, and data-dependent display features that allow software engineers to easily develop and realize the full potential of multi-core processors without the need to change the source code.

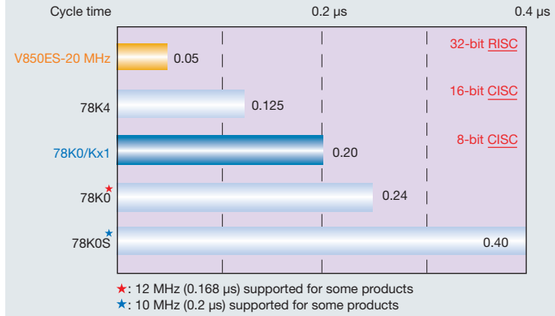
* Made by CriticalBlue, Inc



V850 Benchmark

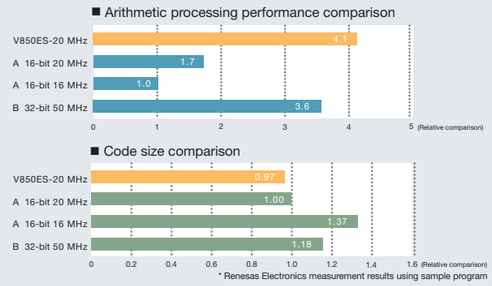
The V850 microcontrollers realize high speed, high performance, and high code efficiency.

Minimum instruction execution time



★: 12 MHz (0.168 μs) supported for some products
★: 10 MHz (0.2 μs) supported for some products

V850 arithmetic processing performance and code size

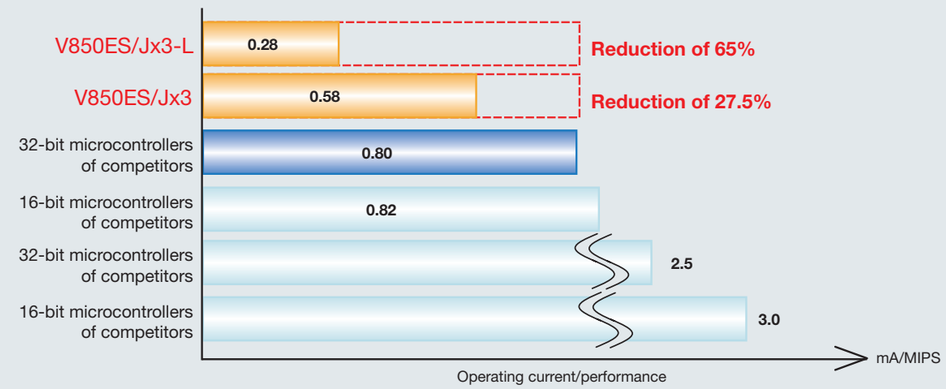


* Renesas Electronics measurement results using sample program

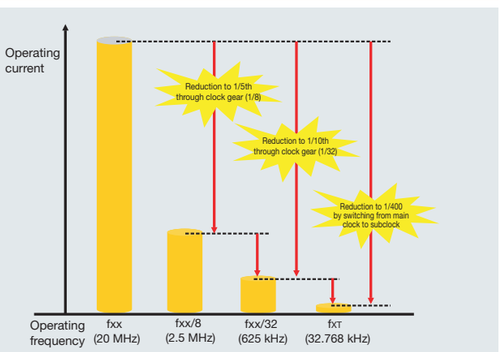
Low Power Consumption

Thanks to a thorough energy-saving design, the V850ES/Jx3-L attains a current/performance ratio of 0.28 mA/MIPS. As a result, compared with the 32- bit and 16-bit microcontrollers made by other manufacturers and having equivalent performances, the power consumption is reduced by over 65%.
Lower system power consumption and higher system performance are simultaneously achieved through the V850's extremely high power performance.

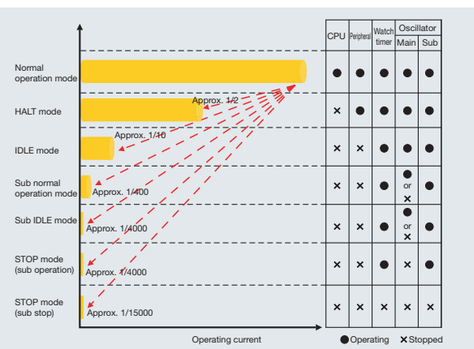
Power performance



Clock gear feature



Standby mode



Solutions for V850

Renesas Electronics supports your product development by supplying various solutions, such as ASSPs intended for particular systems, middleware* for complicated processing, and peripheral devices* for special functions. These solutions can substantially shorten your development period and reduce your costs.

* Through close cooperation with our partner companies, Renesas Electronics offers many solutions consisting of not only our own products but also of products from partner companies.

Efficiently **rotating** motors

Speaking clearly

Showing clearly

Connecting easily

- **System control**
  Real-time control
  Precision control
- **User interface**
  Input via keyboard
  Notification by display
  Notification by sound
- **Networks**
  Communication within a system
  Communication between sets
  Communication with an external source

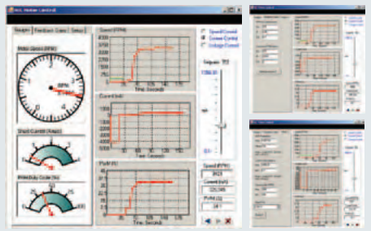
Rotating

Controlling a motor can be easily started by using a V850 ASSP for inverter control applications.
A brushless DC (BLDC) motor is also supplied, making this evaluation kit ideal for those who wish to rotate a motor.

Evaluation kit supporting "rotating" (low-voltage version motor starter kit*)

- **Features**
  - Speed display: 7-SEG LED 4
  - User interface: Push-button switch 4
    Variable resistor 1
  - PC interface: RS-232C 1
  - Safety: Isolation by photocoupler
    Overcurrent detection signal
  - Control signal: U-/V-/W-phase voltage
    U-/V-/W-phase current
    BEMF signal by comparator
  - Parameter display by GUI
  - System power supply: 15 V
- **Target devices**
  V850ES/IE2, V850ES/IK1, V850E/IG3
- **Sample programs (to be released)**
  Sample programs for 120-degree excitation mode BLDC motors (Hall sensor/sensor-less) and 180-degree excitation mode BLDC motors (Hall sensor) will be made available.

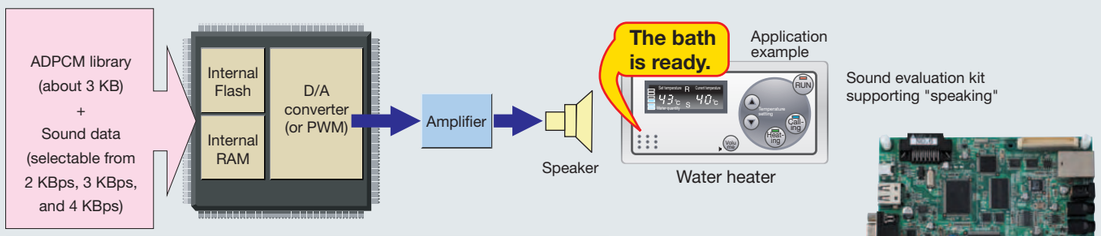
Low-voltage version motor starter kit*
By Renesas Electronics



* For details and purchasing, consult a Renesas Electronics sales representative or distributor.

Speaking

System control and sound function to compress and decompress sounds via software can be achieved by using a single chip.



Size of library		Processing performance (at 20 MHz)*	
ROM	RAM	Compression	Decompression
3 KB	32 bytes	15 µs max.	12 µs max.

* Processing is necessary every 125 µs in the case of 8 kHz sampling sound.

Sound evaluation kit supporting "speaking"

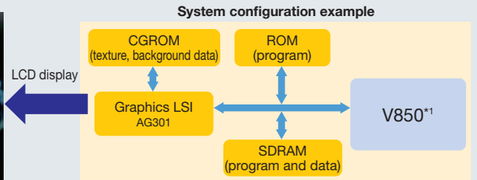
TK-850/JH3U-SP
(with V850ES/JH3-U)
Made by TESSERA Technology Inc.

Showing

"Showing" solutions are available, depending on the performance of the CPU.
A solution of 3D graphics using a high-performance V850E2/ME3 is also proposed.

High-end "showing" solution

- **3D graphics solution using high-end V850+MascotCapsule™**
  MascotCapsule, which enjoys a well-deserved reputation as a 3D drawing engine for cellular phones, can be used with an embedded microcontroller to realize 3D graphics.
  - High-end V850 and advanced MascotCapsule produce low-cost but expression-rich 3D graphics.
  - All leading plug-in 3D creation tools are supported, so that high-quality 3D contents can be developed easily.



*1. The µPD760110, which is pin-compatible with the V850E2/ME3, is available and is provided with a license for MascotCapsule, which is to be used with the AG3 (V850). For details, consult a Renesas Electronics sales representative or distributor.
*2. AG301 is a graphics LSI made by Axel Company.

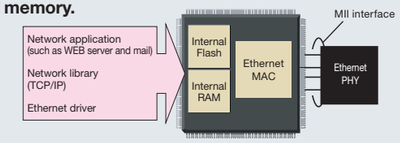
Connecting

Renesas Electronics provides “connecting” solutions using a wide range of network media such as Ethernet and CAN.

Ethernet solution

The V850ES/JH3-E and V850ES/JJ3-E feature an on-chip Ethernet MAC, deliver a high performance of 103 MIPS at a clock speed of 50 MHz, and provide the large-capacity RAM required for network control applications.
These microcontrollers enable single-chip control of networks and systems, allowing you to build low-cost networks in a range of fields such as remote monitoring and production line control.

"Connecting" is achieved by a simple configuration that does not require external memory.



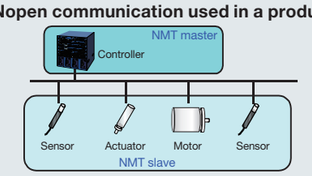
Evaluation kit for the Ethernet solution

TK-850/JH3E+NET
(V850ES/JH3-E mounted)
Made by TESSERA Technology Inc.

CAN solution

Renesas Electronics provides an extensive CAN microcontroller lineup together with a CAN protocol stack for industrial applications, including protocols such as CANopen and DeviceNet (supplied by NSD Co., Ltd., as DNGS for V850), helping you develop networks for industrial equipment more efficiently.

Example of CANopen communication used in a production line system



Remark NMT: Network management

Evaluation kit for CAN solution

CEB-V850ES/FJ3
(V850ES/FJ3 mounted)
Made by Cosmo Co., Ltd.

Features

To reduce your development time and improve maintenance after shipping, Renesas Electronics offers V850 microcontrollers with on-chip flash memory from 16 KB to 2048 KB. Our flash memory microcontrollers offer the following features:

- ◆ Flash capacity
  16 to 2048 KB
- ◆ Overwrite unit
  Entire memory at one time, or block units
- ◆ Rewrite method
  Serial communication using dedicated flash memory programmer (on-board, off-board)
  Self-flash programming
- ◆ Rewrite voltage
  Single-power-supply flash: Operating voltage
  Dual-power-supply flash: Operating voltage 7.8 V
- ◆ Rewrite count: 100/1,000/20,000 times

Rewrite Modes

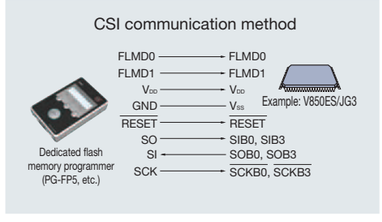
So that you can use the same microcontroller from development to mass production and maintenance, our V850 microcontrollers provide a programmer rewrite mode that uses serial communication to enable on-board programming, as well as a self-programming mode that enables the flash memory to be rewritten by using a user-created program:

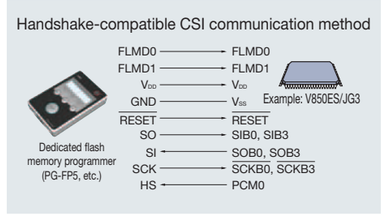
- ◆ On-board programming mode
  This programming mode is used to rewrite the flash memory mounted on the target system using a dedicated flash memory programmer.
- ◆ Off-board programming mode
  This programming mode is used to rewrite the flash memory using a dedicated flash memory programmer and dedicated program adapter (FA Series*1).
- ◆ Self-programming mode
  This programming mode is used to rewrite the flash memory by executing a user-created program written beforehand to the flash memory by using on-board/off-board programming*2.

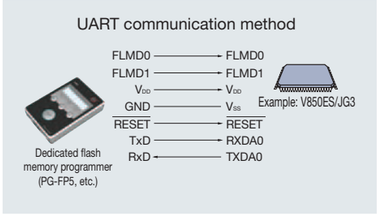
*1. The FA Series is a product of Naito Densei Machida Mfg. Co., Ltd.

2. Since instruction fetch and data access cannot be performed from the internal flash memory area during self-programming, a program for rewriting the internal RAM or external memory must be transferred in advance.

Programming using programmer (on-board/off-board)

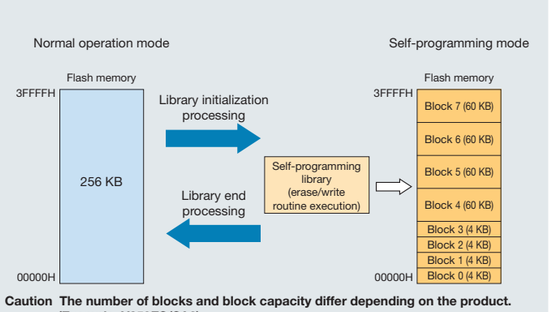






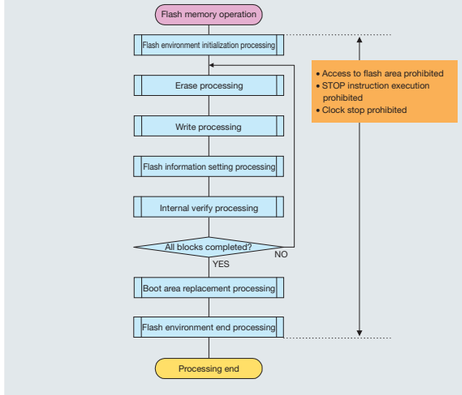
Self-programming mode (single-power-supply method)

The flash memory can be erased and rewritten using a self-programming library in a program placed in an area outside the flash memory.



Caution The number of blocks and block capacity differ depending on the product. (Example: V850ES/SA2)

Self-programming flow



Flash Specification List

CPU	Product	Max. Operating Frequency	Rewrite Voltage		Rewrite Mode				Rewrite Count (Times)
					On-Board/Off-Board Programming			Self-Programming	
			VDD	VPP	CSI	UART	CSI+HS		
V850E	V850E/MA3	80 MHz	2.3 V to 2.7 V (internal), 3.0 V to 3.6 V (external)	–	√	√	√	√	100
	V850E/IG4, IH4	100 MHz	1.35 V to 1.65 V (internal), 4.0 V to 5.5 V (external)	–	√	√	√	√	100
	V850E/IG4-H, IH4-H	100 MHz	1.35 V to 1.65 V (internal), 4.0 V to 5.5 V (external)	–	√	√	√	√	100
	V850E/IF3, IG3	64 MHz	3.5 V to 5.5 V	–	√	√	√	√	100
	V850E/IA3, IA4	64 MHz	2.3 V to 2.7 V (internal), 4.5 V to 5.5 V (external)	–	√	√	√	√	100
	V850E/IA2	40 MHz	4.5 V to 5.5 V (using regulator)	7.8 V	√	√	√	–	100
	V850E/IA1	50 MHz	3.0 V to 3.6 V (internal), 4.5 V to 5.5 V (external)	7.8 V	√	√	√	–	100
	V850E/DG3	16 MHz	4.0 V to 5.5 V	–	√	√	√	√	100
	V850E/DJ3	64 MHz/32 MHz	4.0 V to 5.5 V	–	√	√	√	√	100
	V850E/DL3	64 MHz	4.0 V to 5.5 V	–	√	√	√	√	100
	V850E/SJ3-H, SK3-H	48 MHz	2.85 V to 3.6 V	–	√	√	√	√	1000
V850ES	V850ES/HE3, HF3, HG3, HJ3	32 MHz	3.8 V to 5.5 V	–	√	√	√	√	1000
	V850ES/IE2	20 MHz	3.5 V to 5.5 V	–	√	√	√	√	100
	V850E/JE3-E, JF3-E, JG3-E, JH3-E, JJ3-E	50 MHz	2.85 V to 3.6 V	–	√	√	√	√	1000
	V850ES/JC3-H, JE3-H, JG3-H, JH3-H, JG3-U, JH3-U	48 MHz	2.85 V to 3.6 V	–	√	√	√	√	1000
	V850ES/JG3, JJ3	32 MHz	2.85 V to 3.6 V	–	√	√	√	√	1000
	V850ES/JC3-L, JE3-L, JF3-L, JG3-L	20 MHz	2.7 V to 3.6 V	–	√	√	√	√	1000
	V850ES/IK1	32 MHz	3.5 V to 5.5 V	–	√	√	√	√	100
	V850ES/FE3, FF3, FG3, FJ3, FK3	48 MHz/32 MHz	3.3 V to 5.5 V	–	√	√	√	√	1000
	V850ES/FE3-L, FF3-L, FG3-L	20 MHz	3.3 V to 5.5 V	–	√	√	√	√	1000
	V850ES/FE2, FF2, FG2, FJ2	20 MHz	3.5 V to 5.5 V	–	√	√	√	√	100
	V850ES/SG3, SJ3	32 MHz	3.0 V to 3.6 V	–	√	√	√	√	1000
	V850ES/SG2-H, SJ2-H	32 MHz	3.0 V to 3.6 V	–	√	√	√	√	100
	V850ES/SG2, SJ2	20 MHz	3.0 V to 3.6 V	–	√	√	√	√	100
V850E2	V850E2/MN4	200 MHz	1.1 V to 1.3 V (internal), 3.0 V to 3.6 V (external) 3.0 V to 3.6 V or 4.5 V to 5.5 V (analog)	–	√	√	√	√	100
	V850E2/ML4	200 MHz	1.1 V to 1.3 V (internal), 3.0 V to 3.6 V (external)	–	√	√	√	√	100
	V850E2/SG4-H, SJ4-H, SK4-H	160 MHz	1.1 V to 1.3 V (internal), 3.0 V to 3.6 V (external)	–	√	√	√	√	20000
	V850E2/FG4, FJ4, FK4, FL4	80 MHz	3.0 V to 5.5 V	–	√	√	√	√	100
	V850E2/FE4-L, FF4-L, FG4-L, FJ4-L, FK4-L	64 MHz/32 MHz	3.0 V to 5.5 V	–	√	√	√	√	1000
	V850E2/FL4-H	160 MHz	3.0 V to 5.5 V	–	√	√	√	√	100
	V850E2/FK4-G	80 MHz	3.0 V to 5.5 V	–	√	√	√	√	100
	V850E2/FE4-M, FF4-M	80 MHz	3.0 V to 5.5 V	–	√	√	√	√	100

Low-End Lineup (1/10)

5 V Operation

Generic Name		V850ES/HE3	V850ES/HF3
Part No.		μPD70F3747	μPD70F3750
CPU name		V850ES	V850ES
CPU performance (Dhrystone)		69 MIPS (@ 32 MHz)	69 MIPS (@ 32 MHz)
Internal ROM		128 KB (flash)	256 KB (flash)
Internal RAM		8 KB	16 KB
External bus interface	Bus type	–	–
	Address bus	–	–
	Data bus	–	–
	Chip select signal	–	–
Memory controller		–	–
Interrupt sources	Internal	43 (including one NMI)	43 (including one NMI)
	External	9 (9)* (including one NMI)	9 (9)* (including one NMI)
Timer/counter		16-bit timer/event counter (TAA) × 5 ch 16-bit timer/event counter (TAB) × 1 ch (3-phase inverter control PWM timer compatible) 16-bit interval timer (TMM) × 1 ch	16-bit timer/event counter (TAA) × 5 ch 16-bit timer/event counter (TAB) × 1 ch (3-phase inverter control PWM timer compatible) 16-bit interval timer (TMM) × 1 ch
Watchdog timer		1 ch	1 ch
Serial interface		CSI × 2 ch UART (LIN compatible) × 2 ch I^2C × 1 ch	CSI × 2 ch UART (LIN compatible) × 2 ch I^2C × 1 ch
A/D converter		10 bits × 10 ch	10 bits × 12 ch
D/A converter		–	–
DMA controller		4 ch	4 ch
Ports	I/O	51	67
	Input	–	–
Debug control unit		Provided (RUN/break)	Provided (RUN/break)
Other peripheral functions		3-phase inverter control, watch timer:1 ch, POC/LVI/clock monitor, RAM retention flag, SSCG	3-phase inverter control, watch timer: 1 ch, POC/LVI/clock monitor, RAM retention flag, SSCG
Operating frequency		When using main clock: 4 to 32 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz	When using main clock: 4 to 32 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz
Power supply voltage		3.7 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)	3.7 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)
Package		64-pin LQFP (10 × 10 mm)	80-pin LQFP (12 × 12 mm)
Operating ambient temperature		−40°C to +85°C	−40°C to +85°C

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850ES/HG3	V850ES/HJ3	
Part No.		μPD70F3752	μPD70F3755	μPD70F3757
CPU name		V850ES	V850ES	
CPU performance (Dhrystone)		69 MIPS (@ 32 MHz)	69 MIPS (@ 32 MHz)	66 MIPS (@ 32 MHz)
Internal ROM		256 KB (flash)	256 KB (flash)	512 KB (flash)
Internal RAM		16 KB	16 KB	32 KB
External bus interface	Bus type	–	Multiplexed	
	Address bus	–	16-bit	
	Data bus	–	8/16-bit	
	Chip select signal	–	4	
Memory controller		–	SRAM, etc.	
Interrupt sources	Internal	51 (including one NMI)	58 (including one NMI)	64 (including one NMI)
	External	12 (12)*1 (including one NMI)	16 (16)*1 (including one NMI)	
Timer/counter		16-bit timer/event counter (TAA) × 5 ch 16-bit timer/event counter (TAB) × 2 ch (3-phase inverter control PWM timer compatible) 16-bit interval timer (TMM) × 1 ch	16-bit timer/event counter (TAA) × 5 ch 16-bit timer/event counter (TAB) × 3 ch (3-phase inverter control PWM timer compatible) 16-bit interval timer (TMM) × 1 ch	
Watchdog timer		1 ch	1 ch	
Serial interface		CSI × 2 ch UART (LIN compatible) × 3 ch I^2C × 1 ch	CSI × 3 ch UART (LIN compatible) × 3 ch I^2C × 1 ch	CSI × 1 ch UART (LIN compatible) × 4 ch UART (LIN compatible)/CSI × 2 ch*2 UART (LIN compatible)/I^2C × 1 ch
A/D converter		10 bits × 16 ch	10 bits × 24 ch	
D/A converter		–	–	
DMA controller		4 ch	4 ch	
Ports	I/O	84	128	
	Input	–	–	
Debug control unit		Provided (RUN/break)	Provided (RUN/break)	
Other peripheral functions		3-phase inverter control, watch timer: 1 ch, POC/LVI/clock monitor, RAM retention flag, SSCG	3-phase inverter control, watch timer: 1 ch, POC/LVI/clock monitor, RAM retention flag, SSCG	
Operating frequency		When using main clock: 4 to 32 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz	When using main clock: 4 to 32 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz	
Power supply voltage		3.7 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)	3.7 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)	
Package		100-pin LQFP (14 × 14 mm)	144-pin LQFP (20 × 20 mm)	
Operating ambient temperature		−40°C to +85°C	−40°C to +85°C	

*1. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*2. Two channels identical to independent UART are available. The V850ES/HJ3 has a total of 6 UART channels.

Low-End Lineup (2/10)

3 V Operation

Generic Name		V850ES/JE3-E (Under development)				V850ES/JF3-E (Under development)			
Part No.		μPD70F3826	μPD70F3827	μPD70F3828	μPD70F3829	μPD70F3830	μPD70F3831	μPD70F3832	μPD70F3833
CPU name		V850ES				V850ES			
CPU performance (Dhrystone)		103 MIPS (@ 50 MHz)				103 MIPS (@ 50 MHz)			
Internal ROM		64 KB (flash)	128 KB (flash)	256 KB (flash)		64 KB (flash)	128 KB (flash)	256 KB (flash)	
Internal RAM		32 KB*1	48 KB*1	64 KB*1		32 KB*1	48 KB*1	64 KB*1	
External bus interface	Bus type	–				–			
	Address bus	–				–			
	Data bus	–				–			
	Chip select signal	–				–			
Memory controller		–				–			
Interrupt sources	Internal	62 (Including one NMI)			66 (Including one NMI)	66 (Including one NMI)			67 (Including one NMI)
	External	11 (11)*2 (Including one NMI)				20 (20)*2 (Including one NMI)			
Timer/counter		16-bit timer/event counter (TAA) × 4 ch 16-bit timer/event counter (TAB) × 1 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch				16-bit timer/event counter (TAA) × 4 ch 16-bit timer/event counter (TAB) × 1 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch			
Watchdog timer		1 ch				1 ch			
Serial interface		UART (LIN compatible)/CSI × 1 ch UART (LIN compatible)/CSI/I^2C × 1 ch CSI × 1 ch UART (LIN compatible)/I^2C × 1 ch			UART (LIN compatible)/CSI × 1 ch UART (LIN compatible)/CSI/I^2C × 1 ch CSI × 1 ch UART (LIN compatible)/I^2C/CAN × 1 ch	UART (LIN compatible)/CSI × 1 ch UART (LIN compatible)/CSI/I^2C × 2 ch CSI × 2 ch UART (LIN compatible)/I^2C × 1 ch			UART (LIN compatible)/CSI × 1 ch UART (LIN compatible)/CSI/I^2C × 2 ch CSI × 2 ch UART (LIN compatible)/I^2C/CAN × 1 ch
A/D converter		10 bits × 8 ch				10 bits × 8 ch			
D/A converter		–				–			
DMA controller		4 ch				4 ch			
Ports	I/O	29				41			
	Input	–				–			
Debug control unit		Provided (RUN/break)				Provided (RUN/break)			
USB controller		USB 2.0 function (full-speed) × 1 ch				USB 2.0 function (full-speed) × 1 ch			
Ethernet controller		1 ch				1 ch			
Other peripheral functions		Real-time counter (RTC), LVI/clock monitor, CRC, RAM retention flag				Motor control, real-time counter (RTC), LVI/clock monitor, CRC, RAM retention flag			
Operating frequency		When using main clock: 24 to 50 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz				When using main clock: 24 to 50 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz			
Power supply voltage		2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)				2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)			
Package		64-pin LQFP (10 × 10 mm), 64-pin WQFN (9 × 9 mm)				80-pin LQFP (12 × 12 mm)			
Operating ambient temperature		−40°C to +85°C				−40°C to +85°C			

*1. Includes 16 KB of data-only RAM.
*2. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850ES/JG3-E (Under development)			
Part No.		μPD70F3834	μPD70F3835	μPD70F3836	μPD70F3837
CPU name		V850ES			
CPU performance (Dhrystone)		103 MIPS (@ 50 MHz)			
Internal ROM		64 KB (flash)	128 KB (flash)	256 KB (flash)	
Internal RAM		32 KB*1	48 KB*1	64 KB*1	
External bus interface	Bus type	–			
	Address bus	–			
	Data bus	–			
	Chip select signal	–			
Memory controller		–			
Interrupt sources	Internal	66 (Including one NMI)			70 (Including one NMI)
	External	22 (22)*2 (Including one NMI)			
Timer/counter		16-bit timer/event counter (TAA) × 4 ch 16-bit timer/event counter (TAB) × 1 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch			
Watchdog timer		1 ch			
Serial interface		UART (LIN compatible)/CSI × 1 ch UART (LIN compatible)/CSI/I^2C × 2 ch CSI × 2 ch UART (LIN compatible)/I^2C × 1 ch			UART (LIN compatible)/CSI × 1 ch UART (LIN compatible)/CSI/I^2C × 2 ch CSI × 2 ch UART (LIN compatible)/I^2C/CAN × 1 ch
A/D converter		10 bits × 10 ch			
D/A converter		–			
DMA controller		4 ch			
Ports	I/O	64			
	Input	–			
Debug control unit		Provided (RUN/break)			
USB controller		USB 2.0 function (full-speed) × 1 ch			
Ethernet controller		1 ch			
Other peripheral functions		Motor control, real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag			
Operating frequency		When using main clock: 24 to 50 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz			
Power supply voltage		2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)			
Package		100-pin LQFP (14 × 14 mm), 121-pin FBGA (8 × 8 mm)*3			
Operating ambient temperature		−40°C to +85°C			

*1. Includes 16 KB of data-only RAM.
*2. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*3. μPD70F3837 only

Low-End Lineup (3/10)

3 V Operation

Generic Name		V850ES/JH3-E					
Part No.		μPD70F3778	μPD70F3779	μPD70F3780	μPD70F3781	μPD70F3782	μPD70F3783
CPU name		V850ES					
CPU performance (Dhrystone)		103 MIPS (@ 50 MHz)					
Internal ROM		256 KB (flash)	384 KB (flash)	512 KB (flash)	384 KB (flash)	512 KB (flash)	
Internal RAM		76 KB (including 16 KB of data-only RAM)			124 KB (including 64 KB of data-only RAM)		
External bus interface	Bus type	Multiplexed/separate					
	Address bus	22 bits					
	Data bus	8/16 bits					
	Chip select signal	3					
Memory controller		SRAM, etc.					
Interrupt sources	Internal	78 (Including one NMI)					82 (Including one NMI)
	External	22 (22)*1 (Including one NMI)					
Timer/counter		16-bit timer/event counter (TAA) × 6 ch 16-bit timer/event counter (TAB) × 2 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch					
Watchdog timer		1 ch					
Serial interface		UART (LIN compatible)/CSI × 1 ch UART (LIN compatible)/CSI (with FIFO) × 1 ch UART (with FIFO)/CSI × 2 ch*2 UART (LIN compatible)/CSI/I²C × 2 ch UART (LIN compatible)/CSI (with FIFO)*3/I²C × 1 ch CSI (with FIFO)*3 × 1 ch UART (LIN compatible)/I²C × 1 ch					UART (LIN compatible)/CSI × 1 ch UART (LIN compatible)/CSI (with FIFO) × 1 ch UART (with FIFO)/CSI × 2 ch*2 UART (LIN compatible)/CSI/I²C × 2 ch UART (LIN compatible)/CSI (with FIFO)*3/I²C × 1 ch CSI (with FIFO)*3 × 1 ch UART (LIN compatible)/I²C/CAN × 1 ch
A/D converter		10 bits × 10 ch					
D/A converter		–					
DMA controller		4 ch					
Ports	I/O	84					
	Input	–					
Debug control unit		Provided (RUN/break)					
USB controller		USB 2.0 function (full-speed) × 1 ch					
Ethernet controller		1 ch					
Other peripheral functions		Motor control, real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag					
Operating frequency		When using main clock: 24 to 50 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz					
Power supply voltage		2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)					
Package		128-pin LQFP (14 × 20 mm)					
Operating ambient temperature		−40°C to +85°C					

*1. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*2. One channel is assigned to two different pins.
*3. The same channel is assigned to two different pins.

Generic Name		V850ES/JJ3-E		
Part No.		μPD70F3784	μPD70F3785	μPD70F3786
CPU name		V850ES		
CPU performance (Dhrystone)		103 MIPS (@ 50 MHz)		
Internal ROM		512 KB (flash)		
Internal RAM		76 KB (including 16 KB of data-only RAM)	124 KB (including 64 KB of data-only RAM)	
External bus interface	Bus type	Multiplexed/separate		
	Address bus	24 bits		
	Data bus	8/16 bits		
	Chip select signal	2		
Memory controller		SRAM, etc.		
Interrupt sources	Internal	84 (Including one NMI)		88 (Including one NMI)
	External	27 (27)*1 (Including one NMI)		
Timer/counter		16-bit timer/event counter (TAA) × 6 ch 16-bit timer/event counter (TAB) × 2 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch		
Watchdog timer		1 ch		
Serial interface		UART (LIN compatible)/CSI × 3 ch UART (LIN compatible)/CSI (with FIFO) × 1 ch UART (with FIFO)/CSI × 2 ch*2 UART (LIN compatible)/CSI/I²C × 2 ch UART (LIN compatible)/CSI (with FIFO)*3/I²C × 1 ch CSI (with FIFO)*3 × 1 ch I²C × 1 ch UART (LIN compatible)/I²C × 1 ch		UART (LIN compatible)/CSI × 3 ch UART (LIN compatible)/CSI (with FIFO) × 1 ch UART (with FIFO)/CSI × 2 ch*2 UART (LIN compatible)/CSI/I²C × 2 ch UART (LIN compatible)/CSI (with FIFO)*3/I²C × 1 ch CSI (with FIFO)*3 × 1 ch I²C × 1 ch UART (LIN compatible)/I²C/CAN × 1 ch
A/D converter		10 bits × 12 ch		
D/A converter		–		
DMA controller		4 ch		
Ports	I/O	100		
	Input	–		
Debug control unit		Provided (RUN/break)		
USB controller		USB 2.0 function (full-speed) × 1 ch		
Ethernet controller		1 ch		
Other peripheral functions		Motor control, real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag		
Operating frequency		When using main clock: 24 to 50 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz		
Power supply voltage		2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)		
Package		144-pin LQFP (20 × 20 mm)		
Operating ambient temperature		−40°C to +85°C		

*1. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*2. One channel is assigned to two different pins.
*3. The same channel is assigned to two different pins.

Low-End Lineup (4/10)

3 V Operation

Generic Name		V850ES/JC3-H									
Part No.		μPD70F3809	μPD70F3810	μPD70F3811	μPD70F3812	μPD70F3813	μPD70F3814	μPD70F3815	μPD70F3816	μPD70F3817	μPD70F3818	μPD70F3819
CPU name		V850ES										
CPU performance (Dhrystone)		98 MIPS (@ 48 MHz)										
Internal ROM		16 KB (flash)	32 KB (flash)	64 KB (flash)	128 KB (flash)	256 KB (flash)	16 KB (flash)	32 KB (flash)	64 KB (flash)	128 KB (flash)	256 KB (flash)	
Internal RAM		8 KB	16 KB	24 KB			8 KB	16 KB	24 KB			
External bus interface	Bus type	–										
	Address bus	–										
	Data bus	–										
	Chip select signal	–										
Memory controller		–										
Interrupt sources	Internal	52 (Including one NMI)					54 (Including one NMI)					58 (Including one NMI)
	External	10 (10)* (Including one NMI)										
Timer/counter		16-bit timer/event counter (TAA) × 4 ch 16-bit timer/event counter (TAB) × 1 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch										
Watchdog timer		1 ch										
Serial interface		UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/CSI/I²C × 1 ch CSI × 1 ch					UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/CSI/I²C × 1 ch CSI × 1 ch UART (LIN compatible)/I²C × 1 ch					UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/CSI/I²C × 1 ch CSI × 1 ch UART (LIN compatible)/I²C/CAN × 1 ch
A/D converter		10 bits × 5 ch					10 bits × 6 ch					
D/A converter		–					8 bits × 1 ch					
DMA controller		4 ch										
Ports	I/O	25					32					
	Input	–										
Debug control unit		Provided (RUN/break)										
USB controller		USB 2.0 function (full-speed) × 1 ch										
Other peripheral functions		Real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag										
Operating frequency		When using main clock: 24 to 48 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz										
Power supply voltage		2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)										
Package		40-pin WQFN (6 × 6 mm)					48-pin LQFP (7 × 7 mm), 48-pin WQFN (7 × 7 mm)					
Operating ambient temperature		−40°C to +85°C										

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850ES/JE3-H					
Part No.		μPD70F3820	μPD70F3821	μPD70F3822	μPD70F3823	μPD70F3824	μPD70F3825
CPU name		V850ES					
CPU performance (Dhrystone)		98 MIPS (@ 48 MHz)					
Internal ROM		16 KB (flash)	32 KB (flash)	64 KB (flash)	128 KB (flash)	256 KB (flash)	
Internal RAM		8 KB	16 KB	24 KB			
External bus interface	Bus type	–					
	Address bus	–					
	Data bus	–					
	Chip select signal	–					
Memory controller		–					
Interrupt sources	Internal	52 (Including one NMI)					58 (Including one NMI)
	External	11 (11)*1 (Including one NMI)					
Timer/counter		16-bit timer/event counter (TAA) × 4 ch 16-bit timer/event counter (TAB) × 1 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch					
Watchdog timer		1 ch					
Serial interface		UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/CSI/I²C × 1 ch CSI × 1 ch UART (LIN compatible)/I²C × 1 ch					UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/CSI/I²C × 1 ch CSI × 1 ch UART (LIN compatible)/I²C/CAN × 1 ch
A/D converter		10 bits × 10 ch					
D/A converter		8 bits × 1 ch					
DMA controller		4 ch					
Ports	I/O	45					
	Input	–					
Debug control unit		Provided (RUN/break)					
USB controller		USB 2.0 function (full-speed) × 1 ch					
Other peripheral functions		Motor control, real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag					
Operating frequency		When using main clock: 24 to 48 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz					
Power supply voltage		2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)					
Package		64-pin LQFP (10 × 10 mm), 64-pin FBGA (6 × 6 mm)*2, 64-pin WQFN (9 × 9 mm)					
Operating ambient temperature		−40°C to +85°C					

*1. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*2. μPD70F3824 only

Low-End Lineup (5/10)

3 V Operation

Generic Name		V850ES/JG3-H			
Part No.		μPD70F3760	μPD70F3761	μPD70F3762	μPD70F3770
CPU name		V850ES			
CPU performance (Dhrystone)		98 MIPS (@ 48 MHz)			
Internal ROM		256 KB (flash)	384 KB (flash)	512 KB (flash)	256 KB (flash)
Internal RAM		40 KB*1	48 KB*1	56 KB*1	40 KB*1
External bus interface	Bus type	Multiplexed			
	Address bus	16 bits			
	Data bus	8/16 bits			
	Chip select signal	3			
Memory controller		SRAM, etc.			
Interrupt sources	Internal	69 (including one NMI)			73 (including one NMI)
	External	17 (17)*2 (including one NMI)			
Timer/counter		16-bit timer/event counter (TAA) × 6 ch 16-bit timer/event counter (TAB) × 2 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch			
Watchdog timer		1 ch			
Serial interface		CSI × 2 ch UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/I^2C × 2 ch UART (LIN compatible)/CSI/I^2C × 1 ch			CSI × 2 ch UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/I^2C × 1 ch UART (LIN compatible)/CSI/I^2C × 1 ch UART (LIN compatible)/I^2C/CAN × 1 ch
A/D converter		10 bits × 12 ch			
D/A converter		8 bits × 2 ch			
DMA controller		4 ch			
Ports	I/O	77			
	Input	–			
Debug control unit		Provided (RUN/break)			
USB controller		USB 2.0 function (full-speed) × 1 ch			
Other peripheral functions		Motor control, real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag			
Operating frequency		When using main clock: 24 to 48 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz			
Power supply voltage		2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)			
Package		100-pin LQFP (14 × 14 mm)			
Operating ambient temperature		−40°C to +85°C			

*1. Includes 8 KB of data-only RAM.
*2. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850ES/JH3-H			
Part No.		μPD70F3765	μPD70F3766	μPD70F3767	μPD70F3771
CPU name		V850ES			
CPU performance (Dhrystone)		98 MIPS (@ 48 MHz)			
Internal ROM		256 KB (flash)	384 KB (flash)	512 KB (flash)	256 KB (flash)
Internal RAM		40 KB*1	48 KB*1	56 KB*1	40 KB*1
External bus interface	Bus type	Multiplexed/separate			
	Address bus	24 bits			
	Data bus	8/16 bits			
	Chip select signal	3			
Memory controller		SRAM, etc.			
Interrupt sources	Internal	69 (including one NMI)			73 (including one NMI)
	External	20 (20)*2 (including one NMI)			
Timer/counter		16-bit timer/event counter (TAA) × 6 ch 16-bit timer/event counter (TAB) × 2 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch			
Watchdog timer		1 ch			
Serial interface		CSI × 2 ch UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/I^2C × 2 ch UART (LIN compatible)/CSI/I^2C × 1 ch			CSI × 2 ch UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/I^2C × 1 ch UART (LIN compatible)/CSI/I^2C × 1 ch UART (LIN compatible)/I^2C/CAN × 1 ch
A/D converter		10 bits × 12 ch			
D/A converter		8 bits × 2 ch			
DMA controller		4 ch			
Ports	I/O	96			
	Input	–			
Debug control unit		Provided (RUN/break)			
USB controller		USB 2.0 function (full-speed) × 1 ch			
Other peripheral functions		Motor control, real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag			
Operating frequency		When using main clock: 24 to 48 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz			
Power supply voltage		2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)			
Package		128-pin LQFP (14 × 20 mm)			
Operating ambient temperature		−40°C to +85°C			

*1. Includes 8 KB of data-only RAM.
*2 The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Low-End Lineup (6/10)

3 V Operation

Generic Name		V850ES/JG3-U		V850ES/JH3-U	
Part No.		μPD70F3763	μPD70F3764	μPD70F3768	μPD70F3769
CPU name		V850ES		V850ES	
CPU performance (Dhrystone)		98 MIPS (@ 48 MHz)		98 MIPS (@ 48 MHz)	
Internal ROM		384 KB (flash)	512 KB (flash)	384 KB (flash)	512 KB (flash)
Internal RAM		48 KB*1	56 KB*1	48 KB*1	56 KB*1
External bus interface	Bus type	Multiplexed		Multiplexed/separate	
	Address bus	16 bits		24 bits	
	Data bus	8/16 bits		8/16 bits	
	Chip select signal	3		3	
Memory controller		SRAM, etc.		SRAM, etc.	
Interrupt sources	Internal	72 (including one NMI)		72 (including one NMI)	
	External	15 (15)*2 (including one NMI)		20 (20)*2 (including one NMI)	
Timer/counter		16-bit timer/event counter (TAA) × 6 ch 16-bit timer/event counter (TAB) × 2 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch		16-bit timer/event counter (TAA) × 6 ch 16-bit timer/event counter (TAB) × 2 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch	
Watchdog timer		1 ch		1 ch	
Serial interface		CSI × 2 ch UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/I^2C × 2 ch UART (LIN compatible)/CSI/I^2C × 1 ch		CSI × 2 ch UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/I^2C × 2 ch UART (LIN compatible)/CSI/I^2C × 1 ch	
A/D converter		10 bits × 12 ch		10 bits × 12 ch	
D/A converter		8 bits × 2 ch		8 bits × 2 ch	
DMA controller		4 ch		4 ch	
Ports	I/O	75		96	
	Input	–		–	
Debug control unit		Provided (RUN/break)		Provided (RUN/break)	
USB controller		USB 2.0 function (full-speed) × 1 ch USB 2.0 host (full-speed) × 1 ch		USB 2.0 function (full-speed) × 1 ch USB 2.0 host (full-speed) × 1 ch	
Other peripheral functions		Motor control, real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag		Motor control, real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag	
Operating frequency		When using main clock: 24 to 48 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz		When using main clock: 24 to 48 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz	
Power supply voltage		2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)		2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)	
Package		100-pin LQFP (14 × 14 mm)		128-pin LQFP (14 × 20 mm)	
Operating ambient temperature		−40°C to +85°C		−40°C to +85°C	

*1. Includes 8 KB of data-only RAM.
*2. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850ES/JC3-L									
Part No.		μPD70F3797	μPD70F3798	μPD70F3799	μPD70F3800	μPD70F3838	μPD70F3801	μPD70F3802	μPD70F3803	μPD70F3804	μPD70F3839
CPU name		V850ES									
CPU performance (Dhrystone)		43 MIPS (@ 20 MHz)									
Internal ROM		16 KB (flash)	32 KB (flash)	64 KB (flash)	128 KB (flash)	256 KB (flash)	16 KB (flash)	32 KB (flash)	64 KB (flash)	128 KB (flash)	256 KB (flash)
Internal RAM		8 KB				16 KB	8 KB				16 KB
External bus interface	Bus type	–									
	Address bus	–									
	Data bus	–									
	Chip select signal	–									
Memory controller		–									
Interrupt sources	Internal	43 (Including one NMI)					47 (Including one NMI)				
	External	6 (6)* (Including one NMI)									
Timer/counter		16-bit timer/event counter (TMP) × 6 ch 16-bit timer/event counter (TMQ) × 1 ch 16-bit interval timer (TMM) × 1 ch									
Watchdog timer		1 ch									
Serial interface		CSI × 1 ch UART (LIN compatible) × 1 ch CSI/I^2C × 1 ch UART (LIN compatible)/I^2C × 1 ch					CSI × 2 ch UART (LIN compatible)/CSI × 1 ch CSI/I^2C × 1 ch UART (LIN compatible)/I^2C × 2 ch				
A/D converter		10 bits × 5 ch					10 bits × 6 ch				
D/A converter		–					8 bits × 1 ch				
DMA controller		4 ch									
Ports	I/O	27					34				
	Input	–									
Debug control unit		Provided (RUN/break)									
Other peripheral functions		Watch timer: 1 ch, real-time output, LVI/clock monitor, CRC									
Operating frequency		When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz									
Power supply voltage		2.2 V to 3.6 V (A/D converter: 2.7 V to 3.6 V)									
Package		40-pin WQFN (6 × 6 mm)					48-pin LQFP (7 × 7 mm), 48-pin WQFN (7 × 7 mm)				
Operating ambient temperature		−40°C to +85°C									

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Low-End Lineup (7/10)

3 V Operation

Generic Name		V850ES/JE3-L					V850ES/JF3-L	
Part No.		μPD70F3805	μPD70F3806	μPD70F3807	μPD70F3808	μPD70F3840	μPD70F3735	μPD70F3736
CPU name		V850ES					V850ES	
CPU performance (Dhrystone)		43 MIPS (@ 20 MHz)					43 MIPS (@ 20 MHz)	
Internal ROM		16 KB (flash)	32 KB (flash)	64 KB (flash)	128 KB (flash)	256 KB (flash)	128 KB (flash)	256 KB (flash)
Internal RAM		8 KB				16 KB	8 KB	16 KB
External bus interface	Bus type	–					Multiplexed	
	Address bus	–					18 bits	
	Data bus	–					8/16 bits	
	Chip select signal	–					–	
Memory controller		–					SRAM, etc.	
Interrupt sources	Internal	49 (Including one NMI)					40 (including one NMI)	
	External	9 (9)* (Including one NMI)					9 (9)* (including one NMI)	
Timer/counter		16-bit timer/event counter (TMP) × 6 ch 16-bit timer/event counter (TMQ) × 1 ch 16-bit interval timer (TMM) × 1 ch					16-bit timer/event counter (TMP) × 4 ch 16-bit timer/event counter (TMQ) × 1 ch 16-bit interval timer (TMM) × 1 ch	
Watchdog timer		1 ch					1 ch	
Serial interface		CSI × 3 ch UART (LIN compatible)/CSI × 1 ch CSI/I^2C × 1 ch UART (LIN compatible)/I^2C × 2 ch					CSI × 2 ch UART (LIN compatible) × 2 ch CSI/I^2C × 1 ch UART (LIN compatible)/I^2C × 1 ch	
A/D converter		10 bits × 10 ch					10 bits × 8 ch	
D/A converter		8 bits × 1 ch					8 bits × 1 ch	
DMA controller		4 ch					4 ch	
Ports	I/O	50					66	
	Input	–					–	
Debug control unit		Provided (RUN/break)					Provided (RUN/break)	
Other peripheral functions		Watch timer: 1 ch, real-time output, LVI/clock monitor, CRC					Watch timer: 1 ch, real-time output, LVI/clock monitor, CRC	
Operating frequency		When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz					When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz	
Power supply voltage		2.2 V to 3.6 V (A/D converter: 2.7 V to 3.6 V)					2.2 V to 3.6 V (A/D converter: 2.7 V to 3.6 V)	
Package		64-pin LQFP (10 × 10 mm), 64-pin FBGA (5 × 5 mm)					80-pin LQFP (12 × 12 mm), 80-pin LQFP (14 × 14 mm)	
Operating ambient temperature		–40°C to +85°C					–40°C to +85°C	

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850ES/JG3-L									
Part No.		μPD70F3737	μPD70F3738	μPD70F3792	μPD70F3793	μPD70F3794	μPD70F3795	μPD70F3796	μPD70F3841	μPD70F3842	μPD70F3843	μPD70F3844
CPU name		V850ES										
CPU performance (Dhrystone)		43 MIPS (@ 20 MHz)										
Internal ROM		128 KB (flash)	256 KB (flash)	384 KB (flash)	512 KB (flash)	256 KB (flash)	384 KB (flash)	512 KB (flash)	768 KB (flash)	1 MB (flash)	768 KB (flash)	1 MB (flash)
Internal RAM		8 KB	16 KB	32 KB	40 KB				80 KB*1			
External bus interface	Bus type	Multiplexed/separate										
	Address bus	22 bits										
	Data bus	8/16 bits										
	Chip select signal	–										
Memory controller		SRAM, etc							–			
Interrupt sources	Internal	48 (Including one NMI)	55 (Including one NMI)									
	External	9 (9)*2 (Including one NMI)										
Timer/counter		16-bit timer/event counter (TMP) × 6 ch 16-bit timer/event counter (TMQ) × 1 ch 16-bit interval timer (TMM) × 1 ch										
Watchdog timer		1 ch										
Serial interface		CSI × 3 ch UART (LIN compatible)/CSI × 1 ch CSI/I^2C × 1 ch UART (LIN compatible)/I^2C × 2 ch	CSI × 3 ch UART (LIN compatible) × 4 ch UART (LIN compatible)/CSI × 1 ch CSI/I^2C × 1 ch UART (LIN compatible)/I^2C × 2 ch									
A/D converter		10 bits × 12 ch										
D/A converter		8 bits × 2 ch										
DMA controller		4 ch										
Ports	I/O	84		83		80			83		80	
	Input	–										
Debug control unit		Provided (RUN/break)										
USB controller		–				USB function (full-speed) × 1 ch			–		USB function (full-speed) × 1 ch	
Other peripheral functions		Watch timer: 1 ch, real-time output, LVI/clock monitor, CRC	Real-time counter (RTC), watch timer: 1 ch, real-time output, LVI/clock monitor, CRC									
Operating frequency		When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz										
Power supply voltage		2.2 V to 3.6 V (A/D converter: 2.7 V to 3.6 V)	2.0 V to 3.6 V (A/D converter: 2.7 V to 3.6 V)			2.0 V to 3.6 V (A/D converter: 2.7 V to 3.6 V, USB controller: 3.0 V to 3.6 V)			2.0 V to 3.6 V (A/D converter: 2.7 V to 3.6 V)		2.0 V to 3.6 V (A/D converter: 2.7 V to 3.6 V, USB controller: 3.0 V to 3.6 V)	
Package		100-pin LQFP (14 × 14 mm) 100-pin LQFP (14 × 20 mm) 121-pin FBGA (8 × 8 mm)	100-pin LQFP (14 × 14 mm) 121-pin FBGA (8 × 8 mm)									
Operating ambient temperature		–40°C to +85°C										

*1. 24 bytes is expanded internal RAM.
*2. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Low-End Lineup (8/10)

3 V Operation

Generic Name		V850ES/JG3				V850ES/JJ3			
Part No.		μPD70F3739	μPD70F3740	μPD70F3741	μPD70F3742	μPD70F3743	μPD70F3744	μPD70F3745	μPD70F3746
CPU name		V850ES				V850ES			
CPU performance (Dhrystone)		69 MIPS (@ 32 MHz)				69 MIPS (@ 32 MHz)			
Internal ROM		384 KB (flash)	512 KB (flash)	768 KB (flash)	1024 KB (flash)	384 KB (flash)	512 KB (flash)	768 KB (flash)	1024 KB (flash)
Internal RAM		32 KB	40 KB	60 KB	60 KB	32 KB	40 KB	60 KB	
External bus interface	Bus type	Multiplexed/separate				Multiplexed/separate			
	Address bus	22 bits				24 bits			
	Data bus	8/16 bits				8/16 bits			
	Chip select signal	–				4			
Memory controller		SRAM, etc.				SRAM, etc.			
Interrupt sources	Internal	48 (including one NMI)				61 (including one NMI)			
	External	9 (9)* (including one NMI)				10 (10)* (including one NMI)			
Timer/counter		16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 6 ch 16-bit timer/event counter (TMQ) × 1 ch				16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 9 ch 16-bit timer/event counter (TMQ) × 1 ch			
Watchdog timer		1 ch				1 ch			
Serial interface		CSI × 3 ch UART (LIN compatible)/CSI × 1 ch CSI/I^2C × 1 ch UART (LIN compatible)/I^2C × 2 ch				CSI × 4 ch UART (LIN compatible)/CSI × 1 ch CSI/I^2C × 1 ch UART (LIN compatible)/I^2C × 2 ch UART (LIN compatible) × 1 ch			
A/D converter		10 bits × 12 ch				10 bits × 16 ch			
D/A converter		8 bits × 2 ch				8 bits × 2 ch			
DMA controller		4 ch				4 ch			
Ports	I/O	84				128			
	Input	–				–			
Debug control unit		Provided (RUN/break)				Provided (RUN/break)			
Other peripheral functions		Watch timer: 1 ch, real-time output, LVI/clock monitor, CRC, RAM retention flag				Watch timer: 1 ch, real-time output, LVI/clock monitor, CRC			
Operating frequency		When using main clock: 2.5 to 32 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz				When using main clock: 2.5 to 32 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz			
Power supply voltage		2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V)				2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V)			
Package		100-pin LQFP (14 × 14 mm)				144-pin LQFP (20 × 20 mm)			
Operating ambient temperature		–40°C to +85°C				–40°C to +85°C			

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850ES/ST2
Part No.		μPD703220
CPU name		V850ES
CPU performance (Dhrystone)		–
Internal ROM		ROMless
Internal RAM		48 KB
External bus interface	Bus type	Separate (multiplexed selectable only for CS1)
	Address bus	22 bits
	Data bus	8/16 bits
	Chip select signal	4
Memory controller		SRAM, etc.
Interrupt sources	Internal	28 (including one NMI)
	External	9 (including one NMI)
Timer/counter		16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 6 ch
Watchdog timer		1 ch
Serial interface		CSI × 1 ch CSI/UART × 1 ch UART × 1 ch
A/D converter		10 bits × 8 ch
D/A converter		8 bits × 2 ch
DMA controller		–
Ports	I/O	57
	Input	8
Debug control unit		–
Other peripheral functions		Real-time output
Operating frequency		20 to 34 MHz
Power supply voltage		3.0 V to 3.6 V
Package		120-pin TQFP (14 × 14 mm) 144-pin LQFP (20 × 20 mm)
Operating ambient temperature		–40°C to +85°C

Low-End Lineup (9/10)

3 V Operation

Generic Name		V850ES/SG2-H			V850ES/SG2					
Part No.	Without IEBus, CAN	μPD703262HY	μPD703263HY	μPD70F3263HY	μPD703260Y	μPD703261Y	μPD70F3261Y	μPD703262Y	μPD703263Y	μPD70F3263Y
	On-chip IEBus	μPD703272HY	μPD703273HY	μPD70F3273HY	μPD703270Y	μPD703271Y	μPD70F3271Y	μPD703272Y	μPD703273Y	μPD70F3273Y
	On-chip CAN	μPD703282HY	μPD703283HY	μPD70F3283HY	μPD703280Y	μPD703281Y	μPD70F3281Y	μPD703282Y	μPD703283Y	μPD70F3283Y
CPU name		V850ES			V850ES					
CPU performance (Dhrystone)		66 MIPS (@ 32 MHz)			43 MIPS (@ 20 MHz)					
Internal ROM		512 KB (mask)	640 KB (mask)	640 KB (flash)	256 KB (mask)	384 KB (mask)	384 KB (flash)	512 KB (mask)	640 KB (mask)	640 KB (flash)
Internal RAM		40 KB	48 KB		24 KB	32 KB		40 KB	48 KB	
External bus interface	Bus type	Multiplexed/separate			Multiplexed/separate					
	Address bus	22 bits			22 bits					
	Data bus	8/16 bits			8/16 bits					
	Chip select signal	–			–					
Memory controller		SRAM, etc.			SRAM, etc.					
Interrupt sources	Internal	47[*1]/51[*2] (including one NMI for each)			48[*1]/52[*2] (Including one NMI for each)					
	External	9 (9)[*3] (including one NMI)			9 (9)[*3] (including one NMI)					
Timer/counter		16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 6 ch 16-bit timer/event counter (TMQ) × 1 ch			16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 6 ch 16-bit timer/event counter (TMQ) × 1 ch					
Watchdog timer		1 ch			1 ch					
Serial interface		CSI × 3 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch			CSI × 3 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch					
A/D converter		10 bits × 12 ch			10 bits × 12 ch					
D/A converter		8 bits × 2 ch			8 bits × 2 ch					
DMA controller		4 ch			4 ch					
Ports	I/O	84			84					
	Input	–			–					
Debug control unit		–		Provided (RUN/break)	–		Provided (RUN/break)	–		Provided (RUN/break)
Other peripheral functions		Watch timer: 1 ch IEBus controller: 1 ch[*4] CAN controller: 1 ch[*5] ROM correction: 4 points Real-time output Clock monitor, CRC			Watch timer: 1 ch IEBus controller: 1 ch[*6] CAN controller: 1 ch[*7] ROM correction: 4 points Real-time output LVI/clock monitor, CRC					
Operating frequency		When using main clock: 2.5 to 32 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz			When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz					
Power supply voltage		3.0 V to 3.6 V (@ 32 MHz)			2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V) (@ 20 MHz)					
Package		100-pin LQFP (14 × 14mm)			100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)[*8]					
Operating ambient temperature		−40°C to +85°C			−40°C to +85°C					

*1. Products without IEBus and CAN only
*2. Products with IEBus or CAN only
*3. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*4. μPD703272HY/3273HY/F3273HY only
*5. μPD703282HY/3283HY/F3283HY only
*6. μPD703270Y/3271Y/F3271Y/3272Y/3273Y/F3273Y only
*7. μPD703280Y/3281Y/F3281Y/3282Y/3283Y/F3283Y only
*8. μPD703260Y/3261Y/F3261Y/3270Y/3271Y/F3271Y only

Generic Name			V850ES/SJ2-H			V850ES/SJ2				
Part No.	Without IEBus, CAN		μPD703265HY	μPD703266HY	μPD70F3266HY	μPD703264Y	μPD70F3264Y	μPD703265Y	μPD703266Y	μPD70F3266Y
	On-chip IEBus		μPD703275HY	μPD703276HY	μPD70F3276HY	μPD703274Y	μPD70F3274Y	μPD703275Y	μPD703276Y	μPD70F3276Y
	On-chip CAN	1 ch	μPD703285HY	μPD703286HY	μPD70F3286HY	μPD703284Y	μPD70F3284Y	μPD703285Y	μPD703286Y	μPD70F3286Y
		2 ch	μPD703287HY	μPD703288HY	μPD70F3288HY	–	–	μPD703287Y	μPD703288Y	μPD70F3288Y
CPU name			V850ES			V850ES				
CPU performance (Dhrystone)			66 MIPS (@ 32 MHz)			43 MIPS (@ 20 MHz)				
Internal ROM			512 KB (mask)	640 KB (mask)	640 KB (flash)	384 KB (mask)	384 KB (flash)	512 KB (mask)	640 KB (mask)	640 KB (flash)
Internal RAM			40 KB	48 KB		32 KB		40 KB	48 KB	
External bus interface	Bus type		Multiplexed/separate			Multiplexed/separate				
	Address bus		24 bits			24 bits				
	Data bus		8/16 bits			8/16 bits				
	Chip select signal		4			4				
Memory controller			SRAM, etc.			SRAM, etc.				
Interrupt sources	Internal		60[*1]/64[*2]/68[*3] (including one NMI for each)			61[*1]/65[*2]/69[*3] (including one NMI for each)				
	External		10 (10)[*4] (including one NMI)			10 (10)[*4] (including one NMI)				
Timer/counter			16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 9 ch 16-bit timer/event counter (TMQ) × 1 ch			16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 9 ch 16-bit timer/event counter (TMQ) × 1 ch				
Watchdog timer			1 ch			1 ch				
Serial interface			CSI × 4 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch UART (LIN compatible) × 1 ch			CSI × 4 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch UART (LIN compatible) × 1 ch				
A/D converter			10 bits × 16 ch			10 bits × 16 ch				
D/A converter			8 bits × 2 ch			8 bits × 2 ch				
DMA controller			4 ch			4 ch				
Ports	I/O		128			128				
	Input		–			–				
Debug control unit			–		Provided (RUN/break)	–	Provided (RUN/break)	–		Provided (RUN/break)
Other peripheral functions			Watch timer: 1 ch IEBus controller: 1 ch[*5] CAN controller: 1 ch[*6] CAN controller: 2 ch[*7] ROM correction: 4 points Real-time output Clock monitor, CRC			Watch timer: 1 ch IEBus controller: 1 ch[*8] CAN controller: 1 ch[*9] CAN controller: 2 ch[*10] ROM correction: 4 points Real-time output LVI/clock monitor, CRC				
Operating frequency			When using main clock: 2.5 to 32 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz			When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz				
Power supply voltage			3.0 V to 3.6 V (@ 32 MHz)			2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V) (@ 20 MHz)				
Package			144-pin LQFP (20 × 20mm)			144-pin LQFP (20 × 20 mm)				
Operating ambient temperature			−40°C to +85°C			−40°C to +85°C				

*1. Products without IEBus and CAN only
*2. Products with IEBus or CAN only
*3. Products with 2 ch CAN only
*4. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*5. μPD703275HY/3276HY/F3276HY only
*6. μPD703285HY/3286HY/F3286HY only
*7. μPD703287HY/3288HY/F3288HY only
*8. μPD703274Y/F3274Y/3275Y/3276Y/F3276Y only
*9. μPD703284Y/F3284Y/3285Y/3286Y/F3286Y only
*10. μPD703287Y/3288Y/F3288Y only

Low-End Lineup (10/10)

3 V Operation

Generic Name		V850ES/SG1
Part No.		μPD703249Y
CPU name		V850ES
CPU performance (Dhrystone)		43 MIPS (@ 20 MHz)
Internal ROM		256 KB (mask)
Internal RAM		12 KB
External bus interface	Bus type	Multiplexed/separate
	Address bus	22 bits
	Data bus	8/16 bits
	Chip select signal	–
Memory controller		SRAM, etc.
Interrupt sources	Internal	32 (including one NMI)
	External	9 (9)* (including one NMI)
Timer/counter		16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 5 ch
Watchdog timer		1 ch
Serial interface		CSI × 2 ch CSI/I²C × 1 ch UART × 2 ch I²C × 1 ch
A/D converter		10 bits × 12 ch
D/A converter		–
DMA controller		–
Ports	I/O	84
	Input	–
Debug control unit		–
Other peripheral functions		Watch timer: 1 ch, ROM correction: 4 points, clock monitor
Operating frequency		When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz
Power supply voltage		2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V)
Package		100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)
Operating ambient temperature		−40°C to +85°C

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

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High-End Lineup (1/2)

Generic Name		V850E2/MN4 (Under development)			
Part No.		μPD70F3510	μPD70F3512	μPD70F3514	μPD70F3515
CPU name		V850E2M		V850E2M × 2	
CPU performance (Dhrystone)		512 MIPS (@ 200 MHz)			
Internal ROM		1 MB (flash)			2 MB (flash)
Internal RAM		64 KB		64 KB × 2	
External bus interface	Bus type	Separate (2 channels)			
	Address bus	26 bits, 26 bits			
	Data bus	8/16/32 bits, 16/32 bits			
	Chip select signal	4, 5			
Memory controller		SDRAM, SRAM, etc.			
Interrupt sources	Internal	180	190	196	
	External	29 (including one NMI)			
Timer/counter		32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 4 units 16-bit encoder timer: 2 ch			
Watchdog timer		1 ch		2 ch	
Serial interface		UART/CSI × 4 ch UART/CSI/I²C × 6 ch*1	UART/CSI × 4 ch UART/CSI/I²C × 4 ch*2 UART/CSI/I²C/CAN × 2 ch*3		
A/D converter		12 bits × 12 ch (5 V analog), 10 bits × 12 ch (3.3 V analog)			
D/A converter		–			
DMA controller		16 ch			
Ports	I/O	181			
	Input	7			
Debug control unit		Provided (RUN/break)			
USB controller		USB 2.0 function (full-speed) × 1 ch USB 2.0 host (full-speed) × 1 ch			
Ethernet controller		1 ch			
Other peripheral functions		Hardware bus common memory: 64 KB, hardware bus side cache: 16 KB, dedicated DMA for secondary memory controller, inverter timer support, boundary scan			
Operating frequency		144 to 200 MHz			
Power supply voltage		1.1 V to 1.3 V (internal)/3.0 V to 3.6 V (external)/analog: 3.0 V to 3.6 V or 4.5 V to 5.5 V*4			
Package		304-pin FBGA (19 × 19 mm)			
Operating ambient temperature		–40°C to +100°C*5			

*1. Of which, 4 UART/SCII channels have FIFO function.
*2. Of which, 3 UART/SCII channels have FIFO function.
*3. Of which, 1 UART/SCII channel have FIFO function.
*4. 10-bit precision when using 3.3 V analog power supply, 12-bit precision when using 5 V analog power supply
*5. Package surface temperature

Generic Name		V850E2/ML4 (Under development)	
Part No.		μPD70F3510	μPD70F3514
CPU name		V850E2M	
CPU performance (Dhrystone)		512 MIPS (@ 200 MHz)	
Internal ROM		768 KB (flash)	1 MB (flash)
Internal RAM		64 KB + expanded RAM: 64 KB	
External bus interface	Bus type	Separate	
	Address bus	26 bits	
	Data bus	8/16/32 bits	
	Chip select signal	4	
Memory controller		SDRAM, SRAM, etc.	
Interrupt sources	Internal	150	
	External	29 (including one NMI)	
Timer/counter		16-bit timer array: 16 ch × 2 unit 32-bit timer array: 4 ch × 1 units 16-bit encoder timer: 2 ch	
Watchdog timer		1 ch	
Serial interface		UART × 4 ch (of which, 2 have FIFO function) CSI × 4 ch (of which, 2 have FIFO function) I²C × 2 ch	
A/D converter		10 bits or 12 bits × 12 ch (5 V input for 12-bit)	
D/A converter		–	
DMA controller		8 ch (4 ch for internal transfers only)	
Ports	I/O	119	
	Input	1	
Debug control unit		Provided (RUN/break/trace)	
USB controller		USB 2.0 function (full-speed) × 1 ch USB 2.0 host (full-speed) × 1 ch	
Ethernet controller		1 ch	
Other peripheral functions		CAN, FPU	
Operating frequency		200 MHz	
Power supply voltage		1.2 V and 3.3 V (±5 V (12-bits A/D)	
Package		216-pin QFP (24 × 24 mm)	
Operating ambient temperature		–40°C to +100°C*	

* Package surface temperature

High-End Lineup (2/2)

Generic Name		V850E/MA3						V850E2/ME3
Part No.		μPD703131BY	μPD703132BY	μPD703133BY	μPD703134BY	μPD70F3134BY	μPD703136BY	μPD703500
CPU name		V850E1						V850E2
CPU performance (Dhrystone)		158 MIPS (@ 80 MHz)						432 MIPS (@ 200 MHz)
Internal ROM		256 KB (mask)		512 KB (mask)		512 KB (flash)	256 KB (mask)	ROMless (instruction cache: 8 KB, data cache: 8 KB)
Internal RAM		16 KB	32 KB	16 KB	32 KB		8 KB	instruction: 168 KB, data: 32 KB
External bus interface	Bus type	Multiplexed/separate						Separate
	Address bus	26 bits						26 bits
	Data bus	8/16 bits						8/16/32 bits
	Chip select signal	8						8
Memory controller		SDRAM, SRAM, etc.						SDRAM, SRAM, etc.
Interrupt sources	Internal	41 (including one NMI)						59
	External	26 (26)* (including one NMI)						40 (including one NMI)
Timer/counter		16-bit interval timer (TMD) × 4 ch 16-bit timer/event counter (TMP) × 3 ch 16-bit timer/event counter (TMQ) × 1 ch (3-phase inverter control PWM timer compatible) 16-bit encoder counter/timer (TMENC) × 1 ch						16-bit timer/event counter (TMC) × 6 ch 16-bit interval timer (TMD) × 4 ch 16-bit encoder counter/timer (TMENC) × 2 ch
Watchdog timer		1 ch						–
Serial interface		CSI/UART × 3 ch UART/I²C × 1 ch						CSI (with FIFO) × 1 ch CSI (with FIFO)/UART × 1 ch UART × 1 ch
A/D converter		10 bits × 8 ch						10 bits × 8 ch
D/A converter		8 bits × 2 ch						–
DMA controller		4 ch						4 ch
Ports	I/O	101						77
	Input	11						1
Debug control unit		Provided (RUN/break)						Provided (RUN/break/trace)
Other peripheral functions		3-phase inverter control, ROM correction: 4 points						USB (function) × 1 ch, SSCG 16-bit PWM output × 2 ch
Operating frequency		5 to 80 MHz						100 to 200 MHz
Power supply voltage		2.3 V to 2.7 V (internal)/3.0 V to 3.6 V (external)						1.40 V to 1.65 V (internal)/3.0 V to 3.6 V (external)
Package		144-pin LQFP (20 × 20 mm) 161-pin FBGA (13 × 13 mm)						176-pin QFP (24 × 24 mm)
Operating ambient temperature		–40°C to +85°C						–40°C to +80°C

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850E/ME2			
Part No.		μPD703111B-06	μPD703111B-10	μPD703111B-13	μPD703111B-15
CPU name		V850E1			
CPU performance (Dhrystone)		142 MIPS (@ 66 MHz)	215 MIPS (@ 100 MHz)	286 MIPS (@ 133 MHz)	325 MIPS (@ 150 MHz)
Internal ROM		ROMless (instruction cache: 8 KB)			
Internal RAM		instruction: 128 KB, data: 16 KB			
External bus interface	Bus type	Separate			
	Address bus	26 bits			
	Data bus	8/16/32 bits			
	Chip select signal	8			
Memory controller		SDRAM, SRAM, etc.			
Interrupt sources	Internal	59			
	External	40 (32)* (including one NMI)			
Timer/counter		16-bit timer/event counter (TMC) × 6 ch 16-bit interval timer (TMD) × 4 ch 16-bit encoder counter/timer (TMENC) × 2 ch			
Watchdog timer		–			
Serial interface		CSI (with FIFO) × 1 ch CSI (with FIFO)/UART × 1 ch UART × 1 ch			
A/D converter		10 bits × 8 ch			
D/A converter		–			
DMA controller		4 ch			
Ports	I/O	77			
	Input	1			
Debug control unit		Provided (RUN/break/trace)			
Other peripheral functions		USB (function) × 1 ch, SSCG 16-bit PWM output × 2 ch			
Operating frequency		10 to 150 MHz			
Power supply voltage		1.35 V to 1.65 V (internal)/3.0 V to 3.6 V (external)			1.40 V to 1.65 V (internal)/3.0 V to 3.6 V (external)
Package		176-pin LQFP (24 × 24 mm)			
Operating ambient temperature		–40°C to +85°C			–40°C to +70°C

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

ASSP Lineup (Inverter Control, etc.) (1/5)

Generic Name		V850E/IG4			V850E/IH4		
Part No.		μPD70F3913	μPD70F3914	μPD70F3915	μPD70F3916	μPD70F3917	μPD70F3918
CPU name		V850E1			V850E1		
CPU performance (Dhrystone)		197 MIPS (@ 100 MHz)			197 MIPS (@ 100 MHz)		
Internal ROM		256 KB (flash)	384 KB (flash)	480 KB (flash)	256 KB (flash)	384 KB (flash)	480 KB (flash)
Internal RAM		24 KB			24 KB		
External bus interface	Bus type	–			–		
	Address bus	–			–		
	Data bus	–			–		
	Chip select signal	–			–		
Memory controller		–			–		
Interrupt sources	Internal	82 (Including one NMI)			82 (Including one NMI)		
	External	22 (22)*			22 (22)*		
Timer/counter		16-bit timer/event counter (TAB) × 2 ch (3-phase inverter control PWM timer compatible) 16-bit timer/event counter (TAA) × 1 ch 16-bit timer/event counter (TMT) × 4 ch (encoder count function: 2 ch) 16-bit timer/counter (TAA) × 2 ch 16-bit interval timer (TMM) × 4 ch			16-bit timer/event counter (TAB) × 2 ch (3-phase inverter control PWM timer compatible) 16-bit timer/event counter (TAA) × 1 ch 16-bit timer/event counter (TMT) × 4 ch (encoder count function: 2 ch) 16-bit timer/counter (TAA) × 2 ch 16-bit interval timer (TMM) × 4 ch		
Watchdog timer		1 ch			1 ch		
Serial interface		CSI/UART (With FIFO) × 1 ch CSI/UART × 2 ch UART/I²C × 1 ch			CSI/UART (With FIFO) × 1 ch CSI/UART × 2 ch UART/I²C × 1 ch		
A/D converter		12 bits × 4 ch (A/D converter 0), 12 bits × 3 ch (A/D converter 1) (conversion time: 2 μs) 10 bits × 12 ch			12 bits × 4 ch, 2 units (conversion time: 2 μs) 10 bits × 12 ch		
D/A converter		–			–		
DMA controller		7 ch			7 ch		
Ports	I/O	55			68		
	Input	12			12		
Debug control unit		Provided (RUN/break)			Provided (RUN/break/trace)		
USB controller		–			–		
Other peripheral functions		3-phase inverter control, 6 operational amplifiers, comparators: 12 circuits, software pull-up, POC/LVI/clock monitor			3-phase inverter control, 6 operational amplifiers, comparators: 12 circuits, software pull-up, POC/LVI/clock monitor		
Operating frequency		10 to 100 MHz			10 to 100 MHz		
Power supply voltage		1.5 V/5.0 V			1.5 V/5.0 V		
Package		100-pin LQFP (14 × 14 mm) 100-pin LQFP (14 × 20 mm)			128-pin LQFP (14 × 20 mm)		
Operating ambient temperature		–40°C to +85°C			–40°C to +85°C		

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850E/IG4-H			V850E/IH4-H		
Part No.		μPD70F3919	μPD70F3920	μPD70F3921	μPD70F3922	μPD70F3923	μPD70F3924
CPU name		V850E1			V850E1		
CPU performance (Dhrystone)		197 MIPS (@ 100 MHz)			197 MIPS (@ 100 MHz)		
Internal ROM		256 KB (flash)	384 KB (flash)	480 KB (flash)	256 KB (flash)	384 KB (flash)	480 KB (flash)
Internal RAM		24 KB			24 KB		
External bus interface	Bus type	Multiplexed			Multiplexed/separate		
	Address bus	16 bits			Multiplexed: 16 bits, separate: 8 bits		
	Data bus	8/16 bits			8/16 bits		
	Chip select signal	2			2		
Memory controller		SRAM, etc. (5 V interface)			SRAM, etc.		
Interrupt sources	Internal	84 (Including one NMI)			84 (Including one NMI)		
	External	22 (22)*			22 (22)*		
Timer/counter		16-bit timer/event counter (TAB) × 2 ch (3-phase inverter control PWM timer compatible) 16-bit timer/event counter (TAA) × 1 ch 16-bit timer/event counter (TMT) × 4 ch (encoder count function: 2 ch) 16-bit timer/counter (TAA) × 2 ch 16-bit interval timer (TMM) × 4 ch			16-bit timer/event counter (TAB) × 2 ch (3-phase inverter control PWM timer compatible) 16-bit timer/event counter (TAA) × 1 ch 16-bit timer/event counter (TMT) × 4 ch (encoder count function: 2 ch) 16-bit timer/counter (TAA) × 2 ch 16-bit interval timer (TMM) × 4 ch		
Watchdog timer		1 ch			1 ch		
Serial interface		CSI/UART (With FIFO) × 1 ch CSI/UART × 2 ch UART/I²C × 1 ch			CSI/UART (With FIFO) × 1 ch CSI/UART × 2 ch UART/I²C × 1 ch		
A/D converter		12 bits × 4 ch (A/D converter 0), 12 bits × 3 ch (A/D converter 1) (conversion time: 2 μs) 10 bits × 12 ch			12 bits × 4 ch, 2 units (conversion time: 2 μs) 10 bits × 12 ch		
D/A converter		–			–		
DMA controller		7 ch			7 ch		
Ports	I/O	51			68		
	Input	12			12		
Debug control unit		Provided (RUN/break)			Provided (RUN/break/trace)		
USB controller		USB 2.0 function (full-speed) × 1 ch			USB 2.0 function (full-speed) × 1 ch		
Other peripheral functions		3-phase inverter control, 6 operational amplifiers, comparators: 12 circuits, software pull-up, POC/LVI/clock monitor			3-phase inverter control, 6 operational amplifiers, comparators: 12 circuits, software pull-up, POC/LVI/clock monitor		
Operating frequency		10 to 100 MHz			10 to 100 MHz		
Power supply voltage		1.5 V (internal)/5.0 V (pin, A/D)/3.3 V (USB)			1.5 V (internal)/5.0 V (A/D)/3.3 V (pin, USB)		
Package		100-pin LQFP (14 × 14 mm)			128-pin LQFP (14 × 20 mm)		
Operating ambient temperature		–40°C to +85°C			–40°C to +85°C		

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

ASSP Lineup (Inverter Control, etc.) (2/5)

Generic Name		V850E/IG3		V850E/IF3	
Part No.		μPD70F3453	μPD70F3454	μPD70F3451	μPD70F3452
CPU name		V850E1		V850E1	
CPU performance (Dhrystone)		131 MIPS (@ 64 MHz)		131 MIPS (@ 64 MHz)	
Internal ROM		128 KB (flash)	256 KB (flash)	128 KB (flash)	256 KB (flash)
Internal RAM		8 KB	12 KB	8 KB	12 KB
External bus interface	Bus type	–	Multiplexed/separate *1	–	
	Address bus	–	Multiplexed: 16 bits, separate: 8 bits*1	–	
	Data bus	–	8/16 bits*1	–	
	Chip select signal	–	2*1	–	
Memory controller		–	SRAM, etc.*1	–	
Interrupt sources	Internal	75 (including one NMI)		74 (including one NMI)	
	External	21 (18)*2		15 (12)*2	
Timer/counter		16-bit timer/event counter (TAB) × 2 ch (3-phase inverter control PWM timer compatible) 16-bit timer/event counter (TAA) × 3 ch 16-bit timer/event counter (TMT) × 2 ch (encoder count function: 2 ch) 16-bit timer/counter (TAA) × 2 ch 16-bit interval timer (TMM) × 4 ch		16-bit timer/event counter (TAB) × 2 ch (3-phase inverter control PWM timer compatible) 16-bit timer/event counter (TAA) × 3 ch 16-bit timer/event counter (TMT) × 2 ch (encoder count function: 1 ch) 16-bit timer/counter (TAA) × 2 ch 16-bit interval timer (TMM) × 4 ch	
Watchdog timer		1 ch		1 ch	
Serial interface		CSI/UART (with FIFO) × 1 ch CSI/UART × 2 ch UART/I²C × 1 ch		CSI/UART (with FIFO) × 1 ch CSI/UART × 2 ch UART/I²C × 1 ch	
A/D converter		12 bits × 5 ch, 2 units (conversion time: 2 μs) 10 bits × 8 ch		12 bits × 5 ch, 2 units (conversion time: 2 μs) 10 bits × 4 ch	
D/A converter		–		–	
DMA controller		4 ch		4 ch	
Ports	I/O	56		44	
	Input	8		4	
Debug control unit		Provided (RUN/break)		–	
Other peripheral functions		3-phase inverter control, 4 operational amplifiers, comparators: 8 circuits, software pull-up, POC/LVI/clock monitor		3-phase inverter control, 4 operational amplifiers, comparator: 8 circuits, software pull-up, POC/LVI/clock monitor	
Operating frequency		4 to 64 MHz		4 to 64 MHz	
Power supply voltage		3.5 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)		3.5 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)	
Package		100-pin LQFP (14 × 14 mm) 100-pin LQFP (14 × 20 mm) 161-pin FBGA (10 × 10 mm)*3		80-pin LQFP (14 × 14 mm)	
Operating ambient temperature		–40°C to +85°C		–40°C to +85°C	

*1. μPD70F3454GC-8EA-A only

*2. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

*3. μPD70F3454F1-DA9-A only

Generic Name		V850E/MA3					
Part No.		μPD703131BY	μPD703132BY	μPD703133BY	μPD703134BY	μPD70F3134BY	μPD703136BY
CPU name		V850E1					
CPU performance (Dhrystone)		158 MIPS (@ 80 MHz)					
Internal ROM		256 KB (mask)		512 KB (mask)		512 KB (flash)	256 KB (mask)
Internal RAM		16 KB	32 KB	16 KB	32 KB		8 KB
External bus interface	Bus type	Multiplexed/separate					
	Address bus	26 bits					
	Data bus	8/16 bits					
	Chip select signal	8					
Memory controller		SDRAM, SRAM, etc.					
Interrupt sources	Internal	41 (including one NMI)					
	External	26 (26)* (including one NMI)					
Timer/counter		16-bit interval timer (TMD) × 4 ch 16-bit timer/event counter (TMP) × 3 ch 16-bit timer/event counter (TMQ) × 1 ch (3-phase inverter control PWM timer compatible) 16-bit encoder counter/timer (TMENC) × 1 ch					
Watchdog timer		1 ch					
Serial interface		CSI/UART × 3 ch UART/I²C × 1 ch					
A/D converter		10 bits × 8 ch					
D/A converter		8 bits × 2 ch					
DMA controller		4 ch					
Ports	I/O	101					
	Input	11					
Debug control unit		Provided (RUN/break)					
Other peripheral functions		3-phase inverter control, ROM correction: 4 points					
Operating frequency		5 to 80 MHz					
Power supply voltage		2.3 V to 2.7 V (internal)/3.0 V to 3.6 V (external)					
Package		144-pin LQFP (20 × 20 mm) 161-pin FBGA (13 × 13 mm)					
Operating ambient temperature		–40°C to +85°C					

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

ASSP Lineup (Inverter Control, etc.) (3/5)

Generic Name		V850E/IA4			V850E/IA3	
Part No.		μPD703185	μPD703186	μPD70F3186	μPD703183	μPD70F3184
CPU name		V850E1			V850E1	
CPU performance (Dhrystone)		126 MIPS (@ 64 MHz)			126 MIPS (@ 64 MHz)	
Internal ROM		128 KB (mask)	256 KB (mask)	256 KB (flash)	128 KB (mask)	256 KB (flash)
Internal RAM		6 KB	12 KB		6 KB	12 KB
External bus interface	Bus type	–			–	
	Address bus	–			–	
	Data bus	–			–	
	Chip select signal	–			–	
Memory controller		–			–	
Interrupt sources	Internal	53 (including one NMI)			49 (including one NMI)	
	External	8 (7)*			7 (6)*	
Timer/counter		16-bit timer/event counter (TMQ) × 2 ch (3-phase inverter control PWM timer compatible) 16-bit encoder counter/timer (TMENC) × 2 ch 16-bit timer/event counter (TMP) × 2 ch 16-bit timer/counter (TMP) × 2 ch 16-bit interval timer (TMM) × 1 ch			16-bit timer/event counter (TMQ) × 1 ch (3-phase inverter control PWM timer compatible) 16-bit encoder counter/timer (TMENC) × 1 ch 16-bit timer/event counter (TMP) × 2 ch 16-bit timer/event counter (TMQ) × 1 ch 16-bit timer/counter (TMP) × 2 ch 16-bit interval timer (TMM) × 1 ch	
Watchdog timer		1 ch			1 ch	
Serial interface		CSI × 1 ch UART × 1 ch CSI/UART × 1 ch			CSI × 1 ch UART × 1 ch CSI/UART × 1 ch	
A/D converter		10 bits × 4 ch, 2 units (conversion time: 2 μs) 8/10 bits × 8 ch			10 bits × 4 ch, 10 bits × 2 ch (conversion time: 2 μs) 8/10 bits × 6 ch	
D/A converter		–			–	
DMA controller		4 ch			4 ch	
Ports	I/O	56			44	
	Input	8			6	
Debug control unit		–		Provided (RUN/break)	–	
Other peripheral functions		3-phase inverter control, ROM correction: 4 points, operational amplifiers: 6 circuits, comparators: 6 circuits, software pull-up			3-phase inverter control, ROM correction: 4 points, operational amplifiers: 5 circuits, comparators: 5 circuits, software pull-up	
Operating frequency		4 to 64 MHz			4 to 64 MHz	
Power supply voltage		2.3 V to 2.7 V (internal)/4.0 V to 5.5 V (external) (A/D converter: 4.5 V to 5.5 V)			2.3 V to 2.7 V (internal)/4.0 V to 5.5 V (external) (A/D converter: 4.5 V to 5.5 V)	
Package		100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)			80-pin QFP (14 × 14 mm)	
Operating ambient temperature		–40°C to +85°C			–40°C to +85°C	

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850E/IA1		V850E/IA2	
Part No.		μPD703116	μPD70F3116	μPD703114	μPD70F3114
CPU name		V850E1		V850E1	
CPU performance (Dhrystone)		103 MIPS (@ 50 MHz)		82 MIPS (@ 40 MHz)	
Internal ROM		256 KB (mask)	256 KB (flash)	128 KB (mask)	128 KB (flash)
Internal RAM		10 KB		6 KB	
External bus interface	Bus type	Multiplexed		Multiplexed	
	Address bus	24 bits		22 bits	
	Data bus	8/16 bits		8/16 bits	
	Chip select signal	8		–	
Memory controller		SRAM, etc.		SRAM, etc.	
Interrupt sources	Internal	45		42	
	External	20 (14)* (including one NMI)		16 (12)* (including one NMI)	
Timer/counter		16-bit 3-phase inverter control PWM timer × 2 ch 16-bit encoder counter/timer × 2 ch 16-bit timer/counter × 2 ch 16-bit timer/event counter × 1 ch 16-bit interval timer × 1 ch		16-bit 3-phase inverter control PWM timer × 2 ch 16-bit encoder counter/timer × 1 ch 16-bit timer/counter × 2 ch 16-bit timer/event counter × 1 ch 16-bit interval timer × 1 ch	
Watchdog timer		–		–	
Serial interface		CSI × 2 ch UART × 3 ch		CSI × 1 ch CSI/UART × 1 ch UART × 1 ch	
A/D converter		10 bits × 8 ch, 2 units		10 bits × 6 ch (A/D converter 0) 10 bits × 8 ch (A/D converter 1)	
D/A converter		–		–	
DMA controller		4 ch		4 ch	
Ports	I/O	75		47	
	Input	8		6	
Debug control unit		–		–	
Other peripheral functions		CAN controller × 1 ch		–	
Operating frequency		4 to 50 MHz		4 to 40 MHz	
Power supply voltage		3.0 V to 3.6 V (internal) 4.5 V to 5.5 V (external)		4.5 V to 5.5 V (when internal regulator used)	
Package		144-pin LQFP (20 × 20 mm)		100-pin QFP (14 × 20 mm) 100-pin LQFP (14 × 14 mm)	
Operating ambient temperature		–40°C to +85°C (110°C version available)		–40°C to +85°C	

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

ASSP Lineup (Inverter Control, etc.) (4/5)

Generic Name		V850ES/HE3	V850ES/HF3
Part No.		μPD70F3747	μPD70F3750
CPU name		V850ES	V850ES
CPU performance (Dhrystone)		69 MIPS (@ 32 MHz)	69 MIPS (@ 32 MHz)
Internal ROM		128 KB (flash)	256 KB (flash)
Internal RAM		8 KB	16 KB
External bus interface	Bus type	–	–
	Address bus	–	–
	Data bus	–	–
	Chip select signal	–	–
Memory controller		–	–
Interrupt sources	Internal	43 (including one NMI)	43 (including one NMI)
	External	9 (9)* (including one NMI)	9 (9)* (including one NMI)
Timer/counter		16-bit timer/event counter (TAA) × 5 ch 16-bit timer/event counter (TAB) × 1 ch (3-phase inverter control PWM timer compatible) 16-bit interval timer (TMM) × 1 ch	16-bit timer/event counter (TAA) × 5 ch 16-bit timer/event counter (TAB) × 1 ch (3-phase inverter control PWM timer compatible) 16-bit interval timer (TMM) × 1 ch
Watchdog timer		1 ch	1 ch
Serial interface		CSI × 2 ch UART (LIN compatible) × 2 ch I^2C × 1 ch	CSI × 2 ch UART (LIN compatible) × 2 ch I^2C × 1 ch
A/D converter		10 bits × 10 ch	10 bits × 12 ch
D/A converter		–	–
DMA controller		4 ch	4 ch
Ports	I/O	51	67
	Input	–	–
Debug control unit		Provided (RUN/break)	Provided (RUN/break)
Other peripheral functions		3-phase inverter control, watch timer: 1 ch, POC/LVI/clock monitor, RAM retention flag, SSCG	3-phase inverter control, watch timer: 1 ch, POC/LVI/clock monitor, RAM retention flag, SSCG
Operating frequency		When using main clock: 4 to 32 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz	When using main clock: 4 to 32 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz
Power supply voltage		3.7 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)	3.7 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)
Package		64-pin LQFP (10 × 10 mm)	80-pin LQFP (12 × 12 mm)
Operating ambient temperature		–40°C to +85°C	–40°C to +85°C

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850ES/HG3	V850ES/HJ3	
Part No.		μPD70F3752	μPD70F3755	μPD70F3757
CPU name		V850ES	V850ES	
CPU performance (Dhrystone)		69 MIPS (@ 32 MHz)	69 MIPS (@ 32 MHz)	66 MIPS (@ 32 MHz)
Internal ROM		256 KB (flash)	256 KB (flash)	512 KB (flash)
Internal RAM		16 KB	16 KB	32 KB
External bus interface	Bus type	–	Multiplexed	
	Address bus	–	16 bits	
	Data bus	–	8/16 bits	
	Chip select signal	–	4	
Memory controller		–	SRAM, etc.	
Interrupt sources	Internal	51 (including one NMI)	58 (including one NMI)	64 (including one NMI)
	External	12 (12)*1 (including one NMI)	16 (16)*1 (including one NMI)	
Timer/counter		16-bit timer/event counter (TAA) × 5 ch 16-bit timer/event counter (TAB) × 2 ch (3-phase inverter control PWM timer compatible) 16-bit interval timer (TMM) × 1 ch	16-bit timer/event counter (TAA) × 5 ch 16-bit timer/event counter (TAB) × 3 ch (3-phase inverter control PWM timer compatible) 16-bit interval timer (TMM) × 1 ch	
Watchdog timer		1 ch	1 ch	
Serial interface		CSI × 2 ch UART (LIN compatible) × 3 ch I^2C × 1 ch	CSI × 3 ch UART (LIN compatible) × 3 ch I^2C × 1 ch	CSI × 1 ch UART (LIN compatible) × 4 ch UART (LIN compatible)/CSI × 2 ch*2 UART (LIN compatible)/I^2C × 1 ch
A/D converter		10 bits × 16 ch	10 bits × 24 ch	
D/A converter		–	–	
DMA controller		4 ch	4 ch	
Ports	I/O	84	128	
	Input	–	–	
Debug control unit		Provided (RUN/break)	Provided (RUN/break)	
Other peripheral functions		3-phase inverter control, watch timer: 1 ch, POC/LVI/clock monitor, RAM retention flag, SSCG	3-phase inverter control, watch timer: 1 ch, POC/LVI/clock monitor, RAM retention flag, SSCG	
Operating frequency		When using main clock: 4 to 32 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz	When using main clock: 4 to 32 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz	
Power supply voltage		3.7 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)	3.7 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)	
Package		100-pin LQFP (14 × 14 mm)	144-pin LQFP (20 × 20 mm)	
Operating ambient temperature		–40°C to +85°C	–40°C to +85°C	

*1. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*2. Two channels identical to independent UART are available. The V850ES/HJ3 has a total of 6 UART channels.

ASSP Lineup (Inverter Control, etc.) (5/5)

Generic Name		V850ES/IK1		V850ES/IE2	
Part No.		μPD703327	μPD703329 μPD70F3329	μPD70F3713	μPD70F3714
CPU name		V850ES		V850ES	
CPU performance (Dhrystone)		63 MIPS (@ 32 MHz)		39 MIPS (@ 20 MHz)	
Internal ROM		64 KB (mask)	128 KB (mask) 128 KB (flash)	64 KB (flash)	128 KB (flash)
Internal RAM		4 KB	6 KB	6 KB	6 KB
External bus interface	Bus type	–		–	
	Address bus	–		–	
	Data bus	–		–	
	Chip select signal	–		–	
Memory controller		–		–	
Interrupt sources	Internal	36 (including one NMI)		36 (including one NMI)	
	External	7 (6)*		7 (6)*	
Timer/counter		16-bit timer/event counter (TMQ) × 1 ch (3-phase inverter control PWM timer compatible) 16-bit timer/event counter (TMP) × 2 ch 16-bit timer/event counter (TMQ) × 1 ch 16-bit timer/counter (TMP) × 2 ch 16-bit interval timer (TMM) × 1 ch		16-bit timer/event counter (TMQ) × 1 ch (3-phase inverter control PWM timer compatible) 16-bit timer/event counter (TMP) × 2 ch 16-bit timer/event counter (TMQ) × 1 ch 16-bit timer/counter (TMP) × 2 ch 16-bit interval timer (TMM) × 1 ch	
Watchdog timer		1 ch		1 ch	
Serial interface		CSI × 1 ch UART × 2 ch		CSI × 1 ch UART × 2 ch	
A/D converter		10 bits × 4 ch, 2 units (conversion time: 2 μs)		10 bits × 4 ch, 2 units (conversion time: 3.1 μs)	
D/A converter		–		–	
DMA controller		–		–	
Ports	I/O	39		39	
	Input	–		–	
Debug control unit		–		–	
Other peripheral functions		3-phase inverter control, ROM correction: 4 points, software pull-up, POC/LVI/clock monitor		3-phase inverter control, software pull-up, POC/LVI/clock monitor	
Operating frequency		2.5 to 32 MHz		2.5 to 20 MHz	
Power supply voltage		3.5 V to 5.5 V (A/D converter: 4.5 V to 5.5 V)		3.5 V to 5.5 V (A/D converter: 4.5 V to 5.5 V)	
Package		64-pin LQFP (14 × 14 mm)		64-pin LQFP (14 × 14 mm)	
Operating ambient temperature		−40°C to +85°C		−40°C to +85°C	

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Empower your creativity
V850 Embedded Controller

ASSP Lineup (Dashboard Control, Body Control) (1/10)

Generic Name		V850E/DG3		V850E/DJ3		
Part No.		μPD70F3416	μPD70F3417	μPD70F3421	μPD70F3422	μPD70F3423
CPU name		V850E1		V850E1		
CPU performance (Dhrystone)		34 MIPS (@ 16 MHz)		69 MIPS (@ 32 MHz)		
Internal ROM		128 KB (flash)	256 KB (flash)	256 KB (flash)	384 KB (flash)	512 KB (flash)
Internal RAM		6 KB	12 KB	12 KB	16 KB	20 KB
External bus interface	Bus type	–		–		
	Address bus	–		–		
	Data bus	–		–		
	Chip select signal	–		–		
Memory controller		–		–		
Interrupt sources	Internal	48 (including one NMI)		75 (including one NMI)		
	External	5 (5)* (including one NMI)		8 (8)* (including one NMI)		
Timer/counter		16-bit timer/event counter (TMP) × 1 ch 16-bit timer/event counter (TMG) × 2 ch 16-bit interval timer (TMZ) × 4 ch		16-bit timer/event counter (TMP) × 4 ch 16-bit timer/event counter (TMG) × 3 ch 16-bit interval timer (TMZ) × 6 ch		
Watchdog timer		1 ch		1 ch		
Serial interface		CSI × 1 ch I^2C × 1 ch UART (LIN compatible) × 2 ch		CSI × 2 ch I^2C × 2 ch UART (LIN compatible) × 2 ch		
A/D converter		10 bits × 8 ch		10 bits × 12 ch		
D/A converter		–		–		
DMA controller		–		4 ch		
Ports	I/O	72		98		
	Input	8		16		
Debug control unit		–		Provided (RUN/break)		
Other peripheral functions		Watch timer: 1 ch Meter driver: 4 ch ROM correction: 6 points, POC/clock monitor, SSCG Sound generator LCD controller/driver CAN controller: 1 ch		Watch timer: 1 ch Meter driver: 6 ch ROM correction: 8 points, POC/clock monitor, SSCG Voltage comparator Sound generator LCD controller/driver CAN controller: 2 ch		
Operating frequency		When using main clock: 4 to 16 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 240 kHz		When using main clock: 4 to 32 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 240 kHz		
Power supply voltage		3.2 V to 5.5 V (A/D converter: 3.5 V to 5.5 V)		3.2 V to 5.5 V (A/D converter: 3.5 V to 5.5 V)		
Package		100-pin LQFP (14 × 14 mm)		144-pin LQFP (20 × 20 mm)		
Operating ambient temperature		−40°C to +85°C		−40°C to +85°C		

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850E/DJ3			V850E/DL3
Part No.		μPD70F3424	μPD70F3425	μPD70F3426	μPD70F3427
CPU name		V850E1			V850E1
CPU performance (Dhrystone)		126 MIPS (@ 64 MHz)			126 MIPS (@ 64 MHz)
Internal ROM		512 KB (flash)	1024 KB (flash)	2048 KB (flash)	1024 KB (flash)
Internal RAM		24 KB	32 KB	84 KB	60 KB
External bus interface	Bus type	–			Separate
	Address bus	–			24 bits
	Data bus	–			8/16/32 bits
	Chip select signal	–			4
Memory controller		–			SRAM, etc.
Interrupt sources	Internal	82 (including one NMI)			82 (including one NMI)
	External	9 (9)* (including one NMI)			9 (9)* (including one NMI)
Timer/counter		16-bit timer/event counter (TMP) × 4 ch 16-bit timer/event counter (TMG) × 3 ch 16-bit interval timer (TMZ) × 10 ch			16-bit timer/event counter (TMP) × 4 ch 16-bit timer/event counter (TMG) × 3 ch 16-bit interval timer (TMZ) × 10 ch
Watchdog timer		1 ch			1 ch
Serial interface		CSI × 3 ch I^2C × 2 ch UART (LIN compatible) × 2 ch			CSI × 3 ch I^2C × 2 ch UART (LIN compatible) × 2 ch
A/D converter		10 bits × 16 ch			10 bits × 16 ch
D/A converter		–			–
DMA controller		4 ch			4 ch
Ports	I/O	98			101
	Input	16			16
Debug control unit		Provided (RUN/break)			Provided (RUN/break)
Other peripheral functions		Watch timer: 1 ch Meter driver: 6 ch ROM correction: 8 points, POC/clock monitor, SSCG Voltage comparator Sound generator LCD bus interface CAN controller: 2 ch			Watch timer: 1 ch Meter driver: 6 ch ROM correction: 8 points, POC/clock monitor SSCG, Voltage comparator Sound generator LCD bus interface CAN controller: 2 ch
Operating frequency		When using main clock: 4 to 64 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 240 kHz			When using main clock: 4 to 64 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 240 kHz
Power supply voltage		3.2 V to 5.5 V (A/D converter: 3.5 V to 5.5 V)			3.2 V to 5.5 V (A/D converter: 3.5 V to 5.5 V)
Package		144-pin LQFP (20 × 20 mm)			208-pin LQFP (28 × 28 mm)
Operating ambient temperature		−40°C to +85°C			−40°C to +85°C

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

ASSP Lineup (Dashboard Control, Body Control) (2/10)

Generic Name		V850E2/FE4-L (Under development)			V850E2/FF4-L (Under development)		
Part No.		μPD70F3570	μPD70F3571	μPD70F3572	μPD70F3573	μPD70F3574	μPD70F3575
CPU name		V850E2S			V850E2S		
CPU performance (Dhrystone)		82 MIPS (@ 48 MHz)			82 MIPS (@ 48 MHz)		
Internal ROM		256 KB (flash)	384 KB (flash)	512 KB (flash)	256 KB (flash)	384 KB (flash)	512 KB (flash)
Internal RAM		24 KB	28 KB	32 KB	24 KB	28 KB	32 KB
Data flash		32 KB			32 KB		
External bus interface	Bus type	–			–		
	Address bus	–			–		
	Data bus	–			–		
	Chip select signal	–			–		
Memory controller		–			–		
Interrupt sources	External	9			9		
Timer/counter		32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 1 unit			32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 1 unit		
Watchdog timer		2 ch			2 ch		
Serial interface		UART (LIN compatible) × 2 ch CSI × 2 ch I²C × 1 ch CAN controller × 1 ch			UART (LIN compatible) × 2 ch CSI × 2 ch I²C × 1 ch CAN controller × 1 ch		
A/D converter		10 bits × 12 ch			10 bits × 14 ch		
D/A converter		–			–		
DMA controller		8 ch			8 ch		
Ports	I/O	43			57		
	Input	–			–		
Debug control unit		Provided (RUN/break/trace)			Provided (RUN/break/trace)		
Other peripheral functions		POC, LVI, clock monitor, key return: 8 ch			POC, LVI, clock monitor, key return: 8 ch		
Operating frequency		When using main clock: 48 MHz (max.) When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz			When using main clock: 48 MHz (max.) When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz		
Power supply voltage		3.0 V to 5.5 V			3.0 V to 5.5 V		
Package		64-pin LQFP (10 × 10 mm)			80-pin LQFP (12 × 12 mm)		
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C			–40°C to +85°C, –40°C to +110°C, –40°C to +125°C		

Generic Name		V850E2/FG4-L (Under development)				
Part No.		μPD70F3576	μPD70F3577	μPD70F3578	μPD70F3579	μPD70F3580
CPU name		V850E2S				
CPU performance (Dhrystone)		82 MIPS (@ 48 MHz)			109 MIPS (@ 64 MHz)	
Internal ROM		256 KB (flash)	384 KB (flash)	512 KB (flash)	768 KB (flash)	1 MB (flash)
Internal RAM		24 KB	28 KB	32 KB	48 KB	64 KB
Data flash		32 KB				
External bus interface	Bus type	–				
	Address bus	–				
	Data bus	–				
	Chip select signal	–				
Memory controller		–				
Interrupt sources	External	13 ch				
Timer/counter		32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 1 unit				
Watchdog timer		2 ch				
Serial interface		UART (LIN compatible) × 3 ch CSI × 3 ch I²C × 1 ch CAN controller × 2 ch				
A/D converter		10 bits × 20 ch				
D/A converter		–				
DMA controller		8 ch				
Ports	I/O	75				
	Input	–				
Debug control unit		Provided (RUN/break/trace)				
Other peripheral functions		POC, LVI, clock monitor, key return: 8 ch				
Operating frequency		When using main clock: 48 MHz (max.) When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz			When using main clock: 64 MHz (max.) When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz	
Power supply voltage		3.0 V to 5.5 V				
Package		100-pin LQFP (14 × 14 mm)				
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C				

ASSP Lineup (Dashboard Control, Body Control) (3/10)

Generic Name		V850E2/FJ4-L (Under development)					
Part No.		μPD70F3581	μPD70F3582	μPD70F3583	μPD70F3584	μPD70F3585	μPD70F3586
CPU name		V850E2S					
CPU performance (Dhrystone)		82 MIPS (@ 48 MHz)			109 MIPS (@ 64 MHz)		
Internal ROM		256 KB (flash)	384 KB (flash)	512 KB (flash)	768 KB (flash)	1 MB (flash)	1.5 MB (flash)
Internal RAM		24 KB	28 KB	32 KB	48 KB	64 KB	96 KB
Data flash		32 KB					
External bus interface	Bus type	–					
	Address bus	–					
	Data bus	–					
	Chip select signal	–					
Memory controller		–					
Interrupt sources	External	16					
Timer/counter		32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 2 units					
Watchdog timer		2 ch					
Serial interface		UART (LIN compatible) × 3 ch CSI × 3 ch I²C × 1 ch CAN controller × 2 ch		UART (LIN compatible) × 5 ch CSI × 3 ch I²C × 1 ch CAN controller × 2 ch			
A/D converter		10 bits × 24 ch					
D/A converter		–					
DMA controller		8 ch					
Ports	I/O	118					
	Input	–					
Debug control unit		Provided (RUN/break/trace)					
Other peripheral functions		POC, LVI, clock monitor, key return: 8 ch					
Operating frequency		When using main clock: 48 MHz (max.) When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz			When using main clock: 64 MHz (max.) When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz		
Power supply voltage		3.0 V to 5.5 V					
Package		144-pin LQFP (20 × 20 mm)					
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C					

Generic Name		V850E2/FK4-L (Under development)		
Part No.		μPD70F3587	μPD70F3588	μPD70F3589
CPU name		V850E2S		
CPU performance (Dhrystone)		109 MIPS (@ 64 MHz)		
Internal ROM		768 KB (flash)	1 MB (flash)	1.5 MB (flash)
Internal RAM		48 KB	64 KB	96 KB
Data flash		32 KB		
External bus interface	Bus type	–		
	Address bus	–		
	Data bus	–		
	Chip select signal	–		
Memory controller		–		
Interrupt sources	External	17		
Timer/counter		32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 2 units		
Watchdog timer		2 ch		
Serial interface		UART (LIN compatible) × 5 ch CSI × 4 ch I²C × 1 ch CAN controller × 2 ch		
A/D converter		10 bits × 24 ch		
D/A converter		–		
DMA controller		8 ch		
Ports	I/O	143		
	Input	–		
Debug control unit		Provided (RUN/break/trace)		
Other peripheral functions		POC, LVI, clock monitor, key return: 8 ch		
Operating frequency		When using main clock: 64 MHz (max.) When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz		
Power supply voltage		3.0 V to 5.5 V		
Package		176-pin LQFP (24 × 24 mm)		
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C		

ASSP Lineup (Dashboard Control, Body Control) (4/10)

Generic Name		V850E2/FG4 (Under development)					
Part No.		μPD70F3548	μPD70F4000	μPD70F3549	μPD70F4001	μPD70F3550	μPD70F4002
CPU name		V850E2M					
CPU performance (Dhrystone)		162 MIPS (@ 80 MHz)					
Internal ROM		512 KB (flash)		768 KB (flash)		1 MB (flash)	
Internal RAM		48 KB		64 KB		80 KB	
Data flash		32 KB					
External bus interface	Bus type	–					
	Address bus	–					
	Data bus	–					
	Chip select signal	–					
Memory controller		–					
Interrupt sources	Internal	104	108	104	108	104	108
	External	13					
Timer/counter		32-bit timer: 4 ch × 2 units 16-bit timer: 16 ch × 2 units					
Watchdog timer		2 ch					
Serial interface		UART (LIN compatible) × 5 ch CSI × 2 ch CSI (With FIFO) × 1 ch I^2C × 1 ch CAN controller × 2 ch FlexRay controller × 2 ch × 1 unit*					
A/D converter		12 bits × 20 ch					
D/A converter		–					
DMA controller		8 ch					
Ports	I/O	72					
	Input	–					
Debug control unit		Provided (RUN/break/trace)					
Other peripheral functions		POC, LVI, clock monitor, comparator, random number generator, data CRC, key return: 8 ch					
Operating frequency		When using main clock: 80 MHz (max.) When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz					
Power supply voltage		3.0 V to 5.5 V					
Package		100-pin LQFP (14 × 14 mm)					
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C					

* μPD70F4000/4001/4002 only

Generic Name		V850E2/FJ4 (Under development)							
Part No.		μPD70F3551	μPD70F4003	μPD70F3552	μPD70F4004	μPD70F3553	μPD70F4005	μPD70F3554	μPD70F4006
CPU name		V850E2M							
CPU performance (Dhrystone)		162 MIPS (@ 80 MHz)							
Internal ROM		512 KB (flash)		768 KB (flash)		1 MB (flash)		1.5 MB (flash)	
Internal RAM		48 KB		64 KB		80 KB		112 KB	
Data flash		32 KB						64 KB	
External bus interface	Bus type	–							
	Address bus	–							
	Data bus	–							
	Chip select signal	–							
Memory controller		–							
Interrupt sources	Internal	166	170	166	170	166	170	166	170
	External	16							
Timer/counter		32-bit timer: 4 ch × 2 units 16-bit timer: 16 ch × 6 units							
Watchdog timer		2 ch							
Serial interface		UART (LIN compatible) × 6 ch CSI × 2 ch CSI (With FIFO) × 2 ch I^2C × 1 ch CAN controller × 3 ch FlexRay controller × 2 ch × 1 unit*							
A/D converter		12 bits × 24 ch							
D/A converter		–							
DMA controller		8							
Ports	I/O	109							
	Input	–							
Debug control unit		Provided (RUN/break/trace)							
Other peripheral functions		POC, LVI, clock monitor, comparator × 2, random number generator, data CRC, key return: 8 ch							
Operating frequency		When using main clock: 80 MHz (max.) When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz							
Power supply voltage		3.0 V to 5.5 V							
Package		144-pin HLQFP (20 × 20 mm)							
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C							

* μPD70F4003/4004/4005/4006 only

ASSP Lineup (Dashboard Control, Body Control) (5/10)

Generic Name		V850E2/FK4 (Under development)							
Part No.		μPD70F3555	μPD70F4007	μPD70F3556	μPD70F4008	μPD70F3557	μPD70F4009	μPD70F3558	μPD70F4010
CPU name		V850E2M							
CPU performance (Dhrystone)		162 MIPS (@ 80 MHz)							
Internal ROM		768 KB (flash)		1 MB (flash)		1.5 MB (flash)		2 MB (flash)	
Internal RAM		64 KB		80 KB		112 KB		144 KB	
Data flash		32 KB				64 KB			
External bus interface	Bus type	–							
	Address bus	–							
	Data bus	–							
	Chip select signal	–							
Memory controller		–							
Interrupt sources	Internal	181	185	181	185	181	185	181	185
	External	17							
Timer/counter		32-bit timer: 4 ch × 2 units 16-bit timer: 16 ch × 7 units							
Watchdog timer		2 ch							
Serial interface		UART (LIN compatible) × 8 ch CSI × 2 ch CSI (With FIFO) × 3 ch I^2C × 1 ch CAN controller × 4 ch FlexRay controller × 2 ch × 1 unit*							
A/D converter		12 bits × 24 ch × 1 unit, 12 bits × 16 ch × 1 unit							
D/A converter		–							
DMA controller		8							
Ports	I/O	134							
	Input	–							
Debug control unit		Provided (RUN/break/trace)							
Other peripheral functions		POC, LVI, clock monitor, comparator × 2, random number generator, data CRC, key return: 8 ch							
Operating frequency		When using main clock: 80 MHz (max.) When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz							
Power supply voltage		3.0 V to 5.5 V							
Package		176-pin HLQFP (24 × 24 mm)							
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C							

* μPD70F4007/4008/4009/4010 only

Generic Name		V850E2/FL4 (Under development)			
Part No.		μPD70F3559	μPD70F4011	μPD70F3560	μPD70F4012
CPU name		V850E2M			
CPU performance (Dhrystone)		162 MIPS (@ 80 MHz)			
Internal ROM		1.5 MB (flash)		2 MB (flash)	
Internal RAM		112 KB		144 KB	
Data flash		64 KB			
External bus interface	Bus type	–			
	Address bus	–			
	Data bus	–			
	Chip select signal	–			
Memory controller		–			
Interrupt sources	Internal	196	200	196	200
	External	17			
Timer/counter		32-bit timer: 4 ch × 2 units 16-bit timer: 16 ch × 8 units			
Watchdog timer		2 ch			
Serial interface		UART (LIN compatible) × 12 ch CSI × 2 ch CSI (With FIFO) × 3 ch I^2C × 1 ch CAN controller × 5 ch FlexRay controller × 2 ch × 1 unit*			
A/D converter		12 bits × 24 ch × 2 units			
D/A converter		–			
DMA controller		8			
Ports	I/O	164			
	Input	–			
Debug control unit		Provided (RUN/break/trace)			
Other peripheral functions		POC, LVI, clock monitor, comparator × 2, random number generator, data CRC, key return: 8 ch			
Operating frequency		When using main clock: 80 MHz (max.) When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz			
Power supply voltage		3.0 V to 5.5 V			
Package		208-pin QFP (28 × 28 mm), 256-pin PBGA (21 × 21 mm)			
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C			

* μPD70F4011/4012 only

ASSP Lineup (Dashboard Control, Body Control) (6/10)

Generic Name		V850E2/FE4-M (Under development)			V850E2/FF4-M (Under development)		
Part No.		μPD70F3540	μPD70F3541	μPD70F3542	μPD70F3543	μPD70F3544	μPD70F3545
CPU name		V850E2M			V850E2M		
CPU performance (Dhrystone)		205 MIPS (@ 80 MHz)			205 MIPS (@ 80 MHz)		
Internal ROM		256 KB (flash)	384 KB (flash)	512 KB (flash)	256 KB (flash)	384 KB (flash)	512 KB (flash)
Internal RAM		32 KB	40 KB	48 KB	32 KB	40 KB	48 KB
Data flash		32 KB			32 KB		
External bus interface	Bus type	–			–		
	Address bus	–			–		
	Data bus	–			–		
	Chip select signal	–			–		
Memory controller		–			–		
Interrupt sources	Internal	84			84		
	External	11			12		
Timer/counter		32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 2 units			32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 2 units		
Watchdog timer		2 ch			2 ch		
Serial interface		UART (LIN compatible) × 3 ch CSI × 2 ch I^2C × 1 ch CAN controller × 1 ch			UART (LIN compatible) × 3 ch CSI × 2 ch I^2C × 1 ch CAN controller × 1 ch		
A/D converter		12 bits × 12 ch			12 bits × 12 ch		
D/A converter		–			–		
DMA controller		8 ch			8 ch		
Ports	I/O	33			49		
	Input	–			–		
Debug control unit		Provided (RUN/break/trace)			Provided (RUN/break/trace)		
Other peripheral functions		POC, LVI, clock monitor, comparator × 1, random number generator, data CRC, key return: 8 ch			POC, LVI, clock monitor, comparator × 1, random number generator, data CRC, key return: 8 ch		
Operating frequency		When using main clock: 80 MHz (max.) When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz			When using main clock: 80 MHz (max.) When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz		
Power supply voltage		3.0 V to 5.5 V			3.0 V to 5.5 V		
Package		64-pin LQFP (10 × 10 mm)			80-pin LQFP (12 × 12 mm)		
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C			–40°C to +85°C, –40°C to +110°C, –40°C to +125°C		

Generic Name		V850E2/FK4-G (Under development)	V850E2/FL4-H (Under development)
Part No.		μPD70F3592	μPD70F3564
CPU name		V850E2M	V850E2M
CPU performance (Dhrystone)		T.B.D.	324 MIPS (@ 160 MHz)
Internal ROM		1 MB (flash)	2 MB (flash)
Internal RAM		128 KB	144 KB
Data flash		32 KB	64 KB
External bus interface	Bus type	–	–
	Address bus	–	–
	Data bus	–	–
	Chip select signal	–	–
Memory controller		–	–
Interrupt sources	Internal	T.B.D.	239
	External	17	17
Timer/counter		32-bit timer: 4 ch × 2 units 16-bit timer: 16 ch × 2 units	32-bit timer: 4 ch × 2 units 16-bit timer: 16 ch × 9 units
Watchdog timer		2 ch	2 ch
Serial interface		UART (LIN compatible) × 5 ch CSI × 2 ch I^2C × 1 ch CAN controller × 6 ch FlexRay controller × 2 ch × 1 unit	UART (LIN compatible) × 12 ch CSI × 3 ch CSI (With FIFO) × 3 ch I^2C × 1 ch Ethernet controller × 1 ch CAN controller × 6 ch FlexRay controller × 2 ch × 1 unit
A/D converter		12 bits × 24 ch + 12 ch	12 bits × 24 ch × 2 units
D/A converter		–	–
DMA controller		8 ch	16 ch
Ports	I/O	136	161
	Input	–	–
Debug control unit		Provided (RUN/break/trace)	Provided (RUN/break/trace)
Other peripheral functions		POC, LVI, clock monitor, comparator × 2, random number generator, data CRC	POC, LVI, clock monitor, comparator × 2, random number generator, data CRC, key return: 8 ch
Operating frequency		When using main clock: 80 MHz (max.) When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz	When using main clock: 160 MHz (max.) When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz
Power supply voltage		3.0 V to 5.5 V	3.0 V to 5.5 V
Package		176-pin HLQFP (24 × 24 mm)	208-pin QFP (28 × 28 mm), 256-pin BGA (21 × 21 mm)
Operating ambient temperature		–40°C to +110°	–40°C to +85°C, –40°C to +110°C

ASSP Lineup (Dashboard Control, Body Control) (7/10)

Generic Name		V850ES/FE3		V850ES/FF3		V850ES/FG3			
Part No.		μPD70F3370A	μPD70F3371	μPD70F3372	μPD70F3373	μPD70F3374	μPD70F3375	μPD70F3376A	μPD70F3377A
CPU name		V850ES		V850ES		V850ES			
CPU performance (Dhrystone)		69 MIPS (@ 32 MHz)		69 MIPS (@ 32 MHz)		69 MIPS (@ 32 MHz)		98 MIPS (@ 48 MHz)	
Internal ROM		128 KB (flash)	256 KB (flash)	128 KB (flash)	256 KB (flash)	128 KB (flash)	256 KB (flash)	384 KB (flash)	512 KB (flash)
Internal RAM		8 KB	16 KB	8 KB	16 KB	8 KB	16 KB	24 KB	32 KB
EEPROM emulation		32 KB		32 KB		32 KB			
External bus interface	Bus type	–		–		–			
	Address bus	–		–		–			
	Data bus	–		–		–			
	Chip select signal	–		–		–			
Memory controller		–		–		–			
Interrupt sources	Internal	48 (including one NMI)		48 (including one NMI)		60 (including one NMI)		65 (including one NMI)	
	External	9 (9)* (including one NMI)		9 (9)* (including one NMI)		12 (12)* (including one NMI)		13 (13)* (including one NMI)	
Timer/counter		16-bit timer/event counter (TAB) × 1 ch 16-bit timer/event counter (TAA) × 5 ch 16-bit interval timer (TMM) × 1 ch		16-bit timer/event counter (TAB) × 1 ch 16-bit timer/event counter (TAA) × 5 ch 16-bit interval timer (TMM) × 1 ch		16-bit timer/event counter (TAB) × 2 ch 16-bit timer/event counter (TAA) × 5 ch 16-bit interval timer (TMM) × 1 ch			
Watchdog timer		1 ch		1 ch		1 ch			
Serial interface		CSI × 2 ch UART (LIN compatible) × 2 ch I^2C × 1 ch		CSI × 2 ch UART (LIN compatible) × 2 ch I^2C × 1 ch		CSI × 2 ch UART (LIN compatible) × 3 ch I^2C × 1 ch		CSI × 2 ch UART (LIN compatible) × 5 ch I^2C × 1 ch	
A/D converter		10 bits × 10 ch		10 bits × 12 ch		10 bits × 16 ch			
D/A converter		–		–		–			
DMA controller		4 ch		4 ch		4 ch			
Ports	I/O	51		67		84			
	Input	–		–		–			
Debug control unit		Provided (RUN/break)		Provided (RUN/break)		Provided (RUN/break)			
Other peripheral functions		Watch timer: 1 ch CAN controller: 1 ch Key input interrupt: 8 ch Clock monitor/POC/LVI/PCL output, SSCG		Watch timer: 1 ch CAN controller: 1 ch Key input interrupt: 8 ch Clock monitor/POC/LVI/PCL output, SSCG		Watch timer: 1 ch CAN controller: 2 ch Key input interrupt: 8 ch Clock monitor/POC/LVI/PCL output, SSCG			
Operating frequency		When using main clock: 4 to 32 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz		When using main clock: 4 to 32 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz		When using main clock: 4 to 32 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz		When using main clock: 4 to 48 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz	
Power supply voltage		3.3 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)		3.3 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)		3.3 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)			
Package		64-pin LQFP (10 × 10 mm)		80-pin LQFP (12 × 12 mm)		100-pin LQFP (14 × 14 mm)			
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C			

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850ES/FJ3					V850ES/FK3		
Part No.		μPD70F3378	μPD70F3379	μPD70F3380	μPD70F3381	μPD70F3382	μPD70F3383	μPD70F3384	μPD70F3385
CPU name		V850ES					V850ES		
CPU performance (Dhrystone)		69 MIPS (@ 32 MHz)	98 MIPS (@ 48 MHz)				98 MIPS (@ 48 MHz)		
Internal ROM		256 KB (flash)	384 KB (flash)	512 KB (flash)	768 KB (flash)	1024 KB (flash)	512 KB (flash)	768 KB (flash)	1024 KB (flash)
Internal RAM		16 KB	24 KB	32 KB	40 KB	48 KB	32 KB	48 KB	60 KB
EEPROM emulation		32 KB					32 KB		
External bus interface	Bus type	Multiplexed					Multiplexed		
	Address bus	16 bits					16 bits		
	Data bus	8/16 bits					8/16 bits		
	Chip select signal	4					4		
Memory controller		SRAM, etc.					SRAM, etc.		
Interrupt sources	Internal	71 (including one NMI)	81 (including one NMI)		83 (including one NMI)		101 (including one NMI)		
	External	16 (16)*1 (including one NMI)					17 (17)*1 (including one NMI)		
Timer/counter		16-bit timer/event counter (TAB) × 3 ch 16-bit timer/event counter (TAA) × 5 ch 16-bit interval timer (TMM) × 1 ch					16-bit timer/event counter (TAB) × 3 ch 16-bit timer/event counter (TAA) × 8 ch 16-bit interval timer (TMM) × 1 ch		
Watchdog timer		1 ch					1 ch		
Serial interface		CSI × 3 ch UART (LIN compatible) × 3 ch I^2C × 1 ch	CSI × 3 ch UART (LIN compatible) × 6 ch I^2C × 1 ch		CSI × 4 ch UART (LIN compatible) × 6 ch I^2C × 1 ch		CSI × 4 ch UART (LIN compatible) × 8 ch I^2C × 1 ch		
A/D converter		10 bits × 24 ch					10 bits × 24 ch, 10 bits × 16 ch		
D/A converter		–					–		
DMA controller		4 ch					4 ch		
Ports	I/O	128					152		
	Input	–					–		
Debug control unit		Provided (RUN/break)					Provided (RUN/break)		
Other peripheral functions		Watch timer: 1 ch CAN controller: 3 ch*2 CAN controller: 4 ch*3 Key input interrupt: 8 ch, clock monitor/POC/LVI/PCL output, SSCG					Watch timer: 1 ch CAN controller: 5 ch Key input interrupt: 8 ch Clock monitor/POC/LVI/PCL output, SSCG		
Operating frequency		When using main clock: 4 to 32 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz	When using main clock: 4 to 48 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz				When using main clock: 4 to 48 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz		
Power supply voltage		3.3 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)					3.3 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)		
Package		144-pin LQFP (20 × 20 mm)					176-pin LQFP (24 × 24 mm)		
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C					–40°C to +85°C, –40°C to +110°C, –40°C to +125°C		

*1. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*2. μPD70F3378 only
*3. μPD70F3379/F3380/F3381/F3382 only

ASSP Lineup (Dashboard Control, Body Control) (8/10)

Generic Name		V850ES/FE3-L				
Part No.		μPD70F3610	μPD70F3611	μPD70F3612	μPD70F3613	μPD70F3614
CPU name		V850ES				
CPU performance (Dhrystone)		43 MIPS (@ 20 MHz)				
Internal ROM		64 KB (flash)	96 KB (flash)	128 KB (flash)	192 KB (flash)	256 KB (flash)
Internal RAM		6 KB	6 KB	8 KB	12 KB	16 KB
External bus interface	Bus type	–				
	Address bus	–				
	Data bus	–				
	Chip select signal	–				
Memory controller		–				
Interrupt sources	Internal	39 (including one NMI)				
	External	9 (9)*1 (including one NMI)				
Timer/counter		16-bit timer/event counter (TAA) × 5 ch 16-bit interval timer (TMM) × 1 ch				
Watchdog timer		1 ch				
Serial interface		CSI × 2 ch UART (LIN compatible) × 2 ch I^2C × 1 ch				
A/D converter		10 bits × 10 ch				
D/A converter		–				
DMA controller		–				
Ports	I/O	51				
	Input	–				
Debug control unit		Provided (RUN/break)				
Other peripheral functions		Watch timer: 1 ch CAN controller: 1 ch Key input interrupt: 8 ch Clock monitor/POC/LVI/PCL output				
Operating frequency		When using main clock: 4 to 20 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz				
Power supply voltage		3.3 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)				
Package		64-pin LQFP (10 × 10 mm) 64-pin LQFP (7 × 7 mm)			64-pin LQFP (10 × 10 mm) 64-pin LQFP (7 × 7 mm)*2	
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C				

*1. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*2. μPD70F3614 only

Generic Name		V850ES/FF3-L					V850ES/FG3-L		
Part No.		μPD70F3615	μPD70F3616	μPD70F3617	μPD70F3618	μPD70F3619	μPD70F3620	μPD70F3621	μPD70F3622
CPU name		V850ES					V850ES		
CPU performance (Dhrystone)		43 MIPS (@ 20 MHz)					43 MIPS (@ 20 MHz)		
Internal ROM		64 KB (flash)	96 KB (flash)	128 KB (flash)	192 KB (flash)	256 KB (flash)	128 KB (flash)	192 KB (flash)	256 KB (flash)
Internal RAM		6 KB	6 KB	8 KB	12 KB	16 KB	8 KB	12 KB	16 KB
External bus interface	Bus type	–					–		
	Address bus	–					–		
	Data bus	–					–		
	Chip select signal	–					–		
Memory controller		–					–		
Interrupt sources	Internal	39 (including one NMI)					42 (including one NMI)		
	External	9 (9)* (including one NMI)					12 (12)* (including one NMI)		
Timer/counter		16-bit timer/event counter (TAA) × 5 ch 16-bit interval timer (TMM) × 1 ch					16-bit timer/event counter (TAA) × 5 ch 16-bit interval timer (TMM) × 1 ch		
Watchdog timer		1 ch					1 ch		
Serial interface		CSI × 2 ch UART (LIN compatible) × 2 ch I^2C × 1 ch					CSI × 2 ch UART (LIN compatible) × 3 ch I^2C × 1 ch		
A/D converter		10 bits × 12 ch					10 bits × 16 ch		
D/A converter		–					–		
DMA controller		–					–		
Ports	I/O	67					84		
	Input	–					–		
Debug control unit		Provided (RUN/break)					Provided (RUN/break)		
Other peripheral functions		Watch timer: 1 ch CAN controller: 1 ch Key input interrupt: 8 ch Clock monitor/POC/LVI/PCL output					Watch timer: 1 ch CAN controller: 1 ch Key input interrupt: 8 ch Clock monitor/POC/LVI/PCL output		
Operating frequency		When using main clock: 4 to 20 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz					When using main clock: 4 to 20 MHz When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz		
Power supply voltage		3.3 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)					3.3 V to 5.5 V (A/D converter: 4.0 V to 5.5 V)		
Package		80-pin LQFP (12 × 12 mm)					100-pin LQFP (14 × 14 mm)		
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C					–40°C to +85°C, –40°C to +110°C, –40°C to +125°C		

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

ASSP Lineup (Dashboard Control, Body Control) (9/10)

Generic Name		V850ES/FE2			V850ES/FF2			
Part No.		μPD703230B	μPD703231B	μPD70F3231B	μPD703232B	μPD70F3232B	μPD703233B	μPD70F3233B
CPU name		V850ES			V850ES			
CPU performance (Dhrystone)		43 MIPS (@ 20 MHz)			43 MIPS (@ 20 MHz)			
Internal ROM		64 KB (mask)	128 KB (mask)	128 KB (flash)	128 KB (mask)	128 KB (flash)	256 KB (mask)	256 KB (flash)
Internal RAM		4 KB	6 KB		6 KB	12 KB		
External bus interface	Bus type	–			–			
	Address bus	–			–			
	Data bus	–			–			
	Chip select signal	–			–			
Memory controller		–			–			
Interrupt sources	Internal	36 (including one NMI)			36 (including one NMI)			
	External	9 (9)* (including one NMI)			9 (9)* (including one NMI)			
Timer/counter		16-bit timer/event counter (TMP) × 4 ch 16-bit timer/event counter (TMQ) × 1 ch 16-bit interval timer (TMM) × 1 ch			16-bit timer/event counter (TMP) × 4 ch 16-bit timer/event counter (TMQ) × 1 ch 16-bit interval timer (TMM) × 1 ch			
Watchdog timer		1 ch			1 ch			
Serial interface		CSI × 2 ch UART (LIN compatible) × 2 ch			CSI × 2 ch UART (LIN compatible) × 2 ch			
A/D converter		10 bits × 10 ch			10 bits × 12 ch			
D/A converter		–			–			
DMA controller		–			–			
Ports	I/O	51			67			
	Input	–			–			
Debug control unit		–		Provided (RUN/break)	–	Provided (RUN/break)	–	Provided (RUN/break)
Other peripheral functions		Watch timer: 1 ch, POC/LVI, RAM retention flag, CAN controller: 1 ch			Watch timer: 1 ch, POC/LVI, RAM retention flag, CAN controller: 1 ch			
Operating frequency		When using main clock: 4 to 20 MHz			When using main clock: 4 to 20 MHz			
Power supply voltage		3.5 V to 5.5 V			3.5 V to 5.5 V			
Package		64-pin LQFP (10 × 10 mm)			80-pin TQFP (12 × 12 mm)			
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C			–40°C to +85°C, –40°C to +110°C, –40°C to +125°C			

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850ES/FG2					V850ES/FJ2		
Part No.		μPD703234B	μPD70F3234B	μPD703235B	μPD70F3235B	μPD70F3236B	μPD70F3237B	μPD70F3238B	μPD70F3239B
CPU name		V850ES					V850ES		
CPU performance (Dhrystone)		43 MIPS (@ 20 MHz)					43 MIPS (@ 20 MHz)		
Internal ROM		128 KB (mask)	128 KB (flash)	256 KB (mask)	256 KB (flash)	384 KB (flash)	256 KB (flash)	376 KB (flash)	512 KB (flash)
Internal RAM		6 KB		12 KB		16 KB	12 KB	20 KB	
External bus interface	Bus type	–					Multiplexed		
	Address bus	–					16 bits		
	Data bus	–					8/16 bits		
	Chip select signal	–					4		
Memory controller		–					SRAM, etc.		
Interrupt sources	Internal	51 (including one NMI)					58 (including one NMI)	68 (including one NMI)	
	External	12 (12)* (including one NMI)					16 (16)* (including one NMI)		
Timer/counter		16-bit timer/event counter (TMP) × 4 ch 16-bit timer/event counter (TMQ) × 2 ch 16-bit interval timer (TMM) × 1 ch					16-bit timer/event counter (TMP) × 4 ch 16-bit timer/event counter (TMQ) × 3 ch 16-bit interval timer (TMM) × 1 ch		
Watchdog timer		1 ch					1 ch		
Serial interface		CSI × 2 ch UART (LIN compatible) × 3 ch					CSI × 3 ch UART (LIN compatible) × 3 ch	CSI × 3 ch UART (LIN compatible) × 4 ch	
A/D converter		10 bits × 16 ch					10 bits × 24 ch		
D/A converter		–					–		
DMA controller		4 ch					4 ch		
Ports	I/O	84					128		
	Input	–					–		
Debug control unit		–	Provided (RUN/break)	–	Provided (RUN/break)		Provided (RUN/break)		
Other peripheral functions		Watch timer: 1 ch, POC/LVI, RAM retention flag, CAN controller: 2 ch					Watch timer: 1 ch, POC/LVI, RAM retention flag		
							CAN controller: 2 ch	CAN controller: 4 ch	
Operating frequency		When using main clock: 4 to 20 MHz					When using main clock: 4 to 20 MHz		
Power supply voltage		3.5 V to 5.5 V					3.5 V to 5.5 V		
Package		100-pin LQFP (14 × 14 mm)					144-pin LQFP (20 × 20 mm)		
Operating ambient temperature		–40°C to +85°C, –40°C to +110°C, –40°C to +125°C					–40°C to +85°C, –40°C to +110°C, –40°C to +125°C		

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

ASSP Lineup (Dashboard Control, Body Control) (10/10)

Generic Name		V850E/IA1	
Part No.		μPD703116	μPD70F3116
CPU name		V850E1	
CPU performance (Dhrystone)		103 MIPS (@ 50 MHz)	
Internal ROM		256 KB (mask)	256 KB (flash)
Internal RAM		10 KB	
External bus interface	Bus type	Multiplexed	
	Address bus	24 bits	
	Data bus	8/16 bits	
	Chip select signal	8	
Memory controller		SRAM, etc.	
Interrupt sources	Internal	45	
	External	20 (14)* (including one NMI)	
Timer/counter		16-bit 3-phase inverter control PWM timer × 2 ch 16-bit encoder counter/timer × 2 ch 16-bit timer/counter × 2 ch 16-bit timer/event counter × 1 ch 16-bit interval timer × 1 ch	
Watchdog timer		–	
Serial interface		CSI × 2 ch UART × 3 ch	
A/D converter		10 bits × 8 ch, 2 units	
D/A converter		–	
DMA controller		4 ch	
Ports	I/O	75	
	Input	8	
Debug control unit		–	
Other peripheral functions		CAN controller × 1 ch	
Operating frequency		4 to 50 MHz	
Power supply voltage		3.0 V to 3.6 V (internal) 4.5 V to 5.5 V (external)	
Package		144-pin LQFP (20 × 20 mm)	
Operating ambient temperature		–40°C to +85°C (110°C version also available)	

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

ASSP Lineup (CAN) (1/7)

Generic Name		V850E2/MN4 (Under development)		
Part No.		μPD70F3512	μPD70F3514	μPD70F3515
CPU name		V850E2M	V850E2M × 2	
CPU performance (Dhrystone)		512 MIPS (@ 200 MHz)		
Internal ROM		1 MB (flash)		2 MB (flash)
Internal RAM		64 KB	64 KB × 2	
External bus interface	Bus type	Separate (2 channels)		
	Address bus	26 bits, 26 bits		
	Data bus	8/16/32 bits, 16/32 bits		
	Chip select signal	4, 5		
Memory controller		SDRAM, SRAM, etc.		
Interrupt sources	Internal	190	196	
	External	29 (including one NMI)		
Timer/counter		32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 4 units 16-bit encoder timer: 2 ch		
Watchdog timer		1 ch	2 ch	
Serial interface		UART/CSI × 4 ch UART/CSI/I²C × 4 ch*1 UART/CSI/I²C/CAN × 2 ch*2		
A/D converter		12 bits × 12 ch (5 V analog), 10 bits × 12 ch (3.3 V analog)		
D/A converter		–		
DMA controller		16 ch		
Ports	I/O	181		
	Input	7		
Debug control unit		Provided (RUN/break)		
USB controller		USB 2.0 function (full-speed) × 1 ch USB 2.0 host (full-speed) × 1 ch		
Ethernet controller		1 ch		
Other peripheral functions		Hardware bus common memory: 64 KB, hardware bus side cache: 16 KB, dedicated DMA for secondary memory controller, inverter timer support, boundary scan		
Operating frequency		144 to 200 MHz		
Power supply voltage		1.1 V to 1.3 V (internal)/3.0 V to 3.6 V (external)/analog: 3.0 V to 3.6 V or 4.5 V to 5.5 V*3		
Package		304-pin FBGA (19 × 19 mm)		
Operating ambient temperature		–40°C to +100°C*4		

*1. Of which, 3 UART/SCII channels have FIFO function.
*2. Of which, 1 UART/SCII channel have FIFO function.
*3. 10-bit precision when using 3.3 V analog power supply, 12-bit precision when using 5 V analog power supply
*4. Package surface temperature

Generic Name		V850E2/ML4 (Under development)	
Part No.		μPD70F3510	μPD70F3514
CPU name		V850E2M	
CPU performance (Dhrystone)		512 MIPS (@ 200 MHz)	
Internal ROM		768 KB (flash)	1 MB (flash)
Internal RAM		64 KB + expanded RAM: 64 KB	
External bus interface	Bus type	Separate	
	Address bus	26 bits	
	Data bus	8/16/32 bits	
	Chip select signal	4	
Memory controller		SDRAM, SRAM, etc.	
Interrupt sources	Internal	150	
	External	29 (including one NMI)	
Timer/counter		16-bit timer array: 16 ch × 2 unit 32-bit timer array: 4 ch × 1 units 16-bit encoder timer: 2 ch	
Watchdog timer		1 ch	
Serial interface		UART × 4 ch (of which, 2 have FIFO function) CSI × 4 ch (of which, 2 have FIFO function) I²C × 2 ch	
A/D converter		10 bits or 12 bits × 12 ch (5 V input for 12-bit)	
D/A converter		–	
DMA controller		8 ch (4 ch for internal transfers only)	
Ports	I/O	119	
	Input	1	
Debug control unit		Provided (RUN/break/trace)	
USB controller		USB 2.0 function (full-speed) × 1 ch USB 2.0 host (full-speed) × 1 ch	
Ethernet controller		1 ch	
Other peripheral functions		CAN, FPU	
Operating frequency		200 MHz	
Power supply voltage		1.2 V and 3.3 V (+5 V (12-bits A/D)	
Package		216-pin QFP (24 × 24 mm)	
Operating ambient temperature		–40°C to +100°C*	

* Package surface temperature

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ASSP Lineup (CAN) (2/7)

Generic Name		V850E2/SG4-H (Under planning)		V850E2/SJ4-H (Under planning)		V850E2/SK4-H (Under development)	
Part No.		μPD70F4013	μPD70F4014	μPD70F4015	μPD70F4016	μPD70F4017	μPD70F4018
CPU name		V850E2M		V850E2M		V850E2M	
CPU performance (Dhrystone)		400 MIPS (@ 160 MHz)		400 MIPS (@ 160 MHz)		400 MIPS (@ 160 MHz)	
Internal ROM		1 MB (flash)	1.5 MB (flash)	1 MB (flash)	1.5 MB (flash)	1.5 MB (flash)	2 MB (flash)
Internal RAM		96 KB	128 KB	96 KB	128 KB	128 KB	192 KB
Data flash		32 KB		32 KB		32 KB	
External bus interface	Bus type	Multiplexed SRAM I/F		SDRAM I/F, multiplexed/separate SRAM I/F		SDRAM I/F, multiplexed/separate SRAM I/F	
	Address bus	20 bits		24 bits		24 bits	
	Data bus	8/16 bits		8/16 bits		8/16/32 bits	
	Chip select signal	–		3		4	
Memory controller		SRAM, etc.		SDRAM, SRAM, etc.		SDRAM, SRAM, etc.	
Interrupt sources	Internal	10		16		16	
	External	144		161		208	
Timer/counter		32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 1 unit		32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 1 unit		32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 2 units	
Watchdog timer		2 ch		2 ch		2 ch	
Serial interface		UART/CSI × 4 ch CSI × 2 ch CSI (With FIFO) × 2 ch I^2C × 4 ch CAN controller × 1 ch IEBus × 1 ch MediaLB × 1 ch		UART/CSI × 5 ch CSI × 2 ch CSI (With FIFO) × 3 ch I^2C × 4 ch CAN controller × 2 ch IEBus × 1 ch MediaLB × 1 ch		UART/CSI × 5 ch CSI × 2 ch CSI (With FIFO) × 3 ch I^2C × 4 ch CAN controller × 2 ch IEBus × 1 ch MediaLB × 1 ch	
A/D converter		10 bits × 8 ch × 1 unit		10 bits × 16 ch × 1 unit		10 bits × 16 ch × 1 unit	
D/A converter		–		–		–	
DMA controller		16 ch		16 ch		16 ch	
Ports	I/O	58		100		127	
	Input	–		–		–	
Debug control unit		Provided (RUN/break)		Provided (RUN/break)		Provided (RUN/break)	
Ethernet controller		–		–		1 ch	
Other peripheral functions		Power-on clear (option), LVI, clock monitor, data CRC, Hardware bus common memory: 32 KB, SSCG		Power-on clear (option), LVI, clock monitor, data CRC, Hardware bus common memory: 32 KB, SSCG		Power-on clear (option), LVI, clock monitor, data CRC, Hardware bus common memory: 32 KB, SSCG	
Operating frequency		When using main clock: 160 MHz (max.) When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz		When using main clock: 160 MHz (max.) When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz		When using main clock: 160 MHz (max.) When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz	
Power supply voltage		1.1 V to 1.3 V (internal)/3.0 V to 3.6 V (external)		1.1 V to 1.3 V (internal)/3.0 V to 3.6 V (external)		1.1 V to 1.3 V (internal)/3.0 V to 3.6 V (external)	
Package		100-pin LQFP (14 × 14 mm)		144-pin LQFP (20 × 20 mm)		176-pin LQFP (24 × 24 mm)	
Operating ambient temperature		–40°C to +85°C, –40°C to +105°C		–40°C to +85°C, –40°C to +105°C		–40°C to +85°C, –40°C to +105°C	

Numbers of channels indicate the total number implemented on the product. The actual number of usable channels differs depending on multi-use pin settings.

Generic Name		V850ES/JE3-E (Under development)	V850ES/JF3-E (Under development)	V850ES/JG3-E (Under development)
Part No.		μPD70F3829	μPD70F3833	μPD70F3837
CPU name		V850ES	V850ES	V850ES
CPU performance (Dhrystone)		103 MIPS (@ 50 MHz)	103 MIPS (@ 50 MHz)	103 MIPS (@ 50 MHz)
Internal ROM		256 KB (flash)	256 KB (flash)	256 KB (flash)
Internal RAM		64 KB (Including 16 KB of data-only RAM)	64 KB (Including 16 KB of data-only RAM)	64 KB (Including 16 KB of data-only RAM)
External bus interface	Bus type	–	–	–
	Address bus	–	–	–
	Data bus	–	–	–
	Chip select signal	–	–	–
Memory controller		–	–	–
Interrupt sources	Internal	66 (Including one NMI)	67 (Including one NMI)	70 (Including one NMI)
	External	11 (11)* (Including one NMI)	20 (20)* (Including one NMI)	22 (22)* (Including one NMI)
Timer/counter		16-bit timer/event counter (TAA) × 4 ch 16-bit timer/event counter (TAB) × 1 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch	16-bit timer/event counter (TAA) × 4 ch 16-bit timer/event counter (TAB) × 1 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch	16-bit timer/event counter (TAA) × 4 ch 16-bit timer/event counter (TAB) × 1 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch
Watchdog timer		1 ch	1 ch	1 ch
Serial interface		UART (LIN compatible)/CSI × 1 ch UART (LIN compatible)/CSI/I^2C × 1 ch CSI × 1 ch UART (LIN compatible)/I^2C/CAN × 1 ch	UART (LIN compatible)/CSI × 1 ch UART (LIN compatible)/CSI/I^2C × 2 ch CSI × 2 ch UART (LIN compatible)/I^2C/CAN × 1 ch	UART (LIN compatible)/CSI × 1 ch UART (LIN compatible)/CSI/I^2C × 2 ch CSI × 2 ch UART (LIN compatible)/I^2C/CAN × 1 ch
A/D converter		10 bits × 8 ch	10 bits × 8 ch	10 bits × 10 ch
D/A converter		–	–	–
DMA controller		4 ch	4 ch	4 ch
Ports	I/O	29	41	64
	Input	–	–	–
Debug control unit		Provided (RUN/break)	Provided (RUN/break)	Provided (RUN/break)
USB controller		USB 2.0 function (full-speed) × 1 ch	USB 2.0 function (full-speed) × 1 ch	USB 2.0 function (full-speed) × 1 ch
Ethernet controller		1 ch	1 ch	1 ch
Other peripheral functions		Real-time counter (RTC), LVI/clock monitor, CRC, RAM retention flag	Motor control, real-time counter (RTC), LVI/clock monitor, CRC, RAM retention flag	Motor control, real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag
Operating frequency		When using main clock: 24 to 50 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz	When using main clock: 24 to 50 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz	When using main clock: 24 to 50 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz
Power supply voltage		2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)	2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)	2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)
Package		64-pin LQFP (10 × 10 mm), 64-pin WQFN (9 × 9 mm)	80-pin LQFP (12 × 12 mm)	100-pin LQFP (14 × 14 mm), 121-pin FBGA (8 × 8 mm)
Operating ambient temperature		–40°C to +85°C	–40°C to +85°C	–40°C to +85°C

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

ASSP Lineup (CAN) (3/7)

Generic Name		V850ES/JH3-E	V850ES/JJ3-E
Part No.		μPD70F3783	μPD70F3786
CPU name		V850ES	V850ES
CPU performance (Dhrystone)		103 MIPS (@ 50 MHz)	103 MIPS (@ 50 MHz)
Internal ROM		512 KB (flash)	512 KB (flash)
Internal RAM		124 KB (including 64 KB of data-only RAM)	124 KB (including 64 KB of data-only RAM)
External bus interface	Bus type	Multiplexed/separate	Multiplexed/separate
	Address bus	22 bits	24 bits
	Data bus	8/16 bits	8/16 bits
	Chip select signal	3	2
Memory controller		SRAM, etc.	SRAM, etc.
Interrupt sources	Internal	82 (Including one NMI)	88 (Including one NMI)
	External	22 (22)*1 (Including one NMI)	27 (27)*1 (Including one NMI)
Timer/counter		16-bit timer/event counter (TAA) × 6 ch 16-bit timer/event counter (TAB) × 2 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch	16-bit timer/event counter (TAA) × 6 ch 16-bit timer/event counter (TAB) × 2 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch
Watchdog timer		1 ch	1 ch
Serial interface		UART (LIN compatible)/CSI × 1 ch UART (LIN compatible)/CSI (with FIFO) × 1 ch UART (with FIFO)/CSI × 2 ch*2 UART (LIN compatible)/CSI/I^2C × 2 ch UART (LIN compatible)/CSI (with FIFO)*3/I^2C × 1 ch CSI (with FIFO)*3 × 1 ch UART (LIN compatible)/I^2C/CAN × 1 ch	UART (LIN compatible)/CSI × 3 ch UART (LIN compatible)/CSI (with FIFO) × 1 ch UART (with FIFO)/CSI × 2 ch*2 UART (LIN compatible)/CSI/I^2C × 2 ch UART (LIN compatible)/CSI (with FIFO)*3/I^2C × 1 ch CSI (with FIFO)*3 × 1 ch I^2C × 1 ch UART (LIN compatible)/I^2C/CAN × 1 ch
A/D converter		10 bits × 10 ch	10 bits × 12 ch
D/A converter		–	–
DMA controller		4 ch	4 ch
Ports	I/O	84	100
	Input	–	–
Debug control unit		Provided (RUN/break)	Provided (RUN/break)
USB controller		USB 2.0 function (full-speed) × 1 ch	USB 2.0 function (full-speed) × 1 ch
Ethernet controller		1 ch	1 ch
Other peripheral functions		Motor control, real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag	Motor control, real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag
Operating frequency		When using main clock: 24 to 50 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz	When using main clock: 24 to 50 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz
Power supply voltage		2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)	2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)
Package		128-pin LQFP (14 × 20 mm)	144-pin LQFP (20 × 20 mm)
Operating ambient temperature		–40°C to +85°C	–40°C to +85°C

*1. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*2. One channel is assigned to two different pins.
*3. The same channel is assigned to two different pins.

Generic Name		V850ES/JC3-H	V850ES/JE3-H
Part No.		μPD70F3819	μPD70F3825
CPU name		V850ES	V850ES
CPU performance (Dhrystone)		98 MIPS (@ 48 MHz)	98 MIPS (@ 48 MHz)
Internal ROM		256 KB (flash)	256 KB (flash)
Internal RAM		24 KB	24 KB
External bus interface	Bus type	–	–
	Address bus	–	–
	Data bus	–	–
	Chip select signal	–	–
Memory controller		–	–
Interrupt sources	Internal	58 (Including one NMI)	58 (Including one NMI)
	External	10 (10)* (Including one NMI)	11 (11)* (Including one NMI)
Timer/counter		16-bit timer/event counter (TAA) × 4 ch 16-bit timer/event counter (TAB) × 1 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch	16-bit timer/event counter (TAA) × 4 ch 16-bit timer/event counter (TAB) × 1 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch
Watchdog timer		1 ch	1 ch
Serial interface		UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/CSI/I^2C × 1 ch CSI × 1 ch UART (LIN compatible)/I^2C/CAN × 1 ch	UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/CSI/I^2C × 1 ch CSI × 1 ch UART (LIN compatible)/I^2C/CAN × 1 ch
A/D converter		10 bits × 6 ch	10 bits × 10 ch
D/A converter		8 bits × 1 ch	8 bits × 1 ch
DMA controller		4 ch	4 ch
Ports	I/O	32	45
	Input	–	–
Debug control unit		Provided (RUN/break)	Provided (RUN/break)
USB controller		USB 2.0 function (full-speed) × 1 ch	USB 2.0 function (full-speed) × 1 ch
Other peripheral functions		Real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag	Motor control, real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag
Operating frequency		When using main clock: 24 to 48 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz	When using main clock: 24 to 48 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz
Power supply voltage		2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)	2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)
Package		48-pin LQFP (7 × 7 mm), 48-pin WQFN (7 × 7 mm)	64-pin LQFP (10 × 10 mm), 64-pin WQFN (9 × 9 mm)
Operating ambient temperature		–40°C to +85°C	–40°C to +85°C

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

ASSP Lineup (CAN) (4/7)

Generic Name		V850ES/JG3-H	V850ES/JH3-H
Part No.		μPD70F3770	μPD70F3771
CPU name		V850ES	V850ES
CPU performance (Dhrystone)		98 MIPS (@ 48 MHz)	98 MIPS (@ 48 MHz)
Internal ROM		256 KB (flash)	256 KB (flash)
Internal RAM		40 KB*1	40 KB*1
External bus interface	Bus type	Multiplexed	Multiplexed/separate
	Address bus	16 bits	24 bits
	Data bus	8/16 bits	8/16 bits
	Chip select signal	3	3
Memory controller		SRAM, etc.	SRAM, etc.
Interrupt sources	Internal	73 (including one NMI)	73 (including one NMI)
	External	17 (17)*2 (including one NMI)	20 (20)*2 (including one NMI)
Timer/counter		16-bit timer/event counter (TAA) × 6 ch 16-bit timer/event counter (TAB) × 2 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch	16-bit timer/event counter (TAA) × 6 ch 16-bit timer/event counter (TAB) × 2 ch 16-bit timer/event counter (TMT) × 1 ch 16-bit interval timer (TMM) × 4 ch
Watchdog timer		1 ch	1 ch
Serial interface		CSI × 2 ch UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/I²C × 1 ch UART (LIN compatible)/CSI/I²C × 1 ch UART (LIN compatible)/I²C/CAN × 1 ch	CSI × 2 ch UART (LIN compatible)/CSI × 2 ch UART (LIN compatible)/I²C × 1 ch UART (LIN compatible)/CSI/I²C × 1 ch UART (LIN compatible)/I²C/CAN × 1 ch
A/D converter		10 bits × 12 ch	10 bits × 12 ch
D/A converter		8 bits × 2 ch	8 bits × 2 ch
DMA controller		4 ch	4 ch
Ports	I/O	77	96
	Input	–	–
Debug control unit		Provided (RUN/break)	Provided (RUN/break)
USB controller		USB 2.0 function (full-speed) × 1 ch	USB 2.0 function (full-speed) × 1 ch
Other peripheral functions		Motor control, real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag	Motor control, real-time counter (RTC), real-time output, LVI/clock monitor, CRC, RAM retention flag
Operating frequency		When using main clock: 24 to 48 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz	When using main clock: 24 to 48 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz
Power supply voltage		2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)	2.85 V to 3.6 V (A/D converter, USB controller: 3.0 V to 3.6 V)
Package		100-pin LQFP (14 × 14 mm)	128-pin LQFP (14 × 20 mm)
Operating ambient temperature		−40°C to +85°C	−40°C to +85°C

*1. Includes 8 KB of data-only RAM.
*2. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

Generic Name		V850ES/SG3					
Part No.		μPD70F3335	μPD70F3336	μPD70F3350	μPD70F3351	μPD70F3352	μPD70F3353
CPU name		V850ES					
CPU performance (Dhrystone)		69 MIPS (@ 32 MHz)					
Internal ROM		256 KB (flash)	384 KB (flash)	512 KB (flash)	640 KB (flash)	768 KB (flash)	1024 KB (flash)
Internal RAM		24 KB	32 KB	40 KB	48 KB	60 KB	
External bus interface	Bus type	Multiplexed/separate					
	Address bus	22 bits					
	Data bus	8/16 bits					
	Chip select signal	–					
Memory controller		SRAM, etc.					
Interrupt sources	Internal	52 (including one NMI)					
	External	9 (9)* (including one NMI)					
Timer/counter		16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 6 ch 16-bit timer/event counter (TMQ) × 1 ch					
Watchdog timer		1 ch					
Serial interface		CSI × 3 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch					
A/D converter		10 bits × 12 ch					
D/A converter		8 bits × 2 ch					
DMA controller		4 ch					
Ports	I/O	84					
	Input	–					
Debug control unit		Provided (RUN/break)					
Other peripheral functions		Watch timer: 1 ch IEBus controller/CAN controller: 1 ch ROM correction: 4 points Real-time output LVI/clock monitor/CRC					
Operating frequency		When using main clock: 2.5 to 32 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz					
Power supply voltage		2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V)					
Package		100-pin LQFP (14 × 14 mm)					
Operating ambient temperature		−40°C to +85°C					

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

ASSP Lineup (CAN) (5/7)

Generic Name		V850ES/SJ3				
Part No.	On-chip CAN (1 ch max.)	μPD70F3354	μPD70F3355	μPD70F3356	μPD70F3357	μPD70F3358
	On-chip CAN (2 ch max.)	μPD70F3364	μPD70F3365	μPD70F3366	μPD70F3367	μPD70F3368
CPU name		V850ES				
CPU performance (Dhrystone)		69 MIPS (@ 32 MHz)				
Internal ROM		384 KB (flash)	512 KB (flash)	640 KB (flash)	768 KB (flash)	1024 KB (flash)
Internal RAM		32 KB	40 KB	48 KB	60 KB	
External bus interface	Bus type	Multiplexed/separate				
	Address bus	24 bits				
	Data bus	8/16 bits				
	Chip select signal	4				
Memory controller		SRAM, etc.				
Interrupt sources	Internal	65*1/69*2 (including one NMI for each)				
	External	10 (10)*3 (including one NMI)				
Timer/counter		16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 9 ch 16-bit timer/event counter (TMQ) × 1 ch				
Watchdog timer		1 ch				
Serial interface		CSI × 4 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch UART (LIN compatible) × 1 ch				
A/D converter		10 bits × 16 ch				
D/A converter		8 bits × 2 ch				
DMA controller		4 ch				
Ports	I/O	128				
	Input	–				
Debug control unit		Provided (RUN/break)				
Other peripheral functions		Watch timer: 1 ch IEBus controller/CAN controller*4: 1 ch CAN controller: 2 ch*5 ROM correction: 4 points Real-time output LVI/clock monitor/CRC				
Operating frequency		When using main clock: 2.5 to 32 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz				
Power supply voltage		2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V)				
Package		144-pin LQFP (20 × 20 mm)				
Operating ambient temperature		−40°C to +85°C				

*1. Product with 1 ch CAN only
*2. Products with 2 ch CAN only
*3. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*4. μPD70F3354/F3355/F3356/F3357/F3358 only
*5. μPD70F3364/F3365/F3366/F3367/F3368 only

Generic Name		V850E/SJ3-H			
Part No.	On-chip CAN (1 ch max.)	μPD70F3475A	μPD70F3478A	μPD70F3935A	μPD70F3938A
	On-chip CAN (2 ch max.)	μPD70F3476A	μPD70F3479A	μPD70F3936A	μPD70F3939A
CPU name		V850E1			
CPU performance (Dhrystone)		95 MIPS (@ 48 MHz)			
Internal ROM		1280 KB (flash)	1536 KB (flash)	768 KB (flash)	1024 KB (flash)
Internal RAM		92 KB (internal RAM: 60 KB, expanded internal RAM: 32 KB)		76 KB (internal RAM: 60 KB, expanded internal RAM: 16 KB)	
External bus interface	Bus type	Multiplexed/separate			
	Address bus	24 bits			
	Data bus	8/16 bits			
	Chip select signal	3			
Memory controller		SRAM, etc.			
Interrupt sources	Internal	99*1/103*2 (including one NMI for each)			
	External	11 (11)*3 (including one NMI)			
Timer/counter		16-bit interval timer (TMM) × 3 ch 16-bit timer/event counter (TMP) × 9 ch (encoder count function: 2 ch) 16-bit timer/event counter (TMQ) × 1 ch			
Watchdog timer		1 ch			
Serial interface		UART/CSI × 1 ch, UART/I²C × 2 ch, UART/CSI/I²C × 1 ch, UART/CSI (FIFO compatible) × 1 ch, CSI/I²C × 1 ch, UART × 1 ch, UART (FIFO compatible) × 2 ch, CSI × 3 ch, CSI (FIFO compatible) × 1 ch, I²C × 2 ch or UART/CSI × 1 ch, UART/I²C × 1 ch, UART/CSI/I²C × 2 ch, UART/CSI (FIFO compatible) × 1 ch, CSI/I²C × 1 ch, UART × 1 ch, UART (FIFO compatible) × 2 ch, CSI × 2 ch, CSI (FIFO compatible) × 1 ch, I²C × 2 ch			
A/D converter		10 bits × 16 ch			
D/A converter		8 bits × 2 ch			
DMA controller		4 ch			
Ports	I/O	128			
	Input	–			
Debug control unit		Provided (RUN/break)			
Other peripheral functions		Watch timer: 1 ch Real-time counter (Watch timer): 1 ch IEBus controller/CAN controller*4: 1 ch CAN controller: 2 ch*5 ROM correction: 8 points Real-time output LVI/clock monitor/CRC, SSCG			
Operating frequency		When using main clock: 48 MHz (max.) When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz			
Power supply voltage		2.85 V to 3.6 V (A/D converter, D/A converter: 3.0 V to 3.6 V)			
Package		144-pin LQFP (20 × 20 mm)			
Operating ambient temperature		−40°C to +85°C			

*1. Products with 1 ch CAN only
*2. Products with 2 ch CAN only
*3. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*4. μPD70F3475, 70F3478, 70F3935, 70F3938
*5. μPD70F3476, 70F3479, 70F3936, 70F3939

ASSP Lineup (CAN) (6/7)

Generic Name		V850E/SJ3-H	V850E/SK3-H		
Part No.	On-chip CAN (1 ch max.)	μPD70F3932A	μPD70F3481A	μPD70F3487A	μPD70F3926A
	On-chip CAN (2 ch max.)	μPD70F3933A	μPD70F3482A	μPD70F3488A	μPD70F3927A
CPU name		V850E1	V850E1		
CPU performance (Dhrystone)		95 MIPS (@ 48 MHz)	95 MIPS (@ 48 MHz)		
Internal ROM		512 KB (flash)	1536 KB (flash)	1280 KB (flash)	1024 KB (flash)
Internal RAM		60 KB (internal RAM: 60 KB, expanded internal RAM: none)	92 KB (internal RAM: 60 KB, expanded internal RAM: 32 KB)	76 KB (internal RAM: 60 KB, expanded internal RAM: 16 KB)	
External bus interface	Bus type	Multiplexed/separate	Multiplexed/separate		
	Address bus	24 bits	24 bits		
	Data bus	8/16 bits	8/16 bits		
	Chip select signal	3	3		
Memory controller		SRAM, etc.	SRAM, etc.		
Interrupt sources	Internal	93*1/97*2 (including one NMI for each)	99*1/103*2 (including one NMI for each)		
	External	11 (11)*3 (including one NMI)	11 (11)*3 (including one NMI)		
Timer/counter		16-bit interval timer (TMM) × 3 ch 16-bit timer/event counter (TMP) × 9 ch (encoder count function: 2 ch) 16-bit timer/event counter (TMQ) × 1 ch	16-bit interval timer (TMM) × 3 ch 16-bit timer/event counter (TMP) × 9 ch (encoder count function: 2 ch) 16-bit timer/event counter (TMQ) × 1 ch		
Watchdog timer		1 ch	1 ch		
Serial interface		UART/CSI × 1ch, UART/I²C × 2ch, CSI/I²C × 1ch, UART × 1ch, UART (FIFO compatible) × 2ch, CSI × 3ch, I²C × 1ch or UART/CSI × 1ch, UART/I²C × 1ch, UART/CSI/I²C × 1ch, CSI/I²C × 1ch, UART × 1ch, UART (with FIFO) × 2ch, CSI × 2ch, I²C × 1ch	UART/CSI × 1 ch, UART/I²C × 2 ch, UART/CSI/I²C × 1 ch, UART/CSI (FIFO compatible) × 1 ch, CSI/I²C × 1 ch, UART × 1 ch, UART (FIFO compatible) × 2 ch, CSI × 3 ch, CSI (FIFO compatible) × 1 ch, I²C × 2 ch or UART/CSI × 1 ch, CSI/I²C × 2 ch, UART × 5 ch, UART (FIFO compatible) × 2 ch, CSI × 3 ch, CSI (FIFO compatible) × 2 ch, I²C × 4 ch		
A/D converter		10 bits × 16 ch	10 bits × 16 ch		
D/A converter		8 bits × 2 ch	8 bits × 2 ch		
DMA controller		4 ch	4 ch		
Ports	I/O	128	156		
	Input	–	–		
Debug control unit		Provided (RUN/break)	Provided (RUN/break)		
Other peripheral functions		Watch timer: 1 ch Real-time counter (Watch timer): 1 ch IEBus controller/CAN controller*4: 1 ch CAN controller: 2 ch*5 ROM correction: 8 points Real-time output LVI/clock monitor/CRC, SSCG	Watch timer: 1 ch Real-time counter (Watch timer): 1 ch IEBus controller/CAN controller*6: 1 ch CAN controller: 2 ch*7 ROM correction: 8 points Real-time output LVI/clock monitor/CRC, SSCG		
Operating frequency		When using main clock: 48 MHz (max.) When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz	When using main clock: 48 MHz (max.) When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz		
Power supply voltage		2.85 V to 3.6 V (A/D converter, D/A converter: 3.0 V to 3.6 V)	2.85 V to 3.6 V (A/D converter, D/A converter: 3.0 V to 3.6 V)		
Package		144-pin LQFP (20 × 20 mm)	176-pin LQFP (24 × 24 mm)		
Operating ambient temperature		–40°C to +85°C	–40°C to +85°C		

*1. Products with 1 ch CAN only
*2. Products with 2 ch CAN only
*3. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*4. μPD70F3932
*5. μPD70F3933
*6. μPD70F3481, 3487, 3926
*7. μPD70F3482, 3488, 3927

Generic Name		V850ES/SG2-H			V850ES/SG2					
Part No.		μPD703282HY	μPD703283HY	μPD70F3283HY	μPD703280Y	μPD703281Y	μPD70F3281Y	μPD703282Y	μPD703283Y	μPD70F3283Y
CPU name		V850ES			V850ES					
CPU performance (Dhrystone)		66 MIPS (@ 32 MHz)			43 MIPS (@ 20 MHz)					
Internal ROM		512 KB (mask)	640 KB (mask)	640 KB (flash)	256 KB (mask)	384 KB (mask)	384 KB (flash)	512 KB (mask)	640 KB (mask)	640 KB (flash)
Internal RAM		40 KB	48 KB		24 KB	32 KB		40 KB	48 KB	
External bus interface	Bus type	Multiplexed/separate			Multiplexed/separate					
	Address bus	22 bits			22 bits					
	Data bus	8/16 bits			8/16 bits					
	Chip select signal	–			–					
Memory controller		SRAM, etc.			SRAM, etc.					
Interrupt sources	Internal	51 (including one NMI)			52 (including one NMI)					
	External	9 (9)* (including one NMI)			9 (9)* (including one NMI)					
Timer/counter		16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 6 ch 16-bit timer/event counter (TMQ) × 1 ch			16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 6 ch 16-bit timer/event counter (TMQ) × 1 ch					
Watchdog timer		1 ch			1 ch					
Serial interface		CSI × 3 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch			CSI × 3 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch					
A/D converter		10 bits × 12 ch			10 bits × 12 ch					
D/A converter		8 bits × 2 ch			8 bits × 2 ch					
DMA controller		4 ch			4 ch					
Ports	I/O	84			84					
	Input	–			–					
Debug control unit		–		Provided (RUN/break)	–		Provided (RUN/break)	–		Provided (RUN/break)
Other peripheral functions		Watch timer: 1 ch CAN controller: 1 ch ROM correction: 4 points Real-time output Clock monitor/CRC			Watch timer: 1 ch CAN controller: 1 ch ROM correction: 4 points Real-time output LVI/clock monitor/CRC					
Operating frequency		When using main clock: 2.5 to 32 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz			When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz					
Power supply voltage		3.0 V to 3.6 V			2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V)					
Package		100-pin LQFP (14 × 14 mm)			100-pin LQFP (14 × 14 mm)					
Operating ambient temperature		–40°C to +85°C			–40°C to +85°C					

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

ASSP Lineup (CAN) (7/7)

Generic Name		V850ES/SJ2-H			V850ES/SJ2				
Part No.	On-chip CAN 1 ch	μPD703285HY	μPD703286HY	μPD70F3286HY	μPD703284Y	μPD70F3284Y	μPD703285Y	μPD703286Y	μPD70F3286Y
	On-chip CAN 2 ch	μPD703287HY	μPD703288HY	μPD70F3288HY	–	–	μPD703287Y	μPD703288Y	μPD70F3288Y
CPU name		V850ES			V850ES				
CPU performance (Dhrystone)		66 MIPS (@ 32 MHz)			43 MIPS (@ 20 MHz)				
Internal ROM		512 KB (mask)	640 KB (mask)	640 KB (flash)	384 KB (mask)	384 KB (flash)	512 KB (mask)	640 KB (mask)	640 KB (flash)
Internal RAM		40 KB	48 KB		32 KB		40 KB	48 KB	
External bus interface	Bus type	Multiplexed/separate			Multiplexed/separate				
	Address bus	24 bits			24 bits				
	Data bus	8/16 bits			8/16 bits				
	Chip select signal	4			4				
Memory controller		SRAM, etc.			SRAM, etc.				
Interrupt sources	Internal	64*1 /68*2 (including one NMI for each)			65*1/69*2 (including one NMI for each)				
	External	10 (10)*3 (including one NMI)			10 (10)*3 (including one NMI)				
Timer/counter		16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 9 ch 16-bit timer/event counter (TMQ) × 1 ch			16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 9 ch 16-bit timer/event counter (TMQ) × 1 ch				
Watchdog timer		1 ch			1 ch				
Serial interface		CSI × 4 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch UART (LIN compatible) × 1 ch			CSI × 4 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch UART (LIN compatible) × 1 ch				
A/D converter		10 bits × 16 ch			10 bits × 16 ch				
D/A converter		8 bits × 2 ch			8 bits × 2 ch				
DMA controller		4 ch			4 ch				
Ports	I/O	128			128				
	Input	–			–				
Debug control unit		–		Provided (RUN/break)	–	Provided (RUN/break)	–		Provided (RUN/break)
Other peripheral functions		Watch timer: 1 ch CAN controller: 1 ch*4 CAN controller: 2 ch*5 ROM correction: 4 points Real-time output Clock monitor/CRC			Watch timer: 1 ch CAN controller: 1 ch*6 CAN controller: 2 ch*7 ROM correction: 4 points Real-time output LVI/clock monitor/CRC				
Operating frequency		When using main clock: 2.5 to 32 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz			When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz				
Power supply voltage		3.0 V to 3.6 V			2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V)				
Package		144-pin LQFP (20 × 20 mm)			144-pin LQFP (20 × 20 mm)				
Operating ambient temperature		–40°C to +85°C			–40°C to +85°C				

*1. Products with 1 ch CAN only
*2. Products with 2 ch CAN only
*3. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*4. μPD703285HY/3286HY/F3286HY only
*5. μPD703287HY/3288HY/F3288HY only
*6. μPD703284Y/F3284Y/3285Y/3286Y/F3286Y only
*7. μPD703287Y/3288Y/F3288Y only

Generic Name		V850ES/SG1
Part No.		μPD703253Y
CPU name		V850ES
CPU performance (Dhrystone)		43 MIPS (@ 20 MHz)
Internal ROM		128 KB (mask)
Internal RAM		8 KB
External bus interface	Bus type	Multiplexed/separate
	Address bus	22 bits
	Data bus	8/16 bits
	Chip select signal	–
Memory controller		SRAM, etc.
Interrupt sources	Internal	43 (including one NMI)
	External	9 (9)* (including one NMI)
Timer/counter		16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 6 ch
Watchdog timer		1 ch
Serial interface		CSI × 2 ch CSI/I²C × 1 ch UART × 2 ch I²C × 1 ch
A/D converter		10 bits × 12 ch
D/A converter		8 bits × 2 ch
DMA controller		4 ch
Ports	I/O	84
	Input	–
Debug control unit		–
Other peripheral functions		Watch timer: 1 ch, CAN controller: 1 ch ROM correction: 4 points, clock monitor
Operating frequency		When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz
Power supply voltage		2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V) (@ 20 MHz)
Package		100-pin LQFP (14 × 14 mm)
Operating ambient temperature		–40°C to +85°C

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

ASSP Lineup (Car Audio/Vehicle Navigation Control) (1/4)

Generic Name		V850E2/SG4-H (Under planning)		V850E2/SJ4-H (Under planning)		V850E2/SK4-H (Under development)	
Part No.		μPD70F4013	μPD70F4014	μPD70F4015	μPD70F4016	μPD70F4017	μPD70F4018
CPU name		V850E2M		V850E2M		V850E2M	
CPU performance (Dhrystone)		400 MIPS (@ 160 MHz)		400 MIPS (@ 160 MHz)		400 MIPS (@ 160 MHz)	
Internal ROM		1 MB (flash)	1.5 MB (flash)	1 MB (flash)	1.5 MB (flash)	1.5 MB (flash)	2 MB (flash)
Internal RAM		96 KB	128 KB	96 KB	128 KB	128 KB	192 KB
Data flash		32 KB		32 KB		32 KB	
External bus interface	Bus type	Multiplexed SRAM I/F		SDRAM I/F, multiplexed/separate SRAM I/F		SDRAM I/F, multiplexed/separate SRAM I/F	
	Address bus	20 bits		24 bits		24 bits	
	Data bus	8/16 bits		8/16 bits		8/16/32 bits	
	Chip select signal	–		3		4	
Memory controller		SRAM, etc.		SDRAM, SRAM, etc.		SDRAM, SRAM, etc.	
Interrupt sources	Internal	10		16		16	
	External	144		161		208	
Timer/counter		32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 1 unit		32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 1 unit		32-bit timer: 4 ch × 1 unit 16-bit timer: 16 ch × 2 units	
Watchdog timer		2 ch		2 ch		2 ch	
Serial interface		UART/CSI × 4 ch CSI × 2 ch CSI (With FIFO) × 2 ch I²C × 4 ch MediaLB × 1 ch		UART/CSI × 5 ch CSI × 2 ch CSI (With FIFO) × 3 ch I²C × 4 ch MediaLB × 1 ch		UART/CSI × 5 ch CSI × 2 ch CSI (With FIFO) × 3 ch I²C × 4 ch MediaLB × 1 ch	
A/D converter		10 bits × 8 ch × 1 unit		10 bits × 16 ch × 1 unit		10 bits × 16 ch × 1 unit	
D/A converter		–		–		–	
DMA controller		16 ch		16 ch		16 ch	
Ports	I/O	58		100		127	
	Input	–		–		–	
Debug control unit		Provided (RUN/break)		Provided (RUN/break)		Provided (RUN/break)	
Ethernet controller		–		–		1 ch	
Other peripheral functions		IEBus controller/CAN controller: 1 ch Power-on clear (option), LVI, clock monitor, data CRC, Hardware bus common memory: 32 KB, SSCG		IEBus controller: 1 ch CAN controller: 2 ch Power-on clear (option), LVI, clock monitor, data CRC, Hardware bus common memory: 32 KB, SSCG		IEBus controller: 1 ch CAN controller: 2 ch Power-on clear (option), LVI, clock monitor, data CRC, Hardware bus common memory: 32 KB, SSCG	
Operating frequency		When using main clock: 160 MHz (max.) When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz		When using main clock: 160 MHz (max.) When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz		When using main clock: 160 MHz (max.) When using subclock: 32.768 kHz When using high-speed internal oscillation clock: 8 MHz When using low-speed internal oscillation clock: 240 kHz	
Power supply voltage		1.1 V to 1.3 V (internal)/3.0 V to 3.6 V (external)		1.1 V to 1.3 V (internal)/3.0 V to 3.6 V (external)		1.1 V to 1.3 V (internal)/3.0 V to 3.6 V (external)	
Package		100-pin LQFP (14 × 14 mm)		144-pin LQFP (20 × 20 mm)		176-pin LQFP (24 × 24 mm)	
Operating ambient temperature		−40°C to +85°C, −40°C to +105°C		−40°C to +85°C, −40°C to +105°C		−40°C to +85°C, −40°C to +105°C	

Numbers of channels indicate the total number implemented on the product. The actual number of usable channels differs depending on multi-use pin settings.

Generic Name		V850ES/SG1
Part No.		μPD703252Y
CPU name		V850ES
CPU performance (Dhrystone)		43 MIPS (@ 20 MHz)
Internal ROM		256 KB (mask)
Internal RAM		12 KB
External bus interface	Bus type	Multiplexed/separate
	Address bus	22 bits
	Data bus	8/16 bits
	Chip select signal	–
Memory controller		SRAM, etc.
Interrupt sources	Internal	36 (including one NMI)
	External	9 (9)* (including one NMI)
Timer/counter		16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 5 ch
Watchdog timer		1 ch
Serial interface		CSI × 2 ch CSI/I²C × 1 ch UART × 2 ch I²C × 1 ch
A/D converter		10 bits × 12 ch
D/A converter		–
DMA controller		–
Ports	I/O	84
	Input	–
Debug control unit		–
Other peripheral functions		Watch timer: 1 ch, IEBus controller: 1 ch ROM correction: 4 points, clock monitor
Operating frequency		When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz
Power supply voltage		2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V)
Package		100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)
Operating ambient temperature		−40°C to +85°C

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

ASSP Lineup (Car Audio/Vehicle Navigation Control) (2/4)

Generic Name		V850ES/SG3					
Part No.	On-chip IEBus	μPD70F3333	μPD70F3334	μPD70F3340	μPD70F3341	μPD70F3342	μPD70F3343
	On-chip IEBus/CAN	μPD70F3335	μPD70F3336	μPD70F3350	μPD70F3351	μPD70F3352	μPD70F3353
CPU name		V850ES					
CPU performance (Dhrystone)		69 MIPS (@ 32 MHz)					
Internal ROM		256 KB (flash)	384 KB (flash)	512 KB (flash)	640 KB (flash)	768 KB (flash)	1024 KB (flash)
Internal RAM		24 KB	32 KB	40 KB	48 KB	60 KB	
External bus interface	Bus type	Multiplexed/separate					
	Address bus	22 bits					
	Data bus	8/16 bits					
	Chip select signal	–					
Memory controller		SRAM, etc.					
Interrupt sources	Internal	52 (including one NMI)					
	External	9 (9)*1 (including one NMI)					
Timer/counter		16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 6 ch 16-bit timer/event counter (TMQ) × 1 ch					
Watchdog timer		1 ch					
Serial interface		CSI × 3 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch					
A/D converter		10 bits × 12 ch					
D/A converter		8 bits × 2 ch					
DMA controller		4 ch					
Ports	I/O	84					
	Input	–					
Debug control unit		Provided (RUN/break)					
Other peripheral functions		Watch timer: 1 ch IEBus controller/CAN controller*2: 1 ch ROM correction: 4 points Real-time output LVI/clock monitor/CRC					
Operating frequency		When using main clock: 2.5 to 32 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz					
Power supply voltage		2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V)					
Package		100-pin LQFP (14 × 14 mm)					
Operating ambient temperature		−40°C to +85°C					

*1. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*2. μPD70F3335/F3336/F3350/F3351/F3352/F3353 only

Generic Name		V850ES/SJ3				
Part No.	On-chip IEBus	μPD70F3344	μPD70F3345	μPD70F3346	μPD70F3347	μPD70F3348
	On-chip IEBus/CAN (1 ch)	μPD70F3354	μPD70F3355	μPD70F3356	μPD70F3357	μPD70F3358
	On-chip IEBus/CAN (1 ch), CAN (1 ch)	μPD70F3364	μPD70F3365	μPD70F3366	μPD70F3367	μPD70F3368
CPU name		V850ES				
CPU performance (Dhrystone)		69 MIPS (@ 32 MHz)				
Internal ROM		384 KB (flash)	512 KB (flash)	640 KB (flash)	768 KB (flash)	1024 KB (flash)
Internal RAM		32 KB	40 KB	48 KB	60 KB	
External bus interface	Bus type	Multiplexed/separate				
	Address bus	24 bits				
	Data bus	8/16 bits				
	Chip select signal	4				
Memory controller		SRAM, etc.				
Interrupt sources	Internal	65*1/69*2 (including one NMI for each)				
	External	10 (10)*3 (including one NMI)				
Timer/counter		16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 9 ch 16-bit timer/event counter (TMQ) × 1 ch				
Watchdog timer		1 ch				
Serial interface		CSI × 4 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch UART (LIN compatible) × 1 ch				
A/D converter		10 bits × 16 ch				
D/A converter		8 bits × 2 ch				
DMA controller		4 ch				
Ports	I/O	128				
	Input	–				
Debug control unit		Provided (RUN/break)				
Other peripheral functions		Watch timer: 1 ch IEBus controller/CAN controller*4: 1 ch CAN controller: 2 ch*5 ROM correction: 4 points Real-time output LVI/clock monitor/CRC				
Operating frequency		When using main clock: 2.5 to 32 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz				
Power supply voltage		2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V)				
Package		144-pin LQFP (20 × 20 mm)				
Operating ambient temperature		−40°C to +85°C				

*1. Products without CAN, product with 1 ch CAN only
*2. Products with 2 ch CAN only
*3. The figures in parentheses indicate the number of external interrupts that can be used to release STOP mode.
*4. μPD70F3354/F3355/F3356/F3357/F3358 only
*5. μPD70F3364/F3365/F3366/F3367/F3368 only

ASSP Lineup (Car Audio/Vehicle Navigation Control) (3/4)

Generic Name		V850E/SJ3-H			
Part No.	On-chip IEBus	μPD70F3474A	μPD70F3477A	μPD70F3934A	μPD70F3937A
	On-chip IEBus/CAN (1 ch)	μPD70F3475A	μPD70F3478A	μPD70F3935A	μPD70F3938A
	On-chip IEBus/CAN (1 ch), CAN (1 ch)	μPD70F3476A	μPD70F3479A	μPD70F3936A	μPD70F3939A
CPU name		V850E1			
CPU performance (Dhrystone)		95 MIPS (@ 48 MHz)			
Internal ROM		1280 KB (flash)	1536 KB (flash)	768 KB (flash)	1024 KB (flash)
Internal RAM		92 KB (internal RAM: 60 KB, expanded internal RAM: 32 KB)		76 KB (internal RAM: 60 KB, expanded internal RAM: 16 KB)	
External bus interface	Bus type	Multiplexed/separate			
	Address bus	24 bits			
	Data bus	8/16 bits			
	Chip select signal	3			
Memory controller		SRAM, etc.			
Interrupt sources	Internal	95*1/99*2/103*3 (including one NMI for each)			
	External	11 (11)*4 (including one NMI)			
Timer/counter		16-bit interval timer (TMM) × 3 ch 16-bit timer/event counter (TMP) × 9 ch (encoder count function: 2 ch) 16-bit timer/event counter (TMQ) × 1 ch			
Watchdog timer		1 ch			
Serial interface		UART/CSI × 1 ch, UART/I²C × 2 ch, UART/CSI/I²C × 1 ch, UART/CSI (FIFO compatible) × 1 ch, CSI/I²C × 1 ch, UART × 1 ch, UART (FIFO compatible) × 2 ch, CSI × 3 ch, CSI (FIFO compatible) × 1 ch, I²C × 2 ch or UART/CSI × 1 ch, UART/I²C × 1 ch, UART/CSI/I²C × 2 ch, UART/CSI (FIFO compatible) × 1 ch, CSI/I²C × 1 ch, UART × 1 ch, UART (FIFO compatible) × 2 ch, CSI × 2 ch, CSI (FIFO compatible) × 1 ch, I²C × 2 ch			
A/D converter		10 bits × 16 ch			
D/A converter		8 bits × 2 ch			
DMA controller		4 ch			
Ports	I/O	128			
	Input	–			
Debug control unit		Provided (RUN/break)			
Other peripheral functions		Watch timer: 1 ch Real-time counter (Watch timer): 1 ch IEBus controller/CAN controller*5: 1 ch CAN controller: 2 ch*6 ROM correction: 8 points Real-time output LVI/clock monitor/CRC, SSCG			
Operating frequency		When using main: 48 MHz (max.) When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz			
Power supply voltage		2.85 V to 3.6 V (A/D converter, D/A converter: 3.0 V to 3.6 V)			
Package		144-pin LQFP (20 × 20 mm)			
Operating ambient temperature		−40°C to +85°C			

*1. Products without CAN only
*2. Products with 1 ch CAN only
*3. Products with 2 ch CAN only
*4. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*5. μPD70F3475, 70F3478, 70F3935, 70F3938
*6. μPD70F3476, 70F3479, 70F3936, 70F3939

Generic Name		V850E/SJ3-H	V850E/SK3-H		
Part No.	On-chip IEBus	μPD70F3931A	μPD70F3480A	μPD70F3486A	μPD70F3925A
	On-chip IEBus, CAN (1 ch)	μPD70F3932A	μPD70F3481A	μPD70F3487A	μPD70F3926A
	On-chip IEBus, CAN (2 ch)	μPD70F3933A	μPD70F3482A	μPD70F3488A	μPD70F3927A
CPU name		V850E1	V850E1		
CPU performance (Dhrystone)		95 MIPS (@ 48 MHz)	95 MIPS (@ 48 MHz)		
Internal ROM		512 KB (flash)	1536 KB (flash)	1280 KB (flash)	1024 KB (flash)
Internal RAM		60 KB (internal RAM: 60 KB, expanded internal RAM: none)	92 KB (internal RAM: 60 KB, expanded internal RAM: 32 KB)		76 KB (internal RAM: 60 KB, expanded internal RAM: 16 KB)
External bus interface	Bus type	Multiplexed/separate	Multiplexed/separate		
	Address bus	24 bits	24 bits		
	Data bus	8/16 bits	8/16 bits		
	Chip select signal	3	3		
Memory controller		SRAM, etc.	SRAM, etc.		
Interrupt sources	Internal	89*1/93*2/97*3 (including one NMI for each)	95*1/99*2/103*3 (including one NMI for each)		
	External	11 (11)*4 (including one NMI)	11 (11)*4 (including one NMI)		
Timer/counter		16-bit interval timer (TMM) × 3 ch 16-bit timer/event counter (TMP) × 9 ch (encoder count function: 2 ch) 16-bit timer/event counter (TMQ) × 1 ch	16-bit interval timer (TMM) × 3 ch 16-bit timer/event counter (TMP) × 9 ch (encoder count function: 2 ch) 16-bit timer/event counter (TMQ) × 1 ch		
Watchdog timer		1 ch	1 ch		
Serial interface		UART/CSI × 1ch, UART/I²C × 2ch, CSI/I²C × 1ch, UART × 1ch, UART (FIFO compatible) × 2ch, CSI × 3ch, I²C × 1ch or UART/CSI × 1ch, UART/I²C × 1ch, UART/CSI/I²C × 1ch, CSI/I²C × 1ch, UART × 1ch, UART (FIFO compatible) × 2ch, CSI × 2ch, I²C × 1ch	UART/CSI × 1 ch, UART/I²C × 2 ch, UART/CSI/I²C × 1 ch, UART/CSI (FIFO compatible) × 1 ch, CSI/I²C × 1 ch, UART × 1 ch, UART (FIFO compatible) × 2 ch, CSI × 3 ch, CSI (FIFO compatible) × 1 ch, I²C × 2 ch or UART/CSI × 1 ch, CSI/I²C × 2 ch, UART × 5 ch, UART (FIFO compatible) × 2 ch, CSI × 3 ch, CSI (FIFO compatible) × 2 ch, I²C × 4 ch		
A/D converter		10 bits × 16 ch	10 bits × 16 ch		
D/A converter		8 bits × 2 ch	8 bits × 2 ch		
DMA controller		4 ch	4 ch		
Ports	I/O	128	156		
	Input	–	–		
Debug control unit		Provided (RUN/break)	Provided (RUN/break)		
Other peripheral functions		Watch timer: 1 ch Real-time counter (watch timer): 1 ch IEBus controller/CAN controller*5: 1 ch CAN controller: 2 ch*6 ROM correction: 8 points Real-time output LVI/clock monitor/CRC, SSCG	Watch timer: 1 ch Real-time counter (watch timer): 1 ch IEBus controller/CAN controller*7: 1 ch CAN controller: 2 ch*8 ROM correction: 8 points Real-time output LVI/clock monitor/CRC, SSCG		
Operating frequency		When using main clock: 48 MHz (max.) When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz	When using main clock: 48 MHz (max.) When using subclock: 32.768 kHz When using internal oscillation clock: 220 kHz		
Power supply voltage		2.85 V to 3.6 V (A/D converter, D/A converter: 3.0 V to 3.6 V)	2.85 V to 3.6 V (A/D converter, D/A converter: 3.0 V to 3.6 V)		
Package		144-pin LQFP (20 × 20 mm)	176-pin LQFP (24 × 24 mm)		
Operating ambient temperature		−40°C to +85°C	−40°C to +85°C		

*1. Products without CAN only
*2. Products with 1 ch CAN only
*3. Products with 2 ch CAN only
*4. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*5. μPD70F3932
*6. μPD70F3933
*7. μPD70F3481, 70F3487, 70F3926
*8. μPD70F3482, 70F3488, 70F3927

ASSP Lineup (Car Audio/Vehicle Navigation Control) (4/4)

Generic Name		V850ES/SG2-H			V850ES/SG2					
Part No.		μPD703272HY	μPD703273HY	μPD70F3273HY	μPD703270Y	μPD703271Y	μPD70F3271Y	μPD703272Y	μPD703273Y	μPD70F3273Y
CPU name		V850ES			V850ES					
CPU performance (Dhrystone)		66 MIPS (@ 32 MHz)			43 MIPS (@ 20 MHz)					
Internal ROM		512 KB (mask)	640 KB (mask)	640 KB (flash)	256 KB (mask)	384 KB (mask)	384 KB (flash)	512 KB (mask)	640 KB (mask)	640 KB (flash)
Internal RAM		40 KB	48 KB		24 KB	32 KB		40 KB	48 KB	
External bus interface	Bus type	Multiplexed/separate			Multiplexed/separate					
	Address bus	22 bits			22 bits					
	Data bus	8/16 bits			8/16 bits					
	Chip select signal	–			–					
Memory controller		SRAM, etc.			SRAM, etc.					
Interrupt sources	Internal	51 (including one NMI)			52 (including one NMI)					
	External	9 (9)*1 (including one NMI)			9 (9)*1 (including one NMI)					
Timer/counter		16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 6 ch 16-bit timer/event counter (TMQ) × 1 ch			16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 6 ch 16-bit timer/event counter (TMQ) × 1 ch					
Watchdog timer		1 ch			1 ch					
Serial interface		CSI × 3 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch			CSI × 3 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch					
A/D converter		10 bits × 12 ch			10 bits × 12 ch					
D/A converter		8 bits × 2 ch			8 bits × 2 ch					
DMA controller		4 ch			4 ch					
Ports	I/O	84			84					
	Input	–			–					
Debug control unit		–		Provided (RUN/break)	–		Provided (RUN/break)	–		Provided (RUN/break)
Other peripheral functions		Watch timer: 1 ch IEBus controller: 1 ch ROM correction: 4 points Real-time output Clock monitor/CRC			Watch timer: 1 ch IEBus controller: 1 ch ROM correction: 4 points Real-time output LVI/clock monitor/CRC					
Operating frequency		When using main clock: 2.5 to 32 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz			When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz					
Power supply voltage		3.0 V to 3.6 V			2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V)					
Package		100-pin LQFP (14 × 14 mm)			100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)*2					
Operating ambient temperature		−40°C to +85°C			−40°C to +85°C					

*1. The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.
*2. μPD703270Y/3271Y/F3271Y only

Generic Name		V850ES/SJ2-H			V850ES/SJ2				
Part No.		μPD703275HY	μPD703276HY	μPD70F3276HY	μPD703274Y	μPD70F3274Y	μPD703275Y	μPD703276Y	μPD70F3276Y
CPU name		V850ES			V850ES				
CPU performance (Dhrystone)		66 MIPS (@ 32 MHz)			43 MIPS (@ 20 MHz)				
Internal ROM		512 KB (mask)	640 KB (mask)	640 KB (flash)	384 KB (mask)	384 KB (flash)	512 KB (mask)	640 KB (mask)	640 KB (flash)
Internal RAM		40 KB	48 KB		32 KB		40 KB	48 KB	
External bus interface	Bus type	Multiplexed/separate			Multiplexed/separate				
	Address bus	24 bits			24 bits				
	Data bus	8/16 bits			8/16 bits				
	Chip select signal	4			4				
Memory controller		SRAM, etc.			SRAM, etc.				
Interrupt sources	Internal	64 (including one NMI)			65 (including one NMI)				
	External	10 (10)* (including one NMI)			10 (10)* (including one NMI)				
Timer/counter		16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 9 ch 16-bit timer/event counter (TMQ) × 1 ch			16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 9 ch 16-bit timer/event counter (TMQ) × 1 ch				
Watchdog timer		1 ch			1 ch				
Serial interface		CSI × 4 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch UART (LIN compatible) × 1 ch			CSI × 4 ch UART (LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch UART (LIN compatible)/I²C × 2 ch UART (LIN compatible) × 1 ch				
A/D converter		10 bits × 16 ch			10 bits × 16 ch				
D/A converter		8 bits × 2 ch			8 bits × 2 ch				
DMA controller		4 ch			4 ch				
Ports	I/O	128			128				
	Input	–			–				
Debug control unit		–		Provided (RUN/break)	–		–		Provided (RUN/break)
Other peripheral functions		Watch timer: 1 ch IEBus controller: 1 ch ROM correction: 4 points Real-time output LVI/clock monitor/CRC			Watch timer: 1 ch IEBus controller: 1 ch ROM correction: 4 points Real-time output LVI/clock monitor/CRC				
Operating frequency		When using main clock: 2.5 to 32 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz			When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz When using internal oscillation clock: 200 kHz				
Power supply voltage		3.0 V to 3.6 V			2.85 V to 3.6 V (A/D converter: 3.0 V to 3.6 V)				
Package		144-pin LQFP (20 × 20 mm)			144-pin LQFP (20 × 20 mm)				
Operating ambient temperature		−40°C to +85°C			−40°C to +85°C				

* The figure in parentheses indicates the number of external interrupts that can be used to release STOP mode.

V850 Development Environment

The V850 development environment consists of tools designed to make the development of application systems using Renesas Electronics high-performance V850 microcontrollers more pleasant, faster, and more accurate. Each one of these development tools has features to fully exploit the performance of V850 microcontrollers.

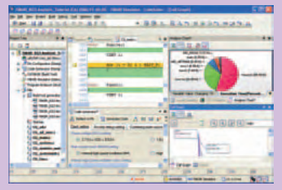
*CASE: Computer Aided Software Engineering

Development Environment Lineup

Software development > Debugging/verification > Writing

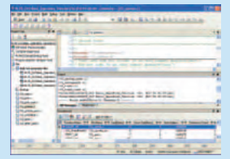
Development Environment

CubeSuite+ integrated development environment (free evaluation version available)



Full-spec-emulator (IECUBE2)

Renesas Flash Programmer flash programmer software (free evaluation version available)



Full-spec-emulator (IECUBE)

Software package SP850
(Includes project manager, compiler, assembler, and integrated debugger)

On-chip debugging emulator (E1)

Flash memory programmer (PG-FP5)

Real-time OS
RI850V4, RI850MP **

★★ : Under development

On-chip debugging emulator (MINICUBE2/MINICUBE)

Test Tool

Free evaluation versions of software tools to let you get started right away

Evaluation versions of the following products are available free of charge to help you build a V850 development environment. Use these free evaluation versions to get started before embarking on full-scale development work.

Lineup

- CubeSuite+ integrated development environment
- Renesas Flash Programmer

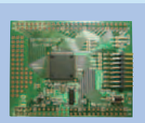
Download site for free evaluation versions of software tools

Free Tool DOWNLOAD

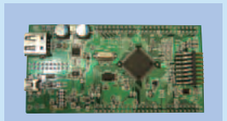
http://www.renesas.com/tool_evaluation

Testing evaluation boards

These CPU boards can be used with the E1 or MINICUBE2 on-chip debugging emulator (sold separately) to test the operation of V850 microcontrollers. You can try out all stages of the development process, from software development through test operation on the target system. All pins of the microcontroller are assigned to peripheral port connectors, making it possible to create evaluation circuits using commercially available universal boards.



QB-V850ESJG3L-TB
Low power consumption, mounted with V850ES/JG3-L



QB-V850ESJG3U-TB
Support for USB 2.0 (Host/Function) Mounted with V850ES/JG3-U

QB-F14T16-01

The adapter that converts the 14-pin/2.54 mm pitch connector of the E1 user I/F cable to the MINICUBE2-compliant 16-pin/2.54 mm pitch connector. It allows the E1 emulator to be used on a board designed for MINICUBE2.

CPU Board Lineup

http://www.renesas.com/cpu_board

Integrated Development Environment

CubeSuite+

Using the intuitive graphical user interface (GUI), operations involving different tools are consistent and easy to master.
An extensive tutorial is provided to help beginning users get up to speed.

Installation and setup
Integration of a variety of tools under a consistent GUI for enhanced ease of use

Using the tutorial

Anyone can try out CubeSuite+ by simply following the tutorial step by step, from program creation through debugging and programming of the microcontroller.

Customizing the GUI

Customize the work screen by docking, floating, and hiding interface elements freely. There are also settings for modifying the menus and icons. You can tailor the GUI to look and work exactly as you prefer.

*Optimize the layout optimized for the functions and tools in use.

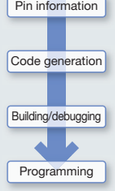
Centralized management of detailed settings

The Properties panel brings together all the setting items. You can select individual nodes of the project tree to display related information, making entering and searching for settings easy.

Coding
Rich support for editing program code

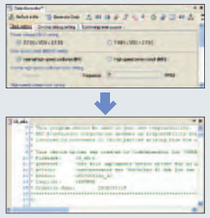
Project tree following the development sequence

The project tree takes into account the microcontroller development sequence. Simply click on a node to move to the corresponding operation.



Easy code generation*

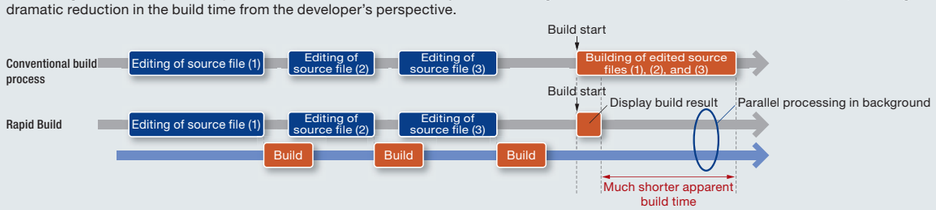
Simply make settings in the GUI to automatically generate program code (device drivers) for microcontroller peripheral functions (timers, UART, A/D converter, etc.).
* Some devices are not supported.



Building
A building environment designed to extract optimal performance from each MCU

Easy building

A conventional development environment requires you to edit all of the source files first and then build the entire project. This can be very time consuming. CubeSuite+ has a Rapid Build function that automatically starts building each time a source file is modified and saved, resulting in a dramatic reduction in the build time from the developer's perspective.

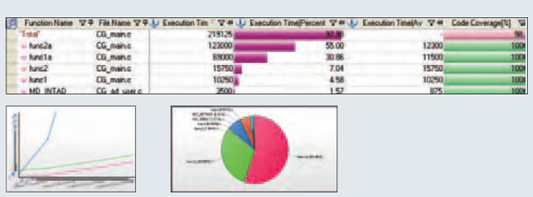


Debugging
Rich debugging functions that interoperate with a simulator or emulator

There is also an Action Event function that displays the value of a variable or variables when program execution reaches a specified address. This function allows convenient debugging, making it possible to access the variable name display function simply by right-clicking and without the need to spend time on additional builds.

Useful visual feedback and ability to search

A convenient listing makes it easy to check information on functions and variables. Graphical displays simplify tracking of variable values and confirming ratios of execution times among functions. Other useful extended functions include a Function Call Graph feature that displays function call relationships, making it possible to check which function called another function, and a Python Console function that makes it possible to write scripts to perform repetitive tasks, such as the operations associated with downloading programs to the microcontroller or operations following breaks.



Effective utilization of development resources

Customers can reuse existing development resources by migrating them to CubeSuite+.

Easy backup

The powerful backup function allows saving and restoring of complete projects and associated tool settings.

Implementation

Software Products

µITRON specification real-time OS (RI850V4, RI850MP)

Features

- Comply with µITRON specifications.
- Support power management function.
- Enable embedding of required functions only (selection of system calls to be used).
- Works with CubeSuite+ integrated development environment.
- Support application operation analysis through system performance analyzer (AZ).

Supported microcontrollers		V850		V850E2M dual-core
Product name		RI850V4	RX850V4	RI850MP★★
µITRON specification version		4.0		4.0
Timer control	Max. tasks	255		1023
	Task priority levels	31		31
Service calls		132		67
Kernel ROM size		Approx. 6 KB to 20 KB		—
Kernel RAM per task	Data	32 bytes		64 bytes
	Stack	128 bytes		136 bytes
Task switching time (task wake-up time using wup_tsk)		16 µs (V850E/MA 1.25 MHz, on-chip memory)		1.68 µs (V850E2/MN4@200MHz)

★★ : Under development

OSEK/VDX compliant OS (RX-OSEK850)

Features

- **Kernel**
  Compliant with OSEK/VDX OS Ver. 2.2.3 specifications
  Supports 4 conformance classes: BCC1, BCC2, ECC1, and ECC2.
- **Configurator**
  Configurator allowing easy system information creation provided as standard.
  Configuration files support formats compatible with OIL Ver. 2.5.
- **Task debugger (RD-OSEK850)**
  Task debugger effective for application debugging using RX-OSEK850 provided as standard.
- **System performance analyzer (AZ-OSEK850)**
  System performance analyzer for the RX-OSEK850 provided as standard.

Linked operation of CubeSuite+ integrated development environment and RI850V4 or RI78V4 real-time OS

Efficient development using convenient functions linked to CubeSuite+ integrated development environment

- Automatic setting of options required to build the OS.
- Displays OS management objects such as tasks and semaphores.
- Issues service calls for launching debugger tasks, setting event flags, etc.
- Graphical display of task operation history and service call issue history (System Performance Analyzer).

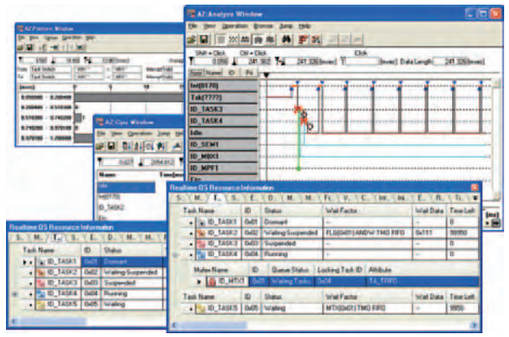


Illustration of linked function screens with CubeSuite+ integrated development environment

Applilet

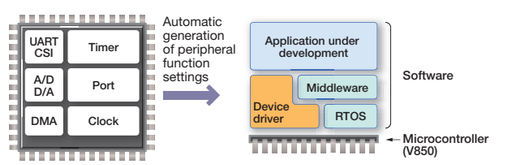
Applilet is a tool that lets you automatically generate software (device drivers) for microcontroller peripheral functions (clocks, timers, serial interfaces, A/D converters, DMA controllers, etc.) by entering settings via a graphical user interface (GUI).

Easy-to-understand GUI

Entering microcontroller peripheral function settings is as simple as pointing and clicking with the mouse. The setting process is intuitive, easy-to-understand, and elegant. Operation is simple enough for beginners, while providing fine-grained control for advanced users. Applilet is designed to reconcile these two seemingly contradictory goals.

Outputs C source code

Applilet generates device drivers as C source code. This makes it possible even for beginning users of microcontrollers to see at a glance the purpose of individual settings or processes. Of course it is only necessary to examine the source code when you need to analyze microcontroller setting methods in detail.



Product Name	Target Microcontroller
Applilet3 for V850ES_Jx3	V850ES/Jx3
Applilet3 for V850ES_Jx3-E	V850ES_Jx3-E
Applilet3 for V850ES_Jx3-H	V850ES_Jx3-H
Applilet3 for V850ES_Jx3-L	V850ES/Jx3-L
Applilet3 for V850ES_Sx3-H	V850ES/Sx3-H
Applilet2 for V850ESFx3	V850ES/Fx3
Applilet2 for V850ESSx3	V850ES/Sx3

Applilet requires installation of the Microsoft® .NET Framework, version 2.0, runtime and related files.

Emulator

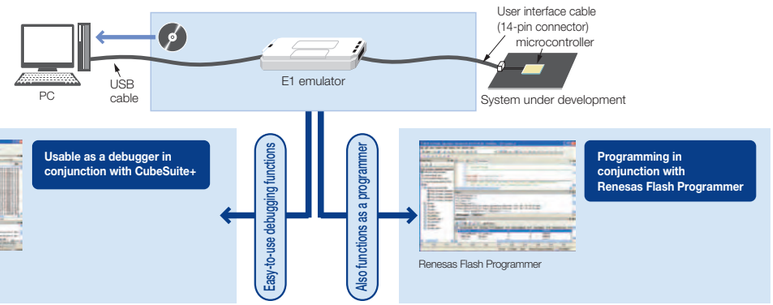
E1

An affordably priced model that doubles as a flash programmer and provides basic debugging functions including on-chip trace.

Features

- Low-priced emulator with basic debugging functions
- Easer to set up than in-circuit emulators using socket connections
- Ideal for evaluating analog functions such as A/D and D/A conversion characteristics
- Elegant graphical user interface (GUI) designed for flexibility and ease of use
- A hot plug-in function is under development that will allow connection of the emulator while a program is running. (A hot plug adapter, sold separately, is required.)
- Outer case made from environmentally friendly polylactide, a plant-based polymer

■ System configuration example



MINICUBE2

On-chip debugging emulator with programmer function

Features

- **Smallest size in the industry, saves space.**
  The compact dimensions are the smallest in the industry: 48 × 48 × 13.9 mm.
- **Economical, affordable price**
  The affordable price helps keep down development and mass production equipment costs.
- **Also available from retailers other than Renesas agents.**
  For details, visit http://japan.renesas.com/tool_retailer.

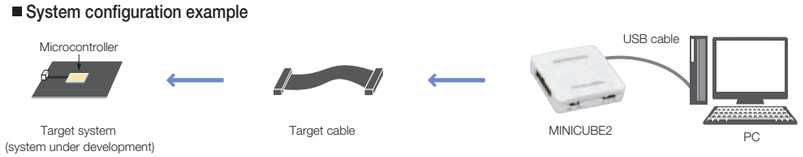
- **Center LED changes color to match the device and operating mode.**

Blue
Indicates startup in V850 microcontroller debugging mode.

Illumination
When the MINICUBE2 is connected only to the USB port of a PC and 15 seconds elapses, it enters illumination mode.

The colors shown are examples. There are additional illumination and flashing patterns other than those described above.

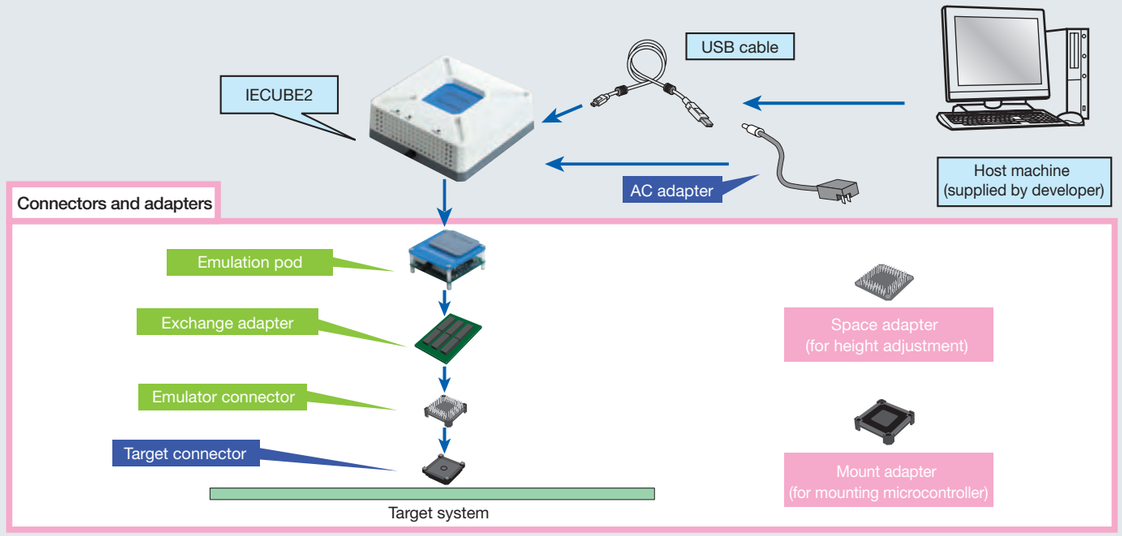
■ System configuration example



Note: Renesas software such as debuggers, USB drivers, and device files can be downloaded from the Renesas Electronics Web site.

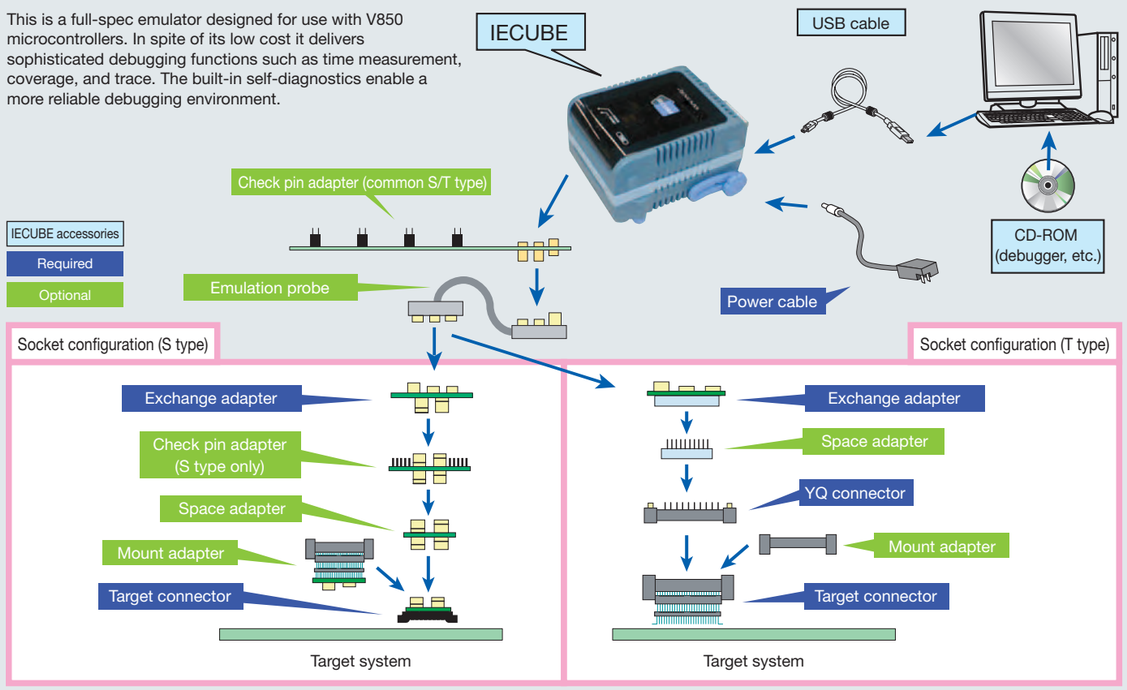
IECUBE2

This product is designed to enable efficient hardware and software debugging when developing systems employing V850E2M microcontrollers. The many debugging functions include event tracking, 9 MB/512,000 frame large-capacity trace, and time measurement. The trace function capacity can be extended to 2.25 GB/128 million frames with the addition of the optional QB-V850E2-SP.



IECUBE

This is a full-spec emulator designed for use with V850 microcontrollers. In spite of its low cost it delivers sophisticated debugging functions such as time measurement, coverage, and trace. The built-in self-diagnostics enable a more reliable debugging environment.



Flash Memory Programmers

Renesas Electronics flash memory programmers

PG-FP5

Features
- Can be used to write to all Renesas Electronics microcontrollers with internal flash memory.
- Many code storing features. (Up to eight types of codes and microcontroller information can be retained.)
- Device-specific information required for writing can be automatically set by using parameter files.
- Supports both on-board programming and program adapter (FA Series of Naito Densei Machida Mfg. Co., Ltd.) programming.
- Small, space-saving button layout with excellent operability.
- Can be manipulated in stand-alone mode or by a dedicated application on Windows™.
- Can be controled automatically from an external source because the PG-FP5 is compatible with communication commands.
- Supports remote interface features that allow an external system to manipulate and check writing and OK/ERROR indication.

Web site: http://www.renesas.com/products/tools/flash_prom_programming/flash_programmers/pg_fp5/pg_fp5_tools_product_landing.jsp
Visit this page for details on supported microcontrollers.

E1

Features
- Easy connection, allows connection to and programming of a V850 mounted in a target system.
- Can also be used with Renesas microcontrollers other than the V850.
- USB connection, no additional power supply needed.
- Also supports on-chip debugging.
- Low cost, compact, lightweight
- Environmentally friendly. All materials, from parts to packaging, are RoHS compliant.

Visit the following Web page for details of the E1 emulator:
http://renesas.com/e1
The E20 emulator provides the same programming functions as the E1 emulator.
Visit the following Web page for details of the E20 emulator:
http://www.renesas.com/_full_product_info_/products/tools/emulation_debugging/onchip_debuggers/e1/e1_tools_product_landing.jsp

MINICUBE2

Target Devices V850 microcontrollers
Features
- Supports both on-chip debugging and flash programming.
- Supports 8-bit to 32-bit single power supply flash memory versions.
- USB support through host machine interface.
- Enables writing via a microcontroller UART and CSI-HS.
- Supports both on-board programming and program adapter (FA Series of Naito Densei Machida Mfg. Co., Ltd.) programming.
- All controls are operated from a host machine-dedicated GUI.
- Use of host machine USB power supply eliminates the need for a power supply adapter to be connected to the programmer.
- Low-cost, compact and light.

See the following website for details:
http://www2.renesas.com/micro/en/development/asia/minicube2/minicube2.html

Partner flash memory programmers (1/2)

AF9723B

Manufacturer/Distributor Flash Support Group, Inc.
Target Devices V850 microcontrollers
Features
- Gang programmer with support for 256 Kb to 1 Gb (64 Mb standard).
- Also provides AF9850 ISB interface functionality, allowing high-speed downloading of master data.
- Ultrahigh-speed data writing at 2 Mb/sec. (when used with 9845).
- CE mark support.
- Supports flash devices, microcontrollers, and a variety of semiconductor card media by changing units.
- Custom units can be developed quickly.

Contact information
Tel: +81-53-459-1050 Fax: +81-53-455-6020
E-mail: SALES@j-fsg.co.jp
Web site: http://www.hokutoelectronic.com/

FlashPRO5 FL-PR5

Manufacturer/Distributor Naito Densei Machida Mfg. Co.
Target Devices V850 microcontrollers
Features
- Can be used to write to all Renesas Electronics microcontrollers with internal flash memory.
- Many code-storing features. (Up to eight types of codes and microcontroller information can be retained.)
- Device-specific information required for writing can be automatically set by using parameter files.
- Supports both on-board programming and program adapter programming.
- Small, space-saving button layout with excellent operability.
- Can be manipulated in stand-alone mode or by a dedicated Windows application.
- Can be controlled automatically from an external source because the FL-PR5 is compatible with communication commands.
- Supports remote interface features that allow an external system to manipulate and check writing and OK/ERROR indication.

Contact information
TEL: +81-42-750-4172 FAX: +81-42-750-4183
Email: info@ndk-m.co.jp
Website: http://www.ndk-m.co.jp/asmis/eng/index.html

FlashproHyper FL-PR5-HP-A

Manufacturer/Distributor Naito Densei Machida Mfg. Co.
Target Devices V850 microcontrollers
Features
- PC-less operation: Standalone specification that requires no PC on-site.
- USB memory support: Easy program management and programming history management with USB memory support.
- Gang programmer function: Adding external FL-PR5 units enables programming of up to eight devices simultaneously.
- LCD touch panel: 6.5-inch LCD display with touch panel input provides enhanced ease of use.
- Same programming functions as the FL-PR5: The well-established FL-PR5 is used as the programming unit, providing excellent performance and reliability.

Contact information
TEL: +81-42-750-4172 FAX: +81-42-750-4183
Email: info@ndk-m.co.jp
Website: http://www.ndk-m.co.jp/asmis/eng/index.html

Partner flash memory programmers (2/2)

NET IMPRESS series

Manufacturer/Distributor Yokogawa Digital Computer Corporation
Target Devices* V850 microcontrollers
Features
- ◆ Enables high-speed on-board programming of on-chip/external flash memory (up to 5 Mbps).
- ◆ Programming conditions for voluminous data and multiple devices (100 or more devices) can be saved, enabling instantaneous switching.
- ◆ Includes a model with a CAN interface for automotive applications (C"arNETIMPRESS).
- ◆ Can be used on a stand-alone basis or remotely controlled from a computer (Windows OS).
- ◆ Interface for external switch activation or PASS/ERROR signal output provided as standard.
- ◆ Applications provided based on proven manufacturing line performance.
- ◆ Extensive customer support (domestic and international).

Contact information
TEL: U.S.A. +1-770-253-7000 (Yokogawa Corporation of America)
Germany +49-721-9628-0 (Hitex Development Tools GmbH)
France, UK +33-1-43-41-06-37 (Ashling Microsystems Ltd.)
Korea +82-2-551-0660 (Yokogawa Measuring Instruments Korea Corp.)
China +86-10-8522-1699 (Yokogawa Shanghai Trading Co., Ltd.)
India +91-80-4158-6000 (Yokogawa India Ltd.)
Other Asia +65-6241-9933 (Yokogawa Engineering Asia Pte. Ltd.)
Other Countries +81-422-52-5606 (Yokogawa Digital Computer Corporation)
FAX: U.S.A. +1-770-251-6427 (Yokogawa Corporation of America)
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Other Countries +81-422-52-4499 (Yokogawa Digital Computer Corporation)
Email: info-impress@yokogawa-digital.com
Website: http://www.yokogawa-digital.com/en/

Flash programming system Y3000-8

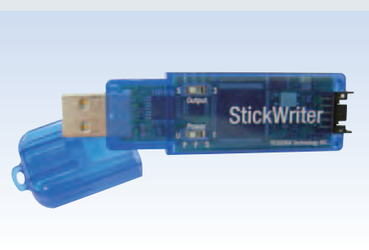
Manufacturer/Distributor Wave Technology Co., Ltd.
Target Devices* V850 microcontrollers
Features
- ◆ Realizes close to device capacity processing speed. Processes verify cycles four times faster than conventional programmers.
- ◆ PASS/FAIL results, checksum values, and task count displayed on computer screen in viewer-friendly color to improve operability and reduce errors.
- ◆ Standardized basic algorithms and socket board enable use in a range of environments, from development to mass production.

Contact information
TEL: +81-3-5452-3101 FAX: +81-3-5452-3102
Email: sales.support@wavetechnology.co.jp
Website: http://www.wavetechnology.co.jp/en/index.html

StickWriter

Manufacturer/Distributor TESSERA Technology Inc.
Target Devices* V850 microcontrollers
Features
- ◆ Programmer for flash memory microcontrollers with single power supply enables development and mass production regardless of location.
- ◆ Compact size that can directly be connected to a USB connector.
- ◆ Can be written on stand-alone basis by supplying power to the target board.
- ◆ High-speed download of 1 MB hex file within about 10 seconds.
- ◆ Board with wirings for flash programming eliminates need for wiring processing.

Contact information
TEL: +81-44-271-7533 FAX: +81-44-271-7534
Website: http://www.tessera.co.jp/eng/



Stick GANG Writer

Manufacturer/Distributor TESSERA Technology Inc.
Target Devices* V850 microcontrollers
Features
- ◆ GANG type programmer using StickWriter as a writing module.
- ◆ Internal flash memory that can store up to eight files.
- ◆ New devices can be supported by replacing the dedicated adapter board.
- ◆ Stand-alone writing that does not need a computer.
- ◆ AC adapter supporting AC 240 V can also be used outside of Japan.

Contact information
TEL: +81-44-271-7533 FAX: +81-44-271-7534
Website: http://www.tessera.co.jp/eng/

* Be sure to check the Renesas Electronics website for the latest news and details related to target devices. Check with related manufacturers for applicability to mass-produced lines.

Mass production support environment for your needs.

Programming by the customer (You can select the mass production method with the largest merit, according to delivery time or mass production quantity.)

Delivery time*1: Practically none, highly flexible

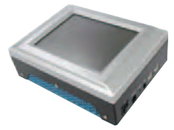
■ Flash memory programmers
Various products selectable for your purposes and price range

*Support details differ depending on the product. Contact the manufacturer for information on suitability for use on mass production lines.

Stick GANG Writer*
TESSERA
Technology Inc.

StickWriter*
TESSERA
Technology Inc.

AF9723B
Flash Support Group, Inc.



FL-PR5-HP-A
Naito Densei Machida Mfg. Co.

PG-FP5
Renesas Electronics

FL-PR5
Naito Densei Machida Mfg. Co.

NET IMPRESS series*
Yokogawa Digital
Computer Corporation

Y3000-8*
Wave Technology Co., Ltd.

External programming (programming service partners)

Flexible support for small-volume programming and short delivery time

■ The following programming service partners support microcontrollers manufactured by Renesas Electronics.

Synchro-work Corporation

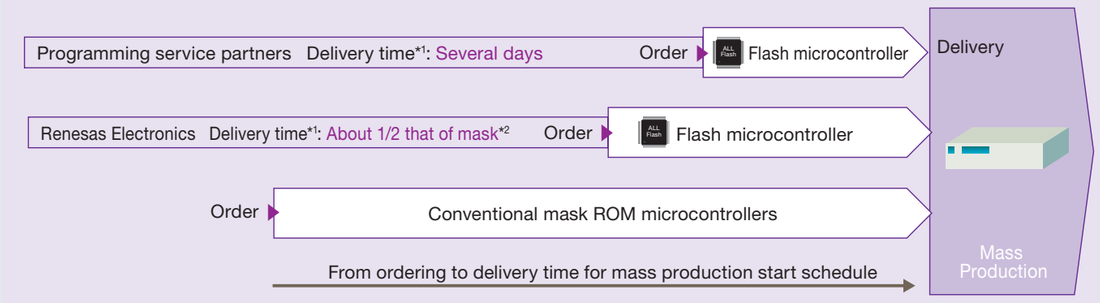
Flash Support Group

Programmed products (Renesas Electronics)

Shipment form same as that of mask ROM microcontrollers

■ The same way as mask ROM microcontrollers, programmed products can be delivered with a short TAT

*Contact the Renesas Electronics sales department or a sales agent for information on supported microcontrollers.



*1. Period from completion of software until start of mass production. *2. Delivery time may vary depending on purchase conditions, such as order quantity.

Development Tools

V850 Development environment

Application	MCU	CPU board*1	Real-time OS	Integrated development environment*3	On-chip debugging emulator*4	Full-spec emulator*5	Flash memory programming tools	
							Flash programmer software*7	Flash memory programmer*8
General-purpose	V850ES/Hx3	QB-V850ESHG3-TB	RI850V4	CubeSuite+	E1/E20	IECUBE	RFP	PG-FP5 or E1/E20
	V850ES/Jx3	QB-V850ESJJ3-TB						
	V850ES/Jx3-L	QB-V850ESJG3L-TB						
	V850ES/Jx3-H	QB-V850ESJG3U-TB						
	V850ES/Jx3-U	QB-V850ESJG3U-TB						
	V850ES/Jx3-E	QB-V850ESJJ3E-TB						
	V850ES/ST2	–		SP850	–	IE-V850ES-G1*6 IE-703220-G1-EM1*6	–	–
	V850E2/MN4	QB-V850E2MN4DUAL-TB	RI850V4 and RI850MP*2	CubeSuite+	E1/E20	–	RFP**	**
	V850E2/ML4	***		CubeSuite+**	E1/E20**			
	V850E/MA3	–		CubeSuite+	E1/E20	IECUBE	RFP	PG-FP5 or E1/E20
	V850E/ME2	–		SP850	MINICUBE	–	–	–
	V850E2/ME3	–						
	V850E/IG4 V850E/IH4	QB-V850EIH4H-TB		CubeSuite+	E1/E20	–	RFP	PG-FP5 or E1/E20
	V850E/IG4-H V850E/IH4-H	QB-V850EIH4H-TB						
	V850E/IF3	QB-V850EIG3-TB				IECUBE		
	V850E/IG3	QB-V850EIG3-TB						
	V850E/IA4	–						
	V850E/IA3	–						
	V850E/IA2	–		SP850	–	IE-V850E-MC*6 IE-703114-MC-EM1*6	–	PG-FP5
	V850E/IA1	–				IE-V850E-MC*6 IE-703116-MC-EM1*6		
	V850ES/IK1	–		CubeSuite+	E1/E20	IECUBE	RFP	PG-FP5 or E1/E20
	V850ES/IE2	QB-V850ESIE2-TB						
Automotive	V850E/Dx3	–		SP850	MINICUBE2 or MINICUBE		QBP	PG-FP5 orMINICUBE2
	V850E2/Fx4	–		CubeSuite+	E1/E20	IECUBE2	RFP	PG-FP5 or E1/E20
	V850E2/Fx4-L	–		CubeSuite+**	E1/E20**		RFP**	**
	V850E2/Fx4-H	–		CubeSuite+	E1/E20		RFP	PG-FP5 or E1/E20
	V850E2/FK4-G	–						
	V850E2/Fx4-M	–						
	V850ES/Fx3	–				IECUBE		
	V850ES/Fx3-L	–						
	V850ES/Fx2	–						
	V850E2/Sx4-H	–				IECUBE2	RFP**	PG-FP5
	V850ES/Sx3	–				IECUBE	RFP	PG-FP5 or E1/E20
	V850E/Sx3-H	–						
	V850ES/SJ2	–						
	V850ES/SG2	–						
	V850ES/SJ2-H	–						
	V850ES/SG2-H	–						
	V850ES/SG1	–			–		–	–

*1. The QB-F14T16-01 14-pin/16-pin conversion adapter (sold separately) is required to connect the CPU board and E1/E20 emulator.
*2. RI850MP is for the dual-core V850E2M.
*3. The CubeSuite+ integrated development environment V850 license pack product is available in two versions: the R0C08500QSW01D with install media and the R0C08500QSW01N without install media. A free evaluation version is available for download from the Renesas Electronics Web site. Software tool free evaluation versions: http://japan.renesas.com/tool_evaluation
*4. The debugging functions of the E1 and E20 on-chip debugging emulators are identical.
*5. Refer to the following Web pages for information on connecting the IECUBE and IECUBE2 to the target.
IECUBE: http://japan.renesas.com/iecube
IECUBE2: http://japan.renesas.com/iecube2
*6. This product is no longer available for sale, but it is still supported.
*7. RFP stands for Renesas Flash Programmer. A free evaluation version is available for download from the Renesas Electronics Web site. Software tool free evaluation versions: http://japan.renesas.com/tool_evaluation
*8. The E1 and E20 on-chip debugging emulators also provide programming functionality. The programming functions of the E1 and E20 are identical.
** Under development
*** Under study

Information on Renesas Partners

The alliance of Renesas partners comprises more than 700 companies worldwide.

Renesas Electronics and our more than 700 alliance partners worldwide are working together to provide customers with the tools and services they need to develop outstanding products.

General Web page for information on Renesas partners: http://renesas.com/partners

Renesas microcontroller customers
- View information on partner companies arranged by product and service.
- Search for partner companies by supported Renesas microcontroller, arranged by company name or product type.
- View a listing of partner companies in Japan and overseas.

Tool vendor partners
- Tool vendor partners can register online.
- Registered partners can log in to their accounts and update information.

Listing of V850 partners

■ IDE/Compilers/Code generators
Accurate Technologies
CATS CO.,LTD.
CriticalBlue
dSPACE GmbH
Gaio Technology Co., Ltd.
Green Hills Software
IAR Systems
MathWorks
Red Hat, Inc.
Ubiquitous Corporation
Vector Informatik GmbH

■ Co-verification
Accurate Technologies
ETAS GmbH
Gaio Technology Co., Ltd.
IAR Systems
Synopsys
Vector Informatik GmbH
Yokogawa Digital Computer Corporation

■ OS
EB (Elektrobit)
ETAS GmbH
Green Hills Software
SEGGER Microcontroller
Vector Informatik GmbH

■ Middleware/Drivers/Softaware IP
Aplix Corporation
E-Globaledge Corporation
eSOL Co., Ltd.
Kyoto Software Research, Inc.
Mentor Graphics Corporation
Ubiquitous Corporation
Vector Informatik GmbH

■ Emulators and related emulation tools
Accurate Technologies
ETAS GmbH
Green Hills Software
iSYSTEM AG
Lauterbach
Tokyo Eletech Corporation
Yokogawa Digital Computer Corporation

■ Starter kits/Evaluation borads/ Platforms
Sophia Systems Co., Ltd.
Vector Informatik GmbH
Yokogawa Digital Computer Corporation

■ Programmers
Flash Support Group, Inc.
Hokuto Denshi Co.,Ltd.
Tokyo Eletech Corporation
Vector Informatik GmbH
WaveTechnology Co., Ltd.
Yokogawa Digital Computer Corporation

V850 Website

Information about V850 microcontrollers and the V850 microcontroller development environment can be found at the Renesas Electronics Microcontrollers Website.

http://www2.renesas.com/micro/en/promotion/allflash/

Product Lineup

- Products are categorized according to bit count and application, enabling direct access to the product you need.
- A variety of information can be accessed, including product features, product lineups, documents and related information.

Design Support

- The website provides a range of helpful information for designers, including sample programs and characteristics data.
- The extensive FAQ helps with troubleshooting and offers useful design hints.

Development Tools Download

- V850 microcontroller development tools can be downloaded from this area. Customers who are registered users can receive upgrade information by email.

  http://www2.renesas.com/micro/en/ods/index.html

MEMO

MEMO

Renesas Electronics Corporation Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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http://www.renesas.com

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Renesas Electronics Europe GmbH
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