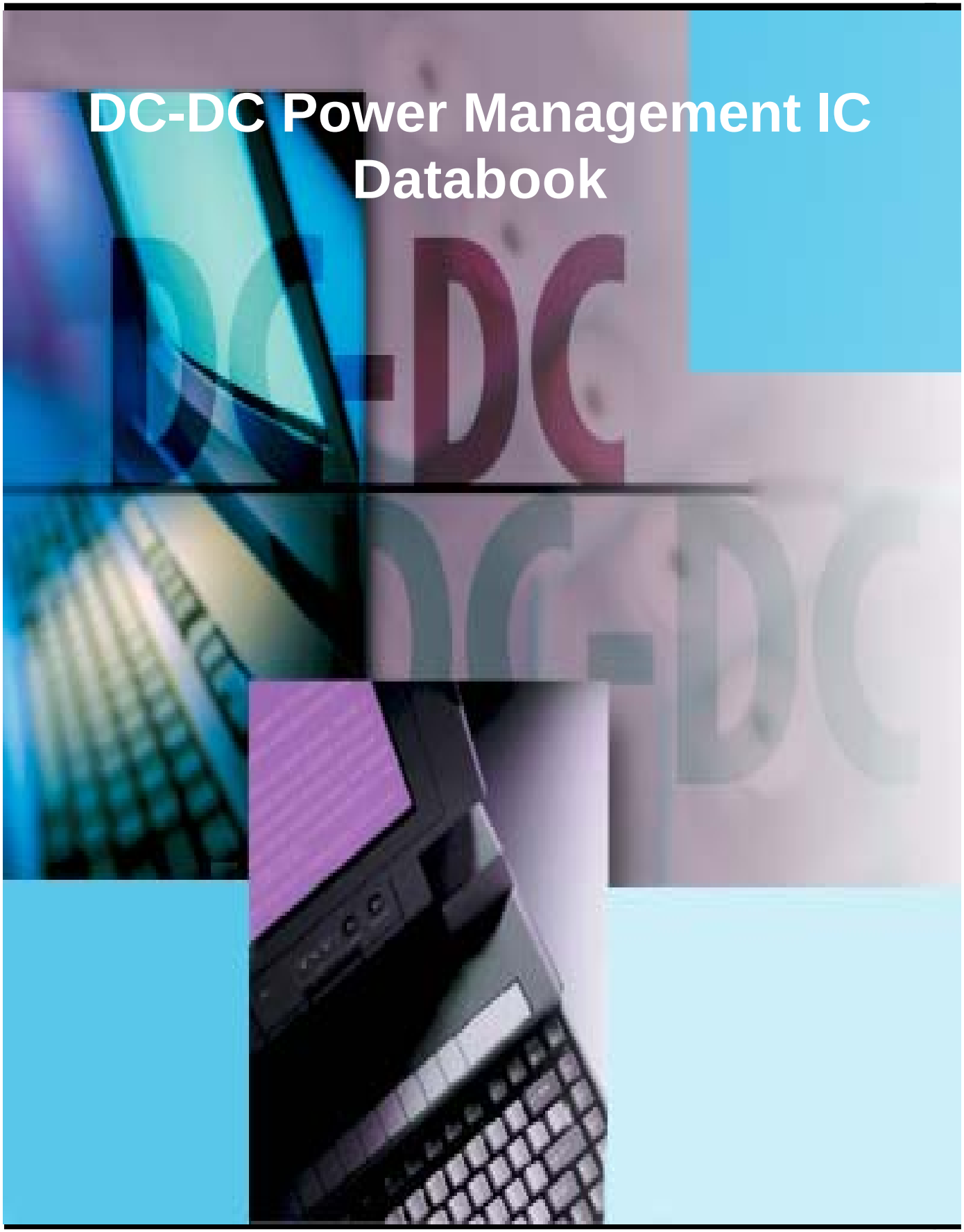
International
IOR Rectifier

Designer's Manual

DC-DC Power Management IC Databook



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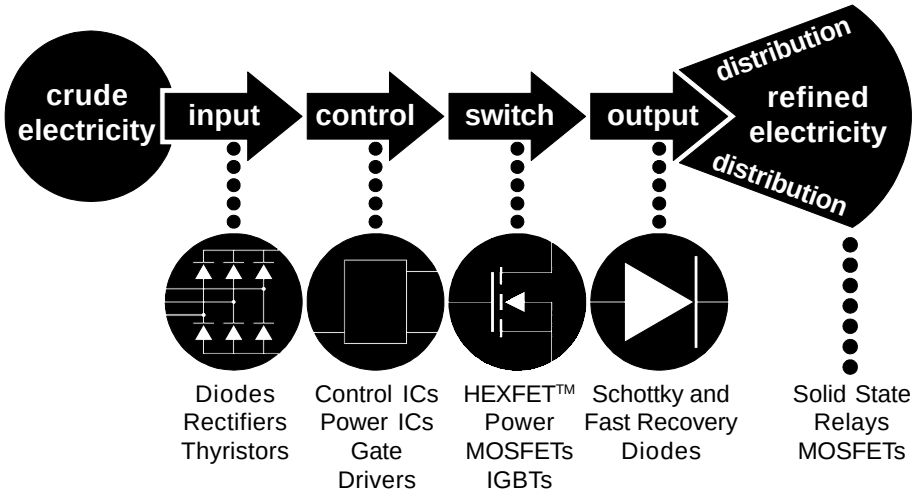
Section 1: General Information

Introduction
The Power Conversion Process

At International Rectifier, we've spent the last 55 years dedicated to improving the conversion of electricity from its crude form to its refined form. The Power Conversion Process takes crude energy in an inconvenient format and refines it to exactly what the load requires. International Rectifier is dedicated to this process. We picture it as a four-stage process, with an additional stage for distribution.



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Part Identification

IRU XXXX -XX X XX XX

IR Prefix

Part Number
Example: 1010

Voltage
Example:
-25 refers to a 2.5V fixed voltage option
-33 refers to a 3.3V fixed voltage option
Blank means Variable voltage option

Temperature Range
C = 0°C to 70°C*****
I = -25°C to 85°C
E = -40°C to 85°C
***Note:** Some regulators are rated up to 180°C max.

Package
See table below for all package options

Other Options
Example:
TR = tape & reel

Package Offering

PACKAGE DESCRIPTION	PACKAGE DESIG
TO-252 D-Pak 2-Pin	D
TSSOP 8, 14, 16, 20 and 24-Pin	F
MLPM 3x3 6-Pin	H
SOT-23 3-Pin	L3
SOT-23 5-Pin	L5
TO-263 3, 5 and 7-Pin	M
Ultra Thin-Pak™ 2, 3, 5 and 7-Pin	P
QSOP Narrow Body 24-Pin	Q
QSOP Wide Body 36-Pin	Q
SOIC Narrow Body 8, 14 and 16-Pin	S
TO-220 3, 5 and 7-Pin	T
SOIC Wide Body 20, 24 and 28-Pin	W
SOT-223 3-Pin	Y

Quality / Reliability Program

Qualification:

A minimum qualification testing is required to be performed on all new products/processes or any major process changes in the production line. A major change in the process will include an additional construction analysis. All samples will be collected from five different lots. Table I describes these requirements:

TABLE I

Test Description	Test Condition	Test Duration	Sample Size/ Acceptance
Operating Life Test	T_A = 125°C T_A = 150°C	1000 Hours 191 Hours	77 / 0 77 / 0
Autoclave	T_A = 121°C, 15 psi, 100% RH	168 Hours	45 / 0
Temperature Cycle	Air to Air, -65°C to +150°C	100 Cycles	45 / 0
Thermal Shock	Liquid to Liquid, -55°C to +125°C	100 Cycles	45 / 0
Power Cycle	Power cycle "ON" and "OFF" at maximum rated current as required to keep the case temperature between 40°C and 125°C	10,000 cycles	45 / 0
Highly Accelerated Stress Test (HAST)	T_A = + 85°C, RH = 85%, Biased T_A = +130°C, RH = 85%, Biased	1000 Hours 100 Hours	45 / 0 45 / 0

On-Going Reliability Program

An on-going reliability program has been implemented to ensure continuous shipment of quality parts. On a regular basis, a minimum sample of parts according to their package outline and functionality will be selected and be introduced to certain testing procedures as described in Table II.

TABLE II

Test Description	Test Condition	Test Duration	Sample Size/ Acceptance
Operating Life Test	T_A = 125°C	168 Hours	77 / 0
Autoclave	T_A = 121°C, 15 psi, 100% RH	96 Hours	45 / 0
Temperature Cycle	Air to Air, -65°C to +150°C	100 Cycles	45 / 0
Thermal Shock	Liquid to Liquid, -55°C to +125°C	100 Cycles	45 / 0
Highly Accelerated Stress Test (HAST)	T_A = +130°C, RH = 85%, Biased	100 Hours	45/0

On-Going Production Program

As part of our on going quality program, a minimum sample of 500 pieces from every production lot will be burned in a minimum of 168 hours at 125°C. All the data will be collected and every single rejected unit will be evaluated. This analysis will be done for a minimum of five production lots.

Also, as part of this program, all production parts will be tested for all extreme temperature requirements. The yield analysis from every lot at these extreme temperatures will enable us to optimize our probe programming while screening out marginal devices at these extreme temperatures.

Cross Reference by Manufacturer

ALPHA / SIPEX SEMICONDUCTOR

Part #	IR Cross	Comments
AS1115	IRU1010	Better Dropout Voltage
AS1115-18	IRU1010-18	Better Dropout Voltage
AS1115-25	IRU1010-25	Better Dropout Voltage
AS1115-33	IRU1010-33	Better Dropout Voltage
AS1117	IRU1117	Better Dropout Voltage
AS1117-18	IRU1117-18	Better Dropout Voltage
AS1117-25	IRU1117-25	Better Dropout Voltage
AS1117-33	IRU1117-33	Better Dropout Voltage
AS1580	IRU1175	Better Dropout Voltage
AS1581	IRU1160	Better Dropout Voltage
AS1582	IRU1150	Better Dropout Voltage
AS2810	IRU1010	
AS2810-18	IRU1010-18	
AS2810-25	IRU1010-25	
AS2810-33	IRU1010-33	
AS2815	IRU1015	
AS2830	IRU1030	Better Dropout Voltage
AS2830-33	IRU1030-33	Better Dropout Voltage
AS2840	IRU1050	Better Dropout Voltage
AS2840-33	IRU1050-33	Better Dropout Voltage
AS2850	IRU1050	Better Dropout Voltage
AS2850-33	IRU1050-33	Better Dropout Voltage
AS2870	IRU1075	Better Dropout Voltage
AS2884	IRU1075	
AS2885	IRU1050	
AS2885-33	IRU1050-33	Better Dropout Voltage
AS2887	IRU1030	Better Dropout Voltage
AS2887-33	IRU1030-33	Better Dropout Voltage

ADVANCED MONOLITHIC SYSTEMS (AMS)

Part #	IR Cross	Comments
AMS1083	IRU1075	Better Dropout Voltage
AMS1084	IRU1050	Better Dropout Voltage
AMS1084-33	IRU1050-33	Better Dropout Voltage
AMS1085	IRU1030	Better Dropout Voltage
AMS1085-33	IRU1030-33	Better Dropout Voltage
AMS1086	IRU1015	Better Dropout Voltage
AMS1086-33	IRU1015-33	Better Dropout Voltage
AMS1117	IRU1117	Better Dropout Voltage
AMS1117-18	IRU1117-18	Better Dropout Voltage
AMS1117-25	IRU1117-25	Better Dropout Voltage
AMS1117-33	IRU1117-33	Better Dropout Voltage
AMS1503	IRU1150	Better Dropout Voltage
AMS1505	IRU1160	Better Dropout Voltage
AMS1508	IRU1175	
AMS1585	IRU1050	
AMS1585-33	IRU1050-33	
AMS1587	IRU1030	Better Dropout Voltage
AMS1587-33	IRU1030-33	Better Dropout Voltage

CHERRY / ON SEMICONDUCTOR

Part #	IR Cross	Comments
CS5201	IRU1010	
CS52015	IRU1015	Better Dropout Voltage
CS5203	IRU1030	
CS5203-33	IRU1030-33	
CS5203A	IRU1050	Better Dropout Voltage
CS5203A-33	IRU1050-33	
CS5204	IRU1050	Better Dropout Voltage
CS5204-33	IRU1050-33	Better Dropout Voltage
CS5205	IRU1050	
CS5206	IRU1075	Better Dropout Voltage
CS5207	IRU1075	
CS5207A	IRU1075	
CS5253	IRU1150	Better Dropout Voltage
CS5257A	IRU1175	

FAIRCHILD

Part #	IR Cross	Comments
RC1117	IRU1117	Better Dropout Voltage
RC1117-33	IRU1117-33	Better Dropout Voltage
RC1584	IRU1075	Better Dropout Voltage
RC1585	IRU1050	Better Dropout Voltage
RC1585-33	IRU1050-33	Better Dropout Voltage
RC1587	IRU1030	Better Dropout Voltage
RC1587-33	IRU1030-33	Better Dropout Voltage

LINEAR TECHNOLOGY

Part #	IR Cross	Comments
LT1083	IRU1075	
LT1084	IRU1050	Better dropout Voltage
LT1084-33	IRU1050-33	
LT1085	IRU1030	Better dropout Voltage
LT1085-33	IRU1030-33	
LT1086	IRU1015	Better dropout Voltage
LT1086-33	IRU1015-33	
LT1117	IRU1117	
LT1117-18	IRU1117-18	
LT1117-25	IRU1117-25	
LT1117-33	IRU1117-33	
LT1580	IRU1175	
LT1582	IRU1150	Better dropout Voltage
LT1584	IRU1075	
LT1585	IRU1050	Better dropout Voltage
LT1585-33	IRU1050-33	
LT1587	IRU1030	
LT1587-33	IRU1030-33	

Cross Reference by Manufacturer

LINFINITY MICRO ELECTRONICS

Part #	IR Cross	Comments
LX8117	IRU1117	Better Dropout Voltage
LX8117-25	IRU1117-25	Better Dropout Voltage
LX8117-33	IRU1117-33	Better Dropout Voltage
LX8117A	IRU1117	Better Dropout Voltage
LX8117A-25	IRU1117-25	Better Dropout Voltage
LX8117A-33	IRU1117-33	Better Dropout Voltage
LX8383	IRU1075	Better Dropout Voltage
LX8383A	IRU1075	
LX8384	IRU1050	Better Dropout Voltage
LX8384A	IRU1050	Better Dropout Voltage
LX8384-33	IRU1050-33	Better Dropout Voltage
LX8385	IRU1030	Better Dropout Voltage
LX8385A	IRU1030	Better Dropout Voltage
LX8385-33	IRU1030-33	
LX8386	IRU1015	Better Dropout Voltage
LX8386-33	IRU1015-33	
LX8415	IRU1010	
LX8415-25	IRU1010-25	
LX8415-33	IRU1010-33	
LX8580	IRU1175	Better Dropout Voltage
LX8584	IRU1075	Better Dropout Voltage
LX8585	IRU1050	Better Dropout Voltage
LX8585-33	IRU1050-33	
LX8586	IRU1075	Better Dropout Voltage
LX8586A	IRU1075	Better Dropout Voltage
LX8587	IRU1030	Better Dropout Voltage
LX8587A	IRU1030	Better Dropout Voltage
LX8587-33	IRU1030-33	
LX8610-25	IRU1206-25*	Better Dropout Voltage
LX8610-33	IRU1206-33*	Better Dropout Voltage

NATIONAL

Part #	IR Cross	Comments
LM1084	IRU1050	Better Dropout Voltage
LM1084-33	IRU1050-33	Better Dropout Voltage
LM1085	IRU1030	Better Dropout Voltage
LM1085-33	IRU1030-33	Better Dropout Voltage
LM1086	IRU1015	Better Dropout Voltage
LM1086-33	IRU1015-33	Better Dropout Voltage
LM1117	IRU1117	Better Dropout Voltage
LM1117-33	IRU1117-33	Better Dropout Voltage
LMS1585A	IRU1050	
LMS1587	IRU1030	Better Dropout Voltage
LMS8117	IRU1010	Better Dropout Voltage

MICREL

Part #	IR Cross	Comments
MIC39100-1.8	IRU1206-18	
MIC39100-2.5	IRU1206-25	
MIC39100-3.3	IRU1206-33	
MIC39101-1.8	IRU1207-18	
MIC39101-2.5	IRU1207-25	
MIC39101-3.3	IRU1207-33	
MIC39102	IRU1209	
MIC5205	IRU1205	

SEMTECH

Part #	IR Cross	Comments
EZ1083	IRU1075	
EZ1084	IRU1050	
EZ1084-33	IRU1050-33	
EZ1085	IRU1030	
EZ1085-33	IRU1030-33	
EZ1086	IRU1015	
EZ1086-33	IRU1015-33	Better Dropout Voltage
EZ1117	IRU1117	Better Dropout Voltage
EZ1117-25	IRU1117-25	Better Dropout Voltage
EZ1117-33	IRU1117-33	Better Dropout Voltage
EZ1580	IRU1175	
EZ1581	IRU1160	Better Dropout Voltage
EZ1582	IRU1150	Better Dropout Voltage
EZ1583	IRU1150	Better Dropout Voltage
EZ1584	IRU1075	
EZ1585	IRU1050	
EZ1585A	IRU1050	
EZ1585-33	IRU1050-33	
EZ1587	IRU1030	Better Dropout Voltage
EZ1587A	IRU1030	Better Dropout Voltage
EZ1587-33	IRU1030-33	Better Dropout Voltage
EZ1588	IRU1030	Better Dropout Voltage
SC1117	IRU1117	Better Dropout Voltage
SC1117-33	IRU1117-33	Better Dropout Voltage
SC1202	IRU1010	Better Dropout Voltage
SC1202-33	IRU1010-33	Better Dropout Voltage
SC431L	IRU431L	
SC5205	IRU1205	

ST

Part #	IR Cross	Comments
LD1117D	IRU1117	Better Dropout Voltage
LD1117D-33	IRU1117-33	Better Dropout Voltage
LF33CDT	IRU1206-33CD	Better Dropout Voltage

TEXAS INSTRUMENTS

Part #	IR Cross	Comments
TLV431A	IRU431L	

*Not drop-in, but pin compatible only with SOT-223 packages. Refer to the datasheet to determine the suitability of the replacement for the specific application.

Section 2: Linear Regulators

SINGLE LOW DROPOUT SELECTION GUIDE

	FEATURES					PACKAGES																	
Part #	Io (A)	Max Dropout (V)	Adj/ Fix (V)	SD Pin	Error Flag	TO-252 2-Pin D-Pak	MLPM 6-Pin 3x3	SOT-23 3-Pin	SOT-23 5-Pin	SOT-23 6-Pin	TO-263 3-Pin	TO-263 5-Pin	TO-263 7-Pin	2-Pin UThin-Pak	3-Pin UThin-Pak	5-Pin UThin-Pak	7-Pin UThin-Pak	8-Pin SOIC Pwr	TO-220 3-Pin	TO-220 5-Pin	TO-220 7-Pin	8-Pin Mini MSOP	SOT-223 3-Pin
						D	H	L3	L5	L6	M	M	M	P	P	P	P	S	T	T	T	U	Y
IRU1175	7.5	0.5	ADJ									X				X		X					
IRU1176	7.5	0.65	ADJ	X									X				X						
IRU1075	7.5	1	ADJ								X				X				X				
IRU1160	6	0.62	ADJ									X				X							
IRU1050-33	5	1.3	FIX 3.3			X					X			X					X				
IRU1050	5	1.3	ADJ			X					X			X					X				
IRU1150	4	0.7	ADJ									X				X		X					
IRU1030-33	3	1.3	FIX 3.3			X					X			X					X				
IRU1030	3	1.3	ADJ			X					X								X				
IRU1120*	2	1.25	ADJ													X							
IRU1015-33	1.5	1.3	FIX 3.3			X					X			X					X				
IRU1015	1.5	1.3	ADJ			X					X								X				
IRU1011-33*	1.3	1.3	FIX 3.3				X																
IRU1206-18	1	0.60	FIX 1.8			X																	X
IRU1207-18	1	0.60	FIX 1.8	X	X													X					
IRU1206-25	1	0.60	FIX 2.5			X																	X
IRU1207-25	1	0.60	FIX 2.5	X	X													X					
IRU1206-33	1	0.60	FIX 3.3			X																	X
IRU1207-33	1	0.60	FIX 3.3	X	X													X					
IRU1208	1	0.60	ADJ		X													X					
IRU1209	1	0.60	ADJ	X														X					

***Note:** Stable with ceramic capacitor.

SINGLE LOW DROPOUT SELECTION GUIDE CONTINUED

	FEATURES					PACKAGES																	
Part #	Io (A)	Max Dropout (V)	Adj/ Fix (V)	SD Pin	Error Flag	TO-252 2-Pin D-Pak	MLPM 6-Pin 3x3	SOT-23 3-Pin	SOT-23 5-Pin	SOT-23 6-Pin	TO-263 3-Pin	TO-263 5-Pin	TO-263 7-Pin	2-Pin UThin-Pak	3-Pin UThin-Pak	5-Pin UThin-Pak	7-Pin UThin-Pak	8-Pin SOIC Pwr	TO-220 3-Pin	TO-220 5-Pin	TO-220 7-Pin	8-Pin Mini MSOP	SOT-223 3-Pin
						D	H	L3	L5	L6	M	M	M	P	P	P	P	S	T	T	T	U	Y
IRU1010-18	1	1.3	FIX 1.8			X								X				X					X
IRU1010-25	1	1.3	FIX 2.5			X								X				X					X
IRU1010-33	1	1.3	FIX 3.3			X								X				X					X
IRU1010	1	1.3	ADJ			X								X				X					X
IRU1117-18	0.8	1.2	FIX 1.8			X								X				X					X
IRU1117-25	0.8	1.2	FIX 2.5			X								X				X					X
IRU1117-33	0.8	1.2	FIX 3.3			X								X				X					X
IRU1117	0.8	1.2	ADJ			X								X				X					X
IRU1205-18*	0.3	0.40	FIX 1.8						X														
IRU1205-25*	0.3	0.40	FIX 2.5						X														
IRU1205-28*	0.3	0.40	FIX 2.8						X														
IRU1205-30*	0.3	0.40	FIX 3.0						X														
IRU1205-33*	0.3	0.40	FIX 3.3						X														
IRU1205-36*	0.3	0.40	FIX 3.6						X														
IRU1205*	0.3	0.40	ADJ						X														

***Note:** Stable with ceramic capacitor.

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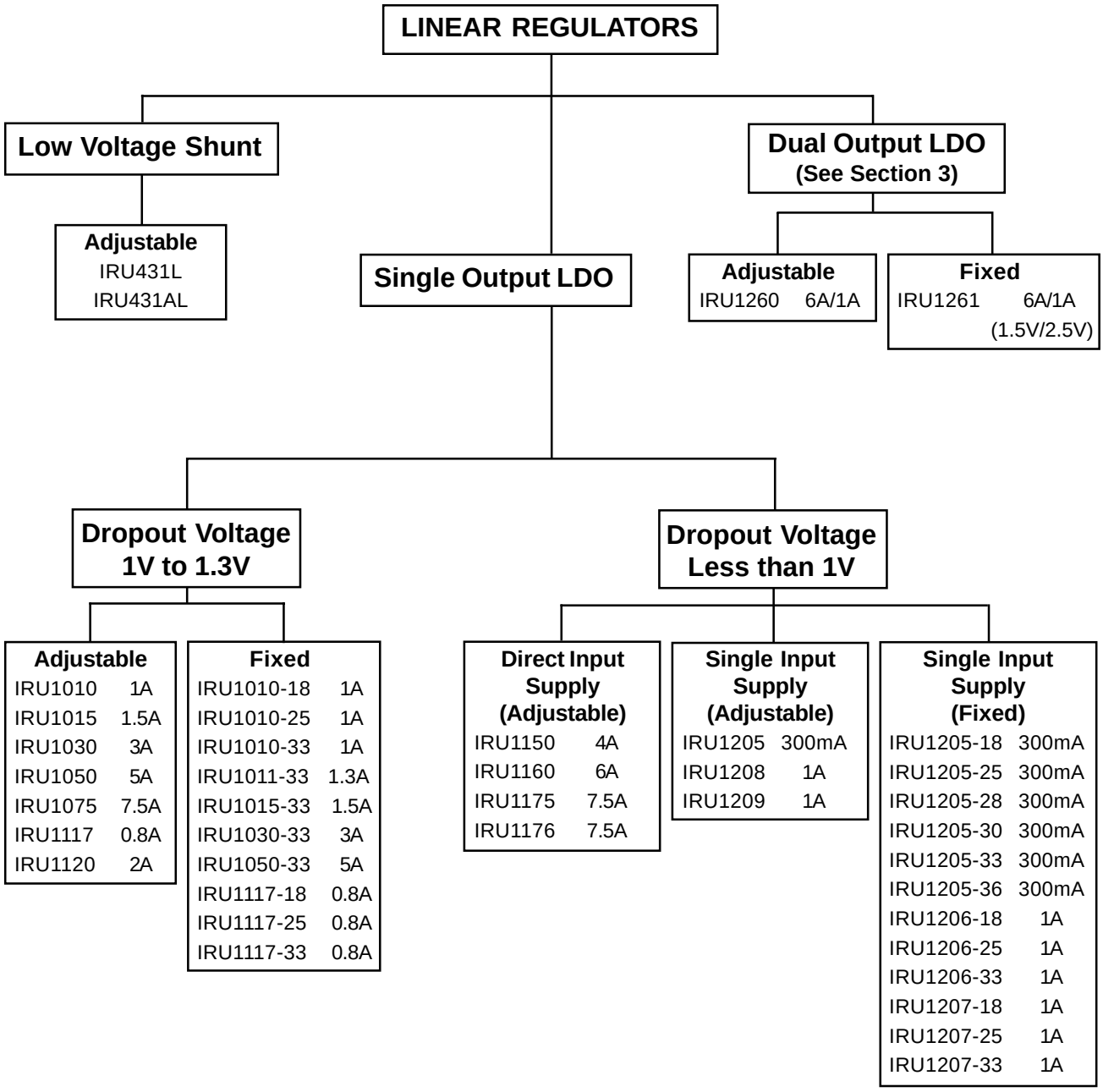
Selection Tree



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IRU431L / IRU431AL

LOW -VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATOR

FEATURES

- SOT-23 Packages
- Voltage Reference Initial Accuracy (1% for IRU431L and 0.5% for IRU431AL)
- Low Operating Cathode Current (80μA max)
- Unconditionally Stable with only 1μF
- Adjustable Output from 1.24V to 15V
- 0.25Ω Typical Output Impedance
- Pin to Pin Compatible with TLV431

APPLICATIONS

- Precision Voltage Reference
- Linear Regulator Controller
- Secondary Side Controller for the low voltage power supply applications

DESCRIPTION

The IRU431L family are three-terminal adjustable shunt regulators that can also be used as precision voltage references. Its output voltage may be set to any value between V_{REF}(1.24V) and 15V with two external resistors as shown in the typical application circuit. Other applications of this device include being used as a merged amplifier and reference in applications such as a linear regulator or as the secondary side controller in low voltage power supply applications. The IRU431L only requires 80μA maximum quiescent current before regulating, making it ideal as a voltage reference for battery type applications. The IRU431L has ±1% initial accuracy while IRU431AL provides ±0.5% initial accuracy.

TYPICAL APPLICATION

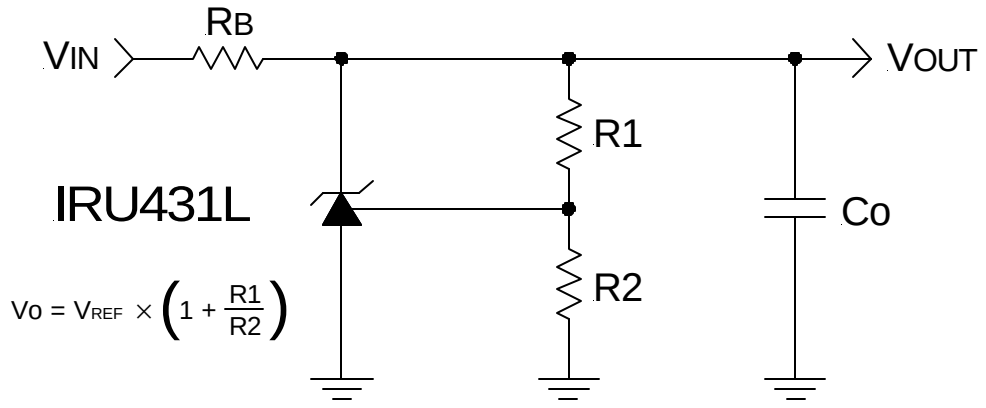


Figure 1 - Typical application of the IRU431L as a shunt regulator / voltage reference.

PACKAGE ORDER INFORMATION

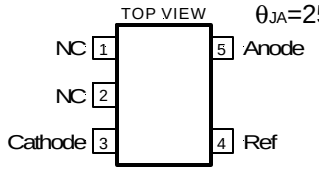
T_A (°C)	5-PIN SOT-23 (L5)	3-PIN SOT-23 (L3)
0 To 70	IRU431LCL5	IRU431LCL3
0 To 70	IRU431ALCL5	IRU431ALCL3

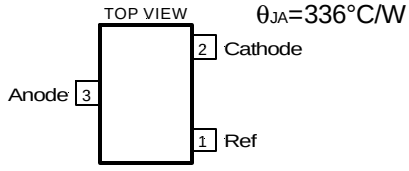
ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 15V
Continuous Cathode Current Range ..... -15mA to +15mA
Reference Current Range ..... -0.05mA to 1mA
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature Range ..... 0°C to 150°C

PACKAGE INFORMATION

5-PIN SOT-23 (L5)	3-PIN SOT-23 (L3)
TOP VIEW θ_{JA}=256°C/W	TOP VIEW θ_{JA}=336°C/W





ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over T_A=0 to 70°C, Co=1µF. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	I_K=10mA, $V_{KA}=V_{REF}$, T_A=25°C	1.228	1.240	1.252	V
IRU431L		I_K=10mA, $V_{KA}=V_{REF}$	1.221	1.240	1.259	
Reference Voltage	V_{REF}	I_K=10mA, $V_{KA}=V_{REF}$, T_A=25°C	1.234	1.240	1.246	V
IRU431AL		I_K=10mA, $V_{KA}=V_{REF}$	1.228	1.240	1.252	
V_{REF} Deviation over full temperature range	$V_{REF(DEV)}$	$V_{KA}=V_{REF}$, I_K=10mA Note 1		6		mV
Ratio of V_{REF} change to cathode voltage change	$\Delta V_{REF}/\Delta V_{KA}$	I_K=10mA, $\Delta V_{KA}=V_{REF}$ to 6V		-1	-6	mV/V
Reference Pin Current		I_K=10mA, R1=10KΩ, R2=open		0.15	1	µA
I_{REF} Deviation over full temperature range	$I_{REF(DEV)}$	I_K=10mA, R1=10KΩ, R2=open Note 1		0.05		µA
Minimum Cathode Current	$I_{K(MIN)}$	$V_{KA}=V_{REF}$		55	80	µA
Off State Cathode Current	Ioff	V_{KA}=6V, V_{REF}=0V		0.6	0.75	µA
		V_{KA}=10V, V_{REF}=0V		1.8	5	
		V_{KA}=15V, V_{REF}=0V		3.2	10	
Dynamic Impedance	Z_{KA0}	$V_{KA}=V_{REF}$, f<1KHz, I_K=0.1 to 15mA, Note 2		0.25	0.4	Ω

Note 1: The deviation parameters, $V_{REF(DEV)}$ and $I_{REF(DEV)}$ are defined as the differences between the maximum and the minimum values obtained over the rated temperature range. The average full range temperature coefficient of the reference input voltage is defined as:

$$|\alpha V_{REF}| = \frac{\left(\frac{V_{REF(DEV)}}{V_{REF(25°C)}}\right) \times 10^6}{\Delta T_A}$$

Where:
$|\alpha V_{REF}|$ unit is ppm/°C
ΔT_A is the rated operating free air temperature of the device.
αV_{REF} can be positive or negative depending on whether minimum V_{REF} or maximum V_{REF} respectively occurs at the lower temperature.

Note 2: The dynamic impedance when $V_{KA}=V_{REF}$ is defined as:

$$|Z_{KA0}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operating with two external resistors (See Figure 3), the total dynamic impedance of the circuit is given by:

$$|Z_{KA}| = \frac{\Delta V}{\Delta I} = |Z_{KA0}| \times \left(1 + \frac{R1}{R2}\right)$$

PIN DESCRIPTIONS

5-PIN	3-PIN	PIN SYMBOL	PIN DESCRIPTION
4	1	Ref	Resistors from the Ref pin to the Cathode pin and to ground form a divider that sets the output voltage.
3	2	Cathode	The output of the shunt regulator. A capacitor of 1μF minimum value must be connected from this pin to Anode pin to insure unconditional stability.
5	3	Anode	Ground pin. This pin must be connected to the lowest potential in the system and all other pins must be at higher potential with respect to this pin.
1, 2	NA	NC	These pins are not connected internally.

BLOCK DIAGRAM

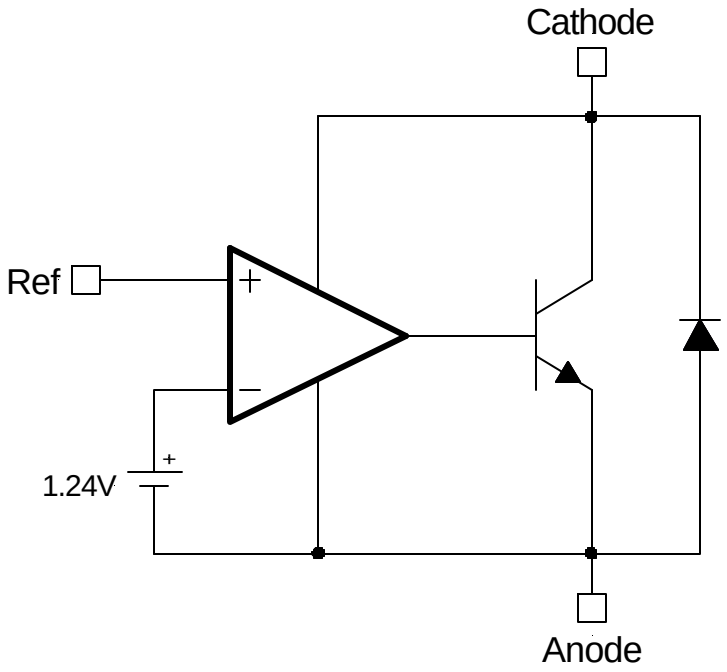


Figure 2 - Simplified block diagram of the IRU431L.

APPLICATION INFORMATION

Output Voltage Setting

The IRU431L can be programmed to any voltages in the range of 1.24 to 15V with the addition of R1 and R2 external resistors according to the following formula:

$$Vo = V_{KA} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) + I_{REF} \times R1$$

The IRU431L keeps a constant voltage of 1.240V between the Ref pin and Ground pin. By placing a resistor R2 across these two pins a constant current flows through R2, adding to the I_{REF} current and into the R1 resistor producing a voltage equal to:

$$\left(\frac{1.240}{R2}\right) \times R1 + I_{REF} \times R1$$

which will be added to the 1.240V to set the output voltage as shown in the above equation. Since the input bias current of the Ref pin is 0.5µA max, it adds a very small error to the output voltage and for most applications can be ignored. For example, in a typical 5V to 3.3V application where R2=1.21KΩ and R1=2KΩ the error due to the I_{ADJ} is only 1mV which is about 0.03% of the nominal set point.

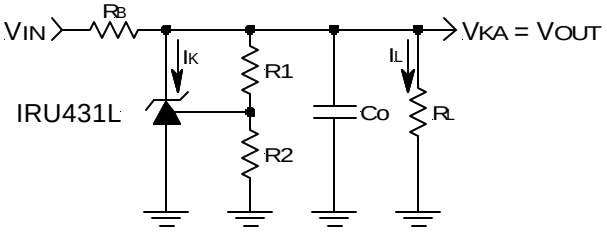


Figure 3 - Typical application of the IRU431L for programming the output voltage.

Biasing Resistor (R_B) Selection

The biasing resistor R_B is selected such that it does not limit the input current under the minimum input supply and maximum load and biasing current.

An example is given below on how to properly select the biasing resistor.

Assuming:

V_{MIN} = 4.5V
V_{MAX} = 6V
V_{KA} = 3.3V
I_L = 10mA

The maximum value for the biasing resistor is calculated using the following equations:

$$R_{B(MAX)} = \frac{V_{MIN} - V_{KA}}{I_{B(MAX)} + I_{L(MAX)}}$$

$$I_{B(MAX)} = I_{K(MIN)} + I_R$$

Where:

V_{MIN} = Minimum supply voltage
$I_{L(MAX)}$ = Maximum load current
$I_{B(MAX)}$ = Maximum bias current
$I_{K(MIN)}$ = Maximum value for the minimum cathode current spec
I_R = Current through R1

Assuming R1 = 2KΩ as before,

$$I_R = \frac{3.3 - 1.24}{2} = 1.03mA$$

$$I_{B(MAX)} = 0.08 + 1.03 = 1.11mA$$

$$R_{B(MAX)} = \frac{4.5 - 3.3}{1.11 + 10} = 108\Omega$$

Select R_B = 100Ω

The maximum power dissipation of the resistor is calculated under the maximum supply voltage as follows:

$$P_{R_B(MAX)} = \frac{(V_{MAX} - V_{KA})^2}{R_B}$$

Where:

V_{MAX} = Maximum supply voltage
$P_{R_B(MAX)}$ = Maximum R_B power dissipation

$$P_{R_B(MAX)} = \frac{(6 - 3.3)^2}{100} = 73mW$$

Thermal Design

The IRU431L is offered in the surface mount SOT-23 (L) packages. The SOT-23 package has the maximum power dissipation capability of 150mW at T_A=25°C with the derating factor of -1.2mW / °C.

The table below summarizes the maximum power dissipation capability of each package versus ambient temperature.

	Ambient Temperature (T_A) °C				
Pkg	**25**	**40**	**50**	**60**	**70**
SOT-23	150mW	132mW	120mW	108mW	96mW

In our previous example, the maximum power dissipation of the device is calculated under no load and maximum input supply condition.

The maximum power is calculated using the following equation:

$$P_{MAX} = V_{KA} \times \left(\frac{V_{MAX} - V_{KA}}{R_B}\right)$$

Where:
P_{MAX} = Maximum power dissipation of the 431L

For our example:

$$P_{MAX} = 3.3 \times \left(\frac{6 - 3.3}{100}\right) = 89mW$$

As shown in the power dissipation table, both packages can handle this power dissipation.

Stability

The IRU431L has many different domains of stability as a function of the cathode current. As is typical of three-terminal shunt regulators, the IRU431L has many domains of stability. The actual domain in which any practical circuit operates is related to cathode current. In general the device will be unconditionally stable for any cathode current if a capacitor, 1μF or larger, is connected between the cathode and the anode. If the cathode current is always higher than 3mA under minimum line and maximum load conditions, the capacitor value can be reduced to 0.01μF and the system will be stable.

TYPICAL APPLICATION

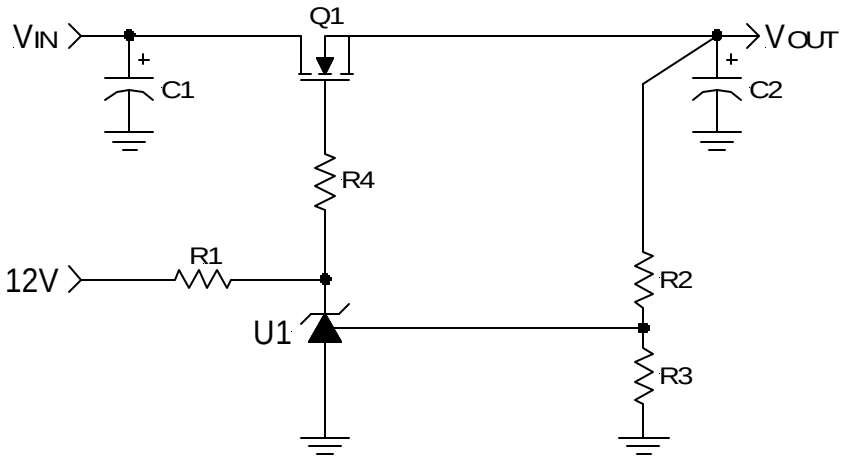


Figure 4 - Low cost 3.3V to 2.7V output.

Ref Desig	Description	Qty	Part #	Manuf
U1	Shunt Regulator	1	IRU431L	IR
C1, C2	Capacitor	2	Elect, 220μF, 6.3V, ECAOJFQ221	Panasonic
R1	Resistor	1	6.2KΩ, 5%, SMT	
R2	Resistor	1	118Ω, 1%, SMT	
R3, R4	Resistor	2	100Ω, 1%, SMT	
HS1	Heat Sink		Use minimum of 1" square copper pad area for load current <4A	

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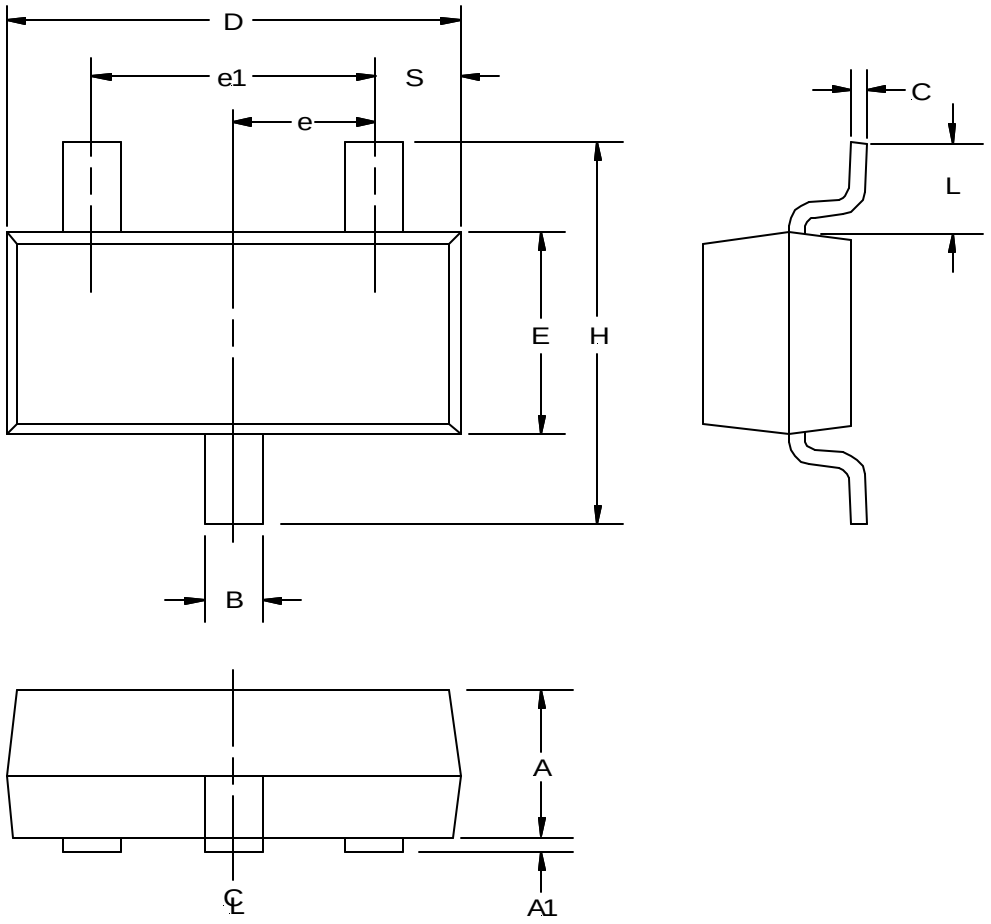
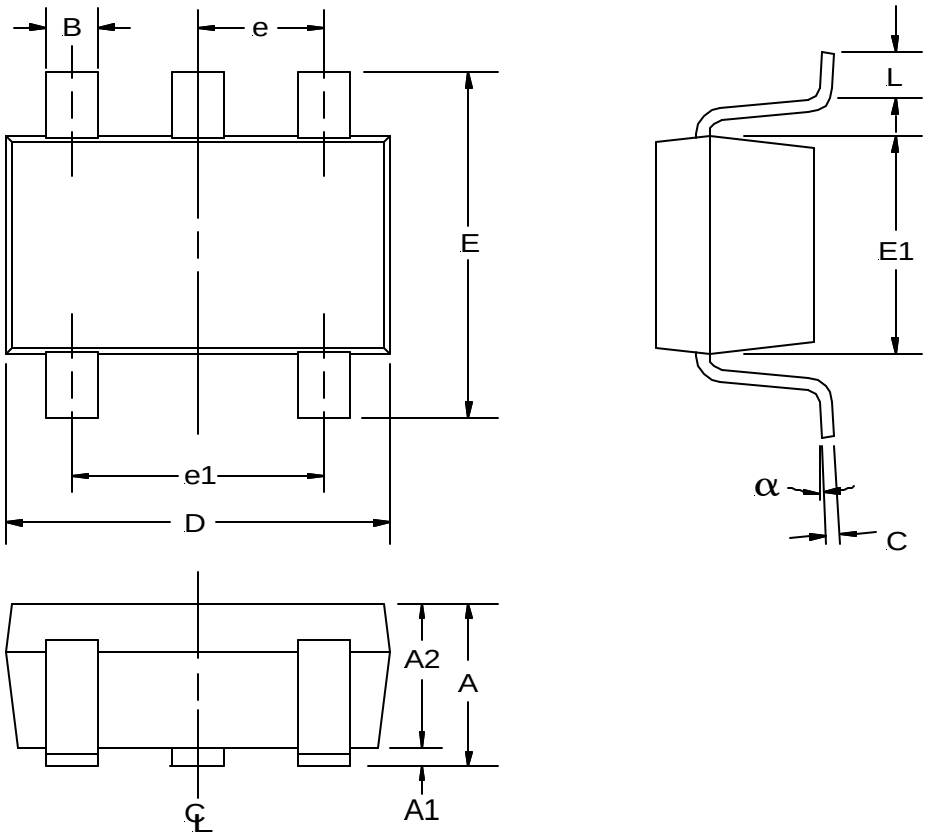
(L3) SOT-23 Package
3-Pin



SYMBOL	MIN	MAX
A	0.890	1.120
A1	0.013	0.100
B	0.370	0.510
C	0.085	0.180
D	2.800	3.040
E	1.200	1.400
e	0.890	1.030
e1	1.780	2.050
H	2.100	2.640
L	0.55 REF	
S	0.450	0.600

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(L5) SOT-23 Package
5-Pin

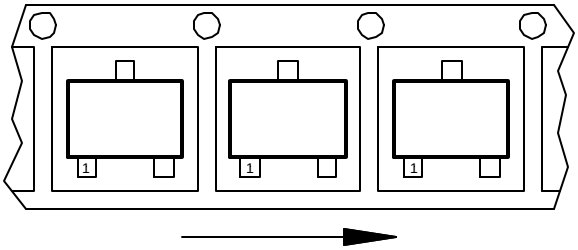


SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.25	0.50
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
e	0.95 REF	
e1	1.90 REF	
L	0.35	0.55
α	0°	10°

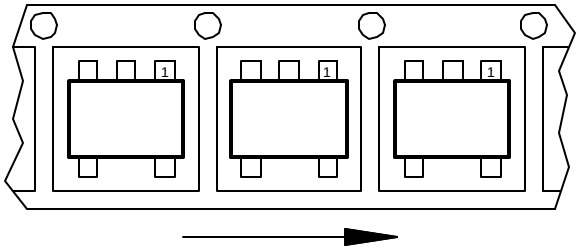
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
L3	SOT-23	3	---	3000	Fig A
L5	SOT-23	5	---	3000	Fig B



Feed Direction
Figure A



Feed Direction
Figure B

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IRU1010

1A LOW DROPOUT POSITIVE ADJUSTABLE REGULATOR

FEATURES

- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown
- Available in SOT-223, D-Pak, Ultra Thin-Pak™ and 8-Pin SOIC Surface-Mount Packages

APPLICATIONS

- VGA & Sound Card Applications
- Low Voltage High Speed Termination Applications
- Standard 3.3V Chip Set and Logic Applications

DESCRIPTION

The IRU1010 is a low dropout, three-terminal adjustable regulator with minimum of 1A output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications such as high speed bus termination and low current 3.3V logic supply. The IRU1010 is also well suited for other applications such as VGA and sound cards. The IRU1010 is guaranteed to have <1.3V dropout at full load current making it ideal to provide well regulated outputs of 2.5V to 3.6V with 4.75V to 7V input supply.

TYPICAL APPLICATION

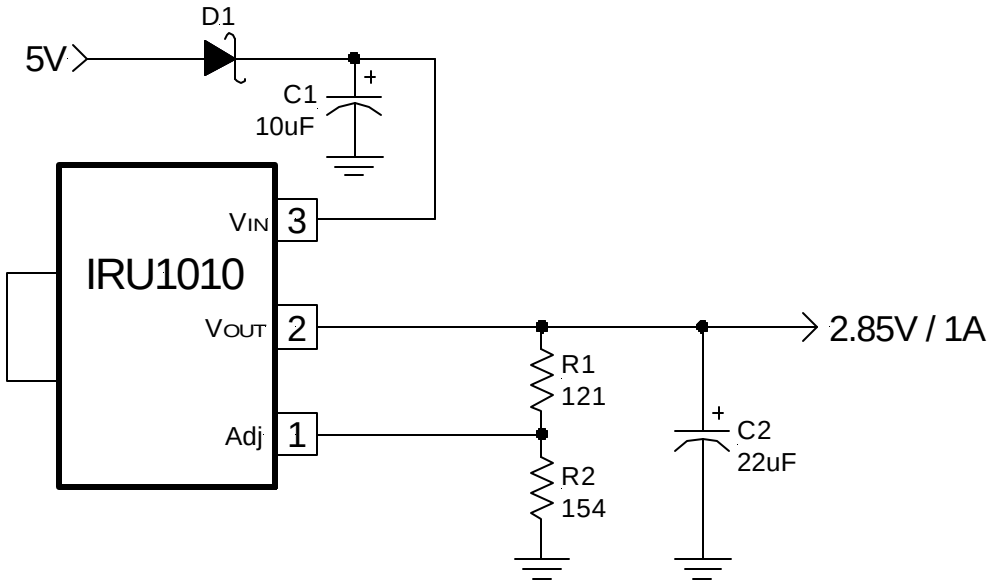


Figure 1 - Typical application of IRU1010 in a 5V to 2.85V SCSI termination regulator.

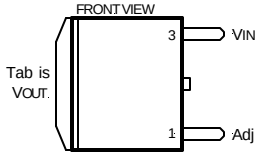
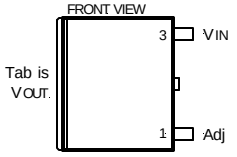
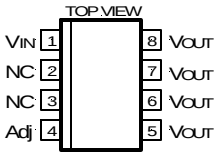
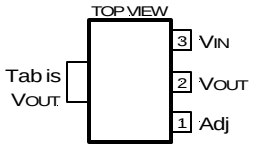
PACKAGE ORDER INFORMATION

T_J (°C)	2-PIN PLASTIC TO-252 (D-Pak)	2-PIN PLASTIC Ultra Thin-Pak™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SOT-223 (Y)
0 To 150	IRU1010CD	IRU1010CP	IRU1010CS	IRU1010CY

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN})	7V
Power Dissipation	Internally Limited
Storage Temperature Range	-65°C To 150°C
Operating Junction Temperature Range	0°C To 150°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)	2-PIN ULTRA THIN-PAK™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SO-223 (Y)
			
θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=55°C/W for 1" Sq pad	θ_{JA}=90°C/W for 0.4" Sq pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=10µF, and T_J=0 to 150°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	Io=10mA, T_J=25°C, (V_{IN}-Vo)=1.5V	1.238	1.250	1.262	V
		Io=10mA, (V_{IN}-Vo)=1.5V	1.225	1.250	1.275	
Line Regulation		Io=10mA, 1.3V<(V_{IN}-Vo)<7V			0.2	%
Load Regulation (Note 1)		V_{IN}=3.3V, V_{ADJ}=0, 10mA<Io<1A			0.4	%
Dropout Voltage (Note 2)	ΔVo	Note 2 , Io=1A		1.1	1.3	V
Current Limit		V_{IN}=3.3V, ΔVo=100mV	1.1			A
Minimum Load Current (Note 3)		V_{IN}=3.3V, V_{ADJ}=0V		5	10	mA
Thermal Regulation		30ms Pulse, V_{IN}-Vo=3V, Io=1A		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum,				
		Io=0.5A, V_{IN}-Vo=3V	60	70		dB
Adjust Pin Current	I_{ADJ}	Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C,				
		Io=10mA, V_{IN}-Vo=1.5V		55	120	µA
Adjust Pin Current Change		Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C		0.2	5	µA
Temperature Stability		V_{IN}=3.3V, V_{ADJ}=0V, Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%Vo

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically, the resistor dividers are selected such that it automatically maintains this current.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	Adj	A resistor divider from this pin to the V_{OUT} pin and ground sets the output voltage.
2	V_{OUT}	The output of the regulator. A minimum of 10µF capacitor must be connected from this pin to ground to insure stability.
3	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum dropout voltage during the load transient response. This pin must always be 1.3V higher than V_{OUT} in order for the device to regulate properly.

BLOCK DIAGRAM

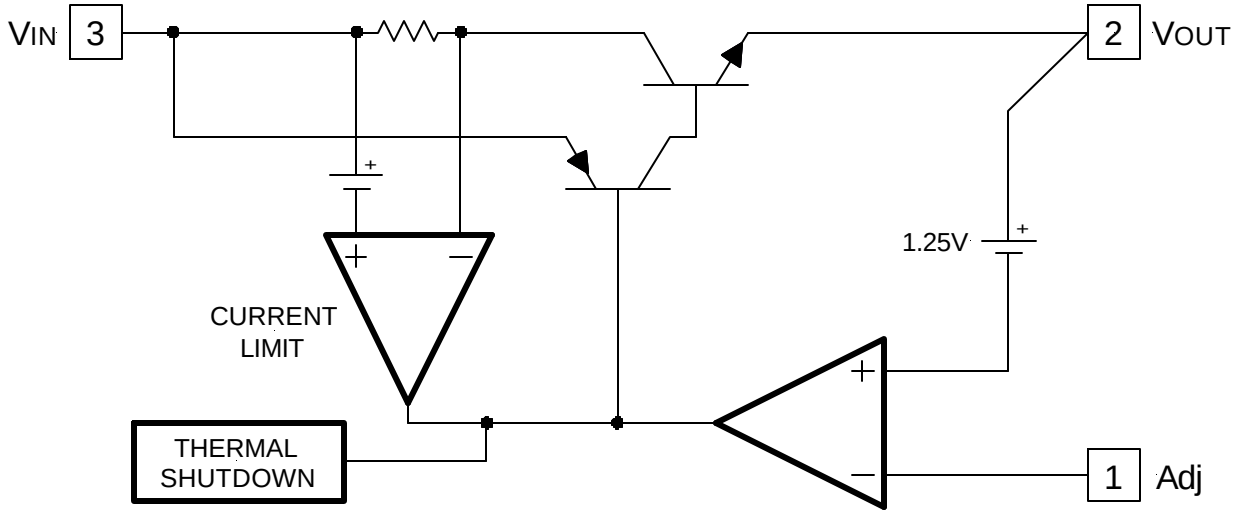


Figure 2 - Simplified block diagram of the IRU1010.

APPLICATION INFORMATION

Introduction

The IRU1010 adjustable Low Dropout (LDO) regulator is a three-terminal device which can easily be programmed with the addition of two external resistors to any voltages within the range of 1.25 to 5.5V. This regulator, unlike the first generation of the three-terminal regulators such as LM117 that required 3V differential between the input and the regulated output, only needs 1.3V differential to maintain output regulation. This is a key requirement for today's low voltage IC applications that typically need 3.3V supply and are often generated from the 5V supply. Other applications such as high speed memory termination need to switch the load current from zero to full load in tens of nanoseconds at their pins, which translates to an approximately 300 to 500ns current step at the regulator. In addition, the output voltage tolerances are sometimes tight and they include the transient response as part of the specification.

The IRU1010 is specifically designed to meet the fast current transient needs as well as providing an accurate initial voltage, reducing the overall system cost with the need for fewer output capacitors.

Output Voltage Setting

The IRU1010 can be programmed to any voltages in the range of 1.25V to 5.5V with the addition of R1 and R2 external resistors according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) + I_{ADJ} \times R2$$

Where:

V_{REF} = 1.25V Typically

I_{ADJ} = 50μA Typically

R1 and R2 as shown in Figure 3:

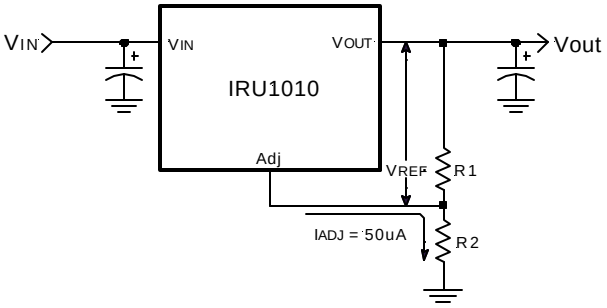


Figure 3 - Typical application of the IRU1010 for programming the output voltage.

The IRU1010 keeps a constant 1.25V between the output pin and the adjust pin. By placing a resistor R1 across these two pins a constant current flows through R1, adding to the I_{ADJ} current and into the R2 resistor producing a voltage equal to the (1.25/R1) × R2+I_{ADJ} × R2 which will be added to the 1.25V to set the output voltage. This is summarized in the above equation. Since the minimum load current requirement of the IRU1010 is 10mA, R1 is typically selected to be 121Ω resistor so that it automatically satisfies the minimum current requirement. Notice that since I_{ADJ} is typically in the range of 50μA it only adds a small error to the output voltage and should only be considered when a very precise output voltage setting is required. For example, in a typical 3.3V application where R1=121Ω and R2=200Ω the error due to I_{ADJ} is only 0.3% of the nominal set point.

Load Regulation

Since the IRU1010 is only a three-terminal device, it is not possible to provide true remote sensing of the output voltage at the load. Figure 4 shows that the best load regulation is achieved when the bottom side of R2 is connected to the load and the top side of R1 resistor is connected directly to the case or the V_{OUT} pin of the regulator and not to the load. In fact, if R1 is connected to the load side, the effective resistance between the regulator and the load is gained up by the factor of (1+ R2/R1), or the effective resistance will be $R_{P(eff)}=R_P \times (1+ R2/R1)$. It is important to note that for high current applications, this can represent a significant percentage of the overall load regulation and one must keep the path from the regulator to the load as short as possible to minimize this effect.

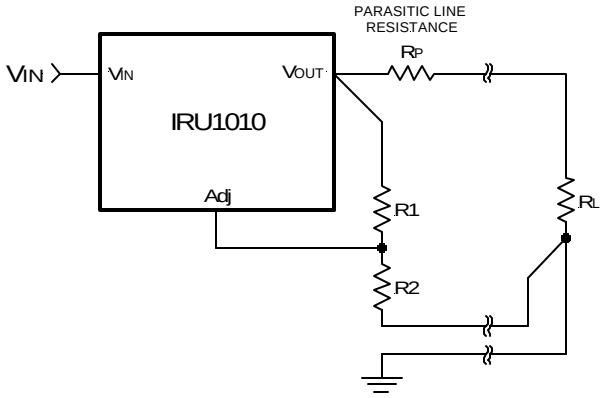


Figure 4 - Schematic showing connection for best load regulation.

Stability

The IRU1010 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for microprocessor applications use standard electrolytic capacitors with a typical ESR in the range of 50 to 100mΩ and an output capacitance of 500 to 1000μF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1010 takes advantage of this phenomena in making the overall regulator loop stable. For most applications a minimum of 100μF aluminum electrolytic capacitor such as Sanyo MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response.

Thermal Design

The IRU1010 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the maximum allowable junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. The next example for a SCSI terminator application shows the steps in sellecting the proper regulator in a surface-mount package. (See IRU1015 for non-surface-mount packages)

Assuming the following specifications:

V_{IN} = 5V
V_F = 0.5V
V_{OUT} = 2.85V
$I_{OUT(MAX)}$ = 0.8A
T_A = 35°C

Where: V_F is the forward voltage drop of the D1 diode as shown in Figure 5.

The steps for selecting the right package with proper board area for heatsinking to keep the junction temperature below 135°C is given as:

1) Calculate the maximum power dissipation using:

$P_D = I_{OUT} \times (V_{IN} - V_F - V_{OUT})$

$P_D = 0.8 \times (5 - 0.5 - 2.85) = 1.32W$

2) Calculate the maximum θ_{JA} allowed for our example:

$$\theta_{JA(MAX)} = \frac{T_J - T_A}{P_D} = \frac{135 - 35}{1.32} = 75.6°C/W$$

3) Select a package from the datasheet with lower θ_{JA} than the one calculated in the previous step.

Selecting TO-252 (D-Pak) with at least 0.5" square of 0.062" FR4 board using 1 oz. copper has 70°C/W which is lower than the calculated number.

To set the output DC voltage, we need to select R1 and R2:

4) Assuming R1 = 121Ω, 1%:

$$R_2 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_1 = \left(\frac{2.85}{1.25} - 1\right) \times 121 = 154.8\Omega$$

Select R2 = 154Ω, 1%.

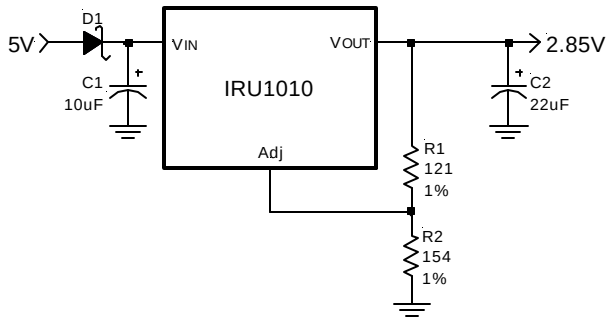


Figure 5 - Final Schematic for half of the GTL+ termination regulator.

Layout Consideration

The output capacitors must be located as close to the V_{OUT} terminal of the device as possible. It is recommended to use a section of a layer of the PC board as a plane to connect the V_{OUT} pin to the output capacitors to prevent any high frequency oscillation that may result due to excessive trace inductance.

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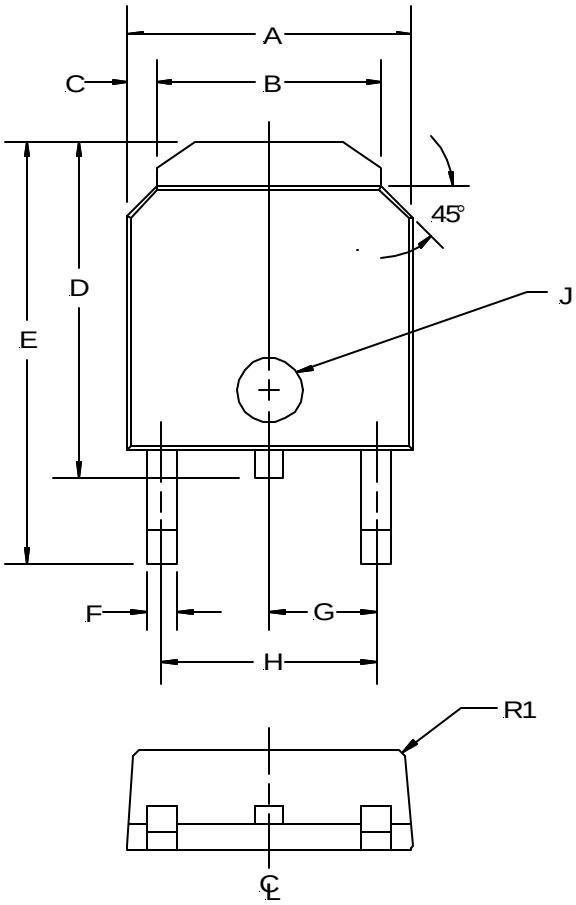
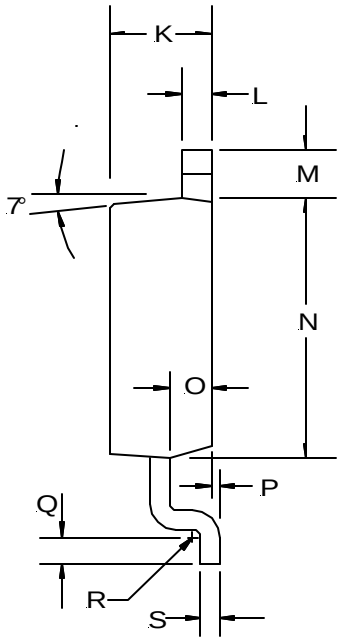
(D) TO-252 Package
2-Pin

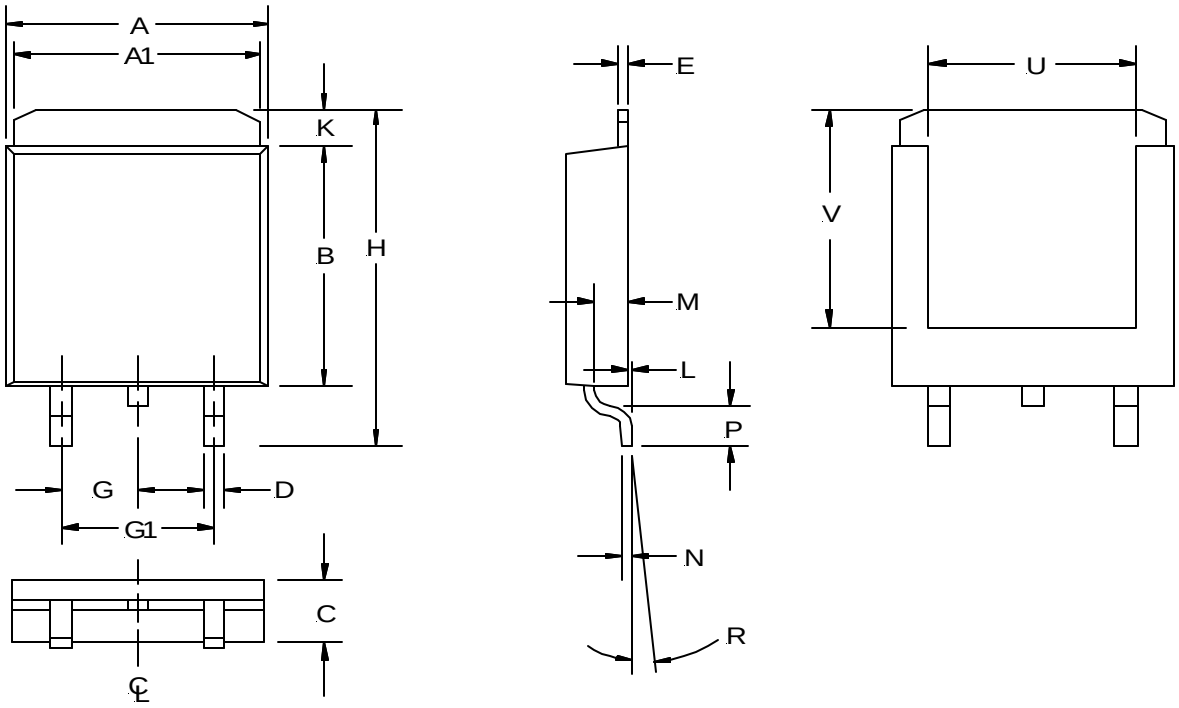




SYMBOL	MIN	MAX
A	6.477	6.731
B	5.004	5.207
C	0.686	0.838
D	7.417	8.179
E	9.703	10.084
F	0.635	0.889
G	2.286 BSC	
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

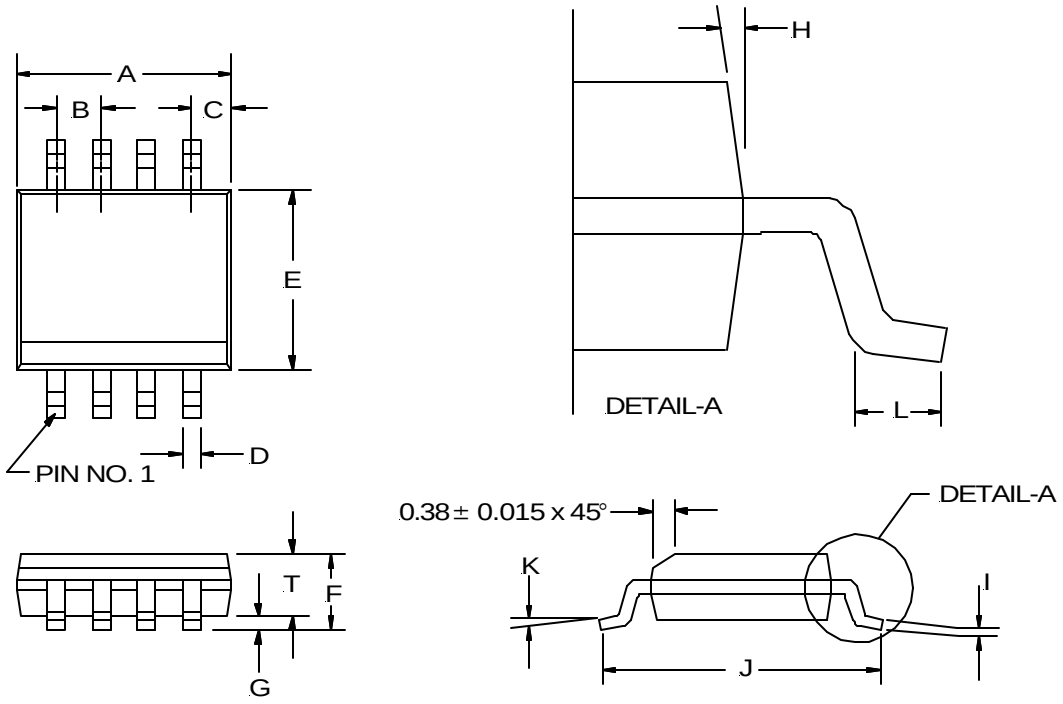
(P) Ultra Thin-Pak™
2-Pin



SYMBOL	MIN	MAX
A	5.91	6.17
A1	5.54	5.79
B	6.02	6.27
C	1.70	2.03
D	0.63	0.79
E	0.17	0.33
G	2.16	2.41
G1	4.45	4.70
H	9.42	9.68
K	0.76	1.27
L	0.02	0.13
M	0.89	1.14
N	0.25	0.25
P	0.94	1.19
R	2°	6°
U	2.92	3.30
V	5.08 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

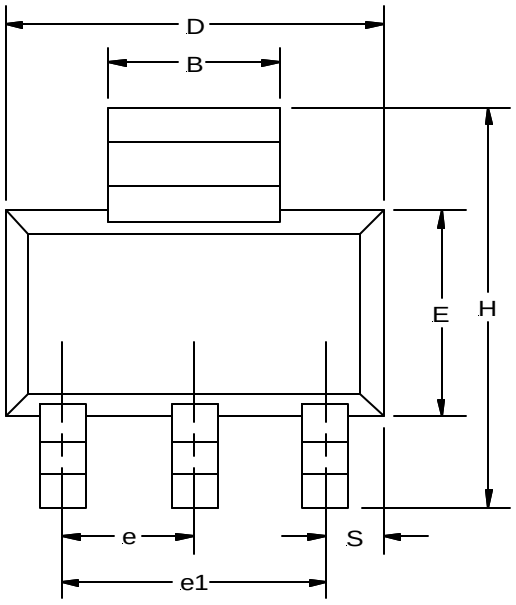
(S) SOIC Package
8-Pin Surface Mount, Narrow Body



8-PIN		
SYMBOL	**MIN**	**MAX**
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

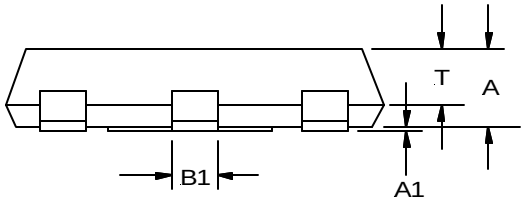
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

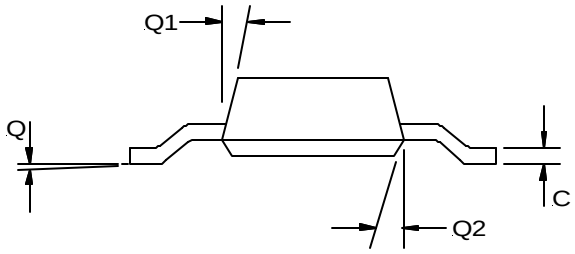
(Y) SOT-223 Package
3-Pin



SYMBOL	MIN	MAX
A	1.498	1.702
A1	0.02	0.11
B	2.895	3.15
B1	0.637	0.85
C	0.239	0.381
D	6.299	6.706
E	3.30	3.708
e	2.209	2.953
e1	4.496	4.699
H	6.70	7.30
Q	0°	10°
Q1	7°	16°
Q2	7°	16°
S	0.838	1.05
T	1.092	1.30

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.





PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
P	Ultra Thin-Pak™	2	75	2500	Fig B
S	SOIC, Narrow Body	8	95	2500	Fig C
Y	SOT-223	3	80	2500	Fig D

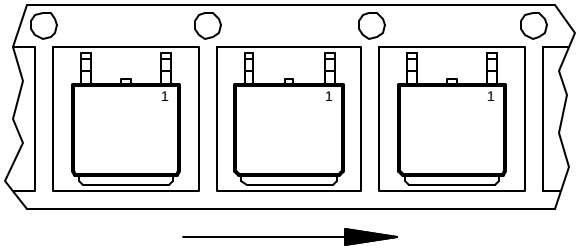


Figure A

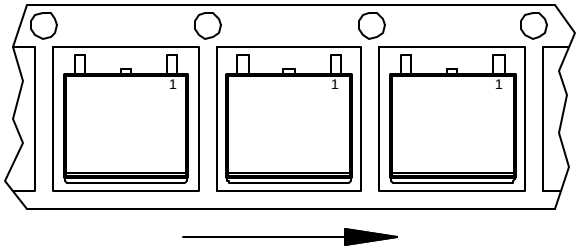


Figure B

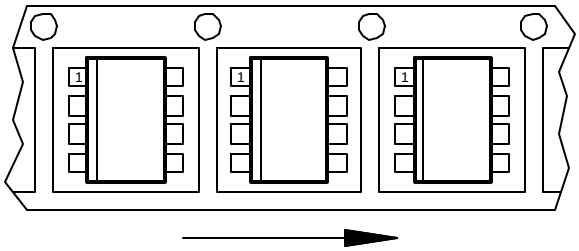


Figure C

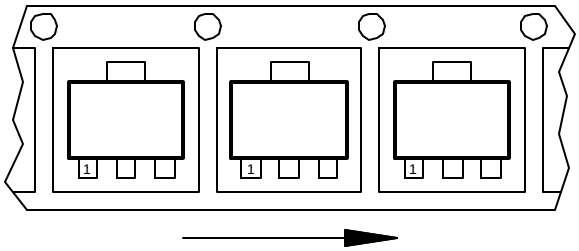


Figure D

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IRU1010-18

1A LOW DROPOUT POSITIVE FIXED 1.8V REGULATOR

FEATURES

- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown
- Available in SOT-223, D-Pak, Ultra Thin-Pak™ and 8-Pin SOIC Surface-Mount Packages

APPLICATIONS

- Low Voltage IC Supply Applications
- DSP Core Voltage

DESCRIPTION

The IRU1010-18 is a low dropout three-terminal fixed output regulator with minimum of 1A output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications as well as generating clock supply for PC applications. The IRU1010-18 is guaranteed to have <1.3V dropout at full load current making it ideal to provide well regulated with 3.8V input supply. The IRU1010-18 is specifically designed to be stable with low cost aluminum capacitors while maintaining stability with low ESR tantalum caps.

TYPICAL APPLICATION

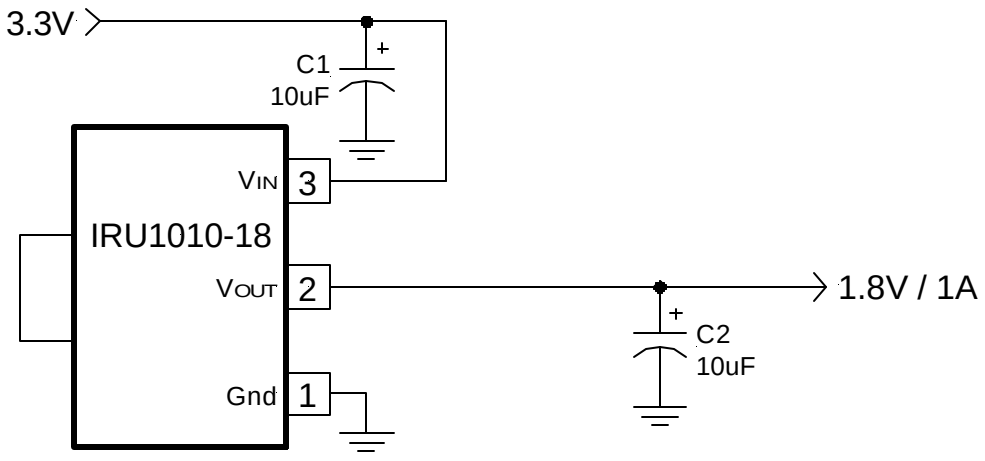


Figure 1 - Typical set-up of the IRU1010-18 in a 3.3V to 1.8V regulator application.

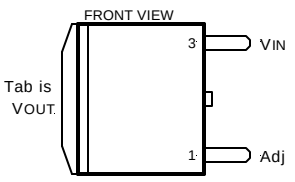
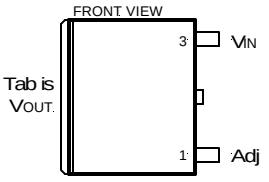
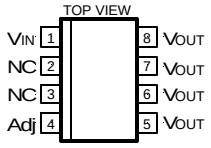
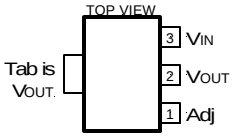
PACKAGE ORDER INFORMATION

T_J (°C)	2-PIN PLASTIC TO-252 (D-Pak)	2-PIN PLASTIC Ultra Thin-Pak™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SOT-223 (Y)
0 To 125	IRU1010-18CD	IRU1010-18CP	IRU1010-18CS	IRU1010-18CY

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)	2-PIN ULTRA THIN-PAK™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SO-223 (Y)
			
θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=55°C/W for 1" Sq pad	θ_{JA}=90°C/W for 0.4" Sq pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, V_{IN}=5V, C_{OUT}=10µF and T_J=0 to 125°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	Vo	Io=10mA, T_J=25°C	1.782	1.800	1.818	V
		Io=10mA	1.764	1.800	1.836	
Line Regulation		Io=10mA, 4.75V<V_{IN}<7V			7	mV
Load Regulation (Note 1)		10mA<Io<1A			17	mV
Dropout Voltage (Note 2)		Io=1A			1.3	V
Current Limit		ΔVo=100mV	1.1			A
Thermal Regulation		30ms Pulse, Io=1A		0.01		%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum, Io=0.5A		70		dB
Temperature Stability		Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3		%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%Vo

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Gnd	Ground pin. This pin must be connected to ground plane using a low inductance short connection.
2	V_{OUT}	The output of the regulator. This pin is also connected to the tab of the package. An output capacitor must be connected to this pin to insure stability of the regulator.
3	V_{IN}	Input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum dropout voltage during the load transient response. This pin must always be 1.3V higher than V_{OUT} in order for the device to regulate properly.

BLOCK DIAGRAM

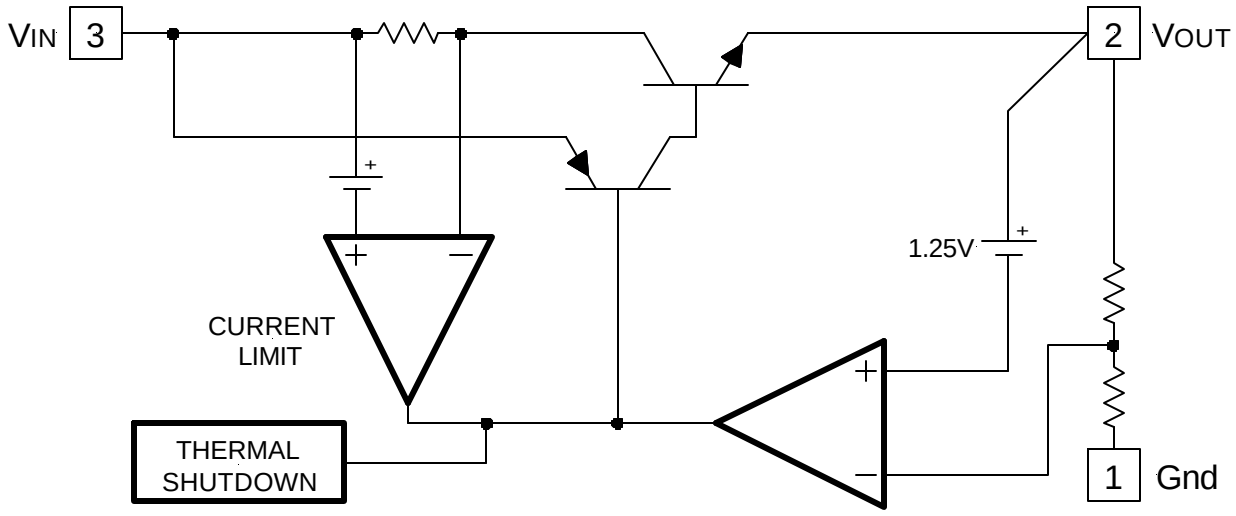


Figure 2 - Simplified block diagram of the IRU1010-18.

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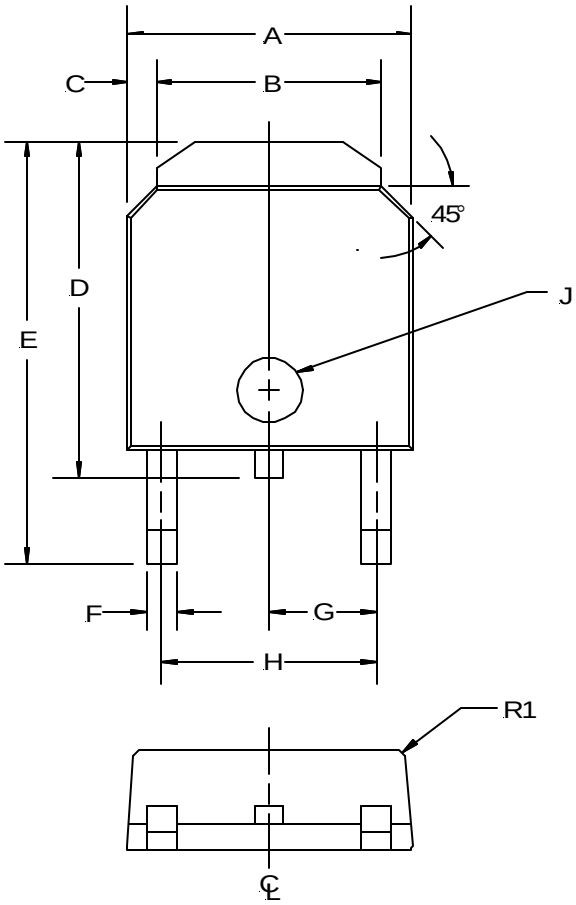
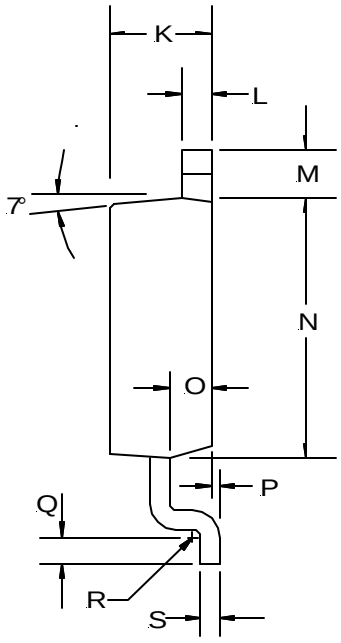
Data and specifications subject to change without notice. 02/01

(D) TO-252 Package
2-Pin





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R	R0.31 TYP	
R1	R0.51 TYP	
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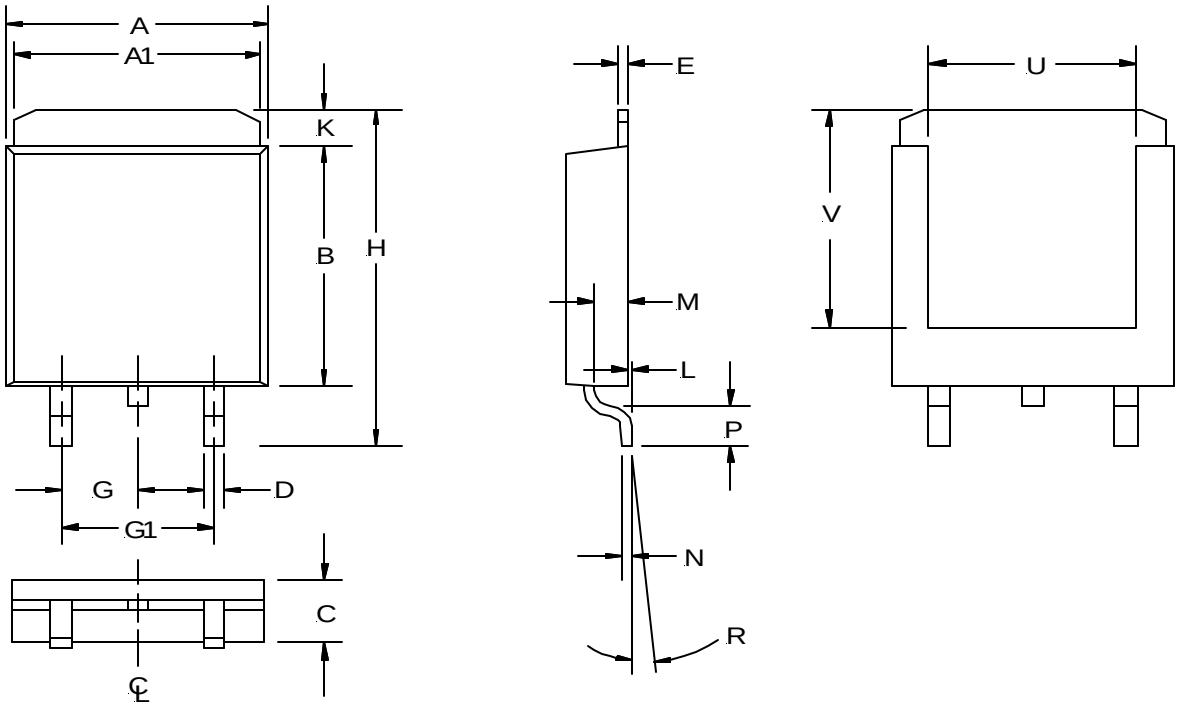
(P) Ultra Thin-Pak™
2-Pin



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R	2°	6°
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V	5.08 NOM	

NOTE: ALL MEASUREMENTS
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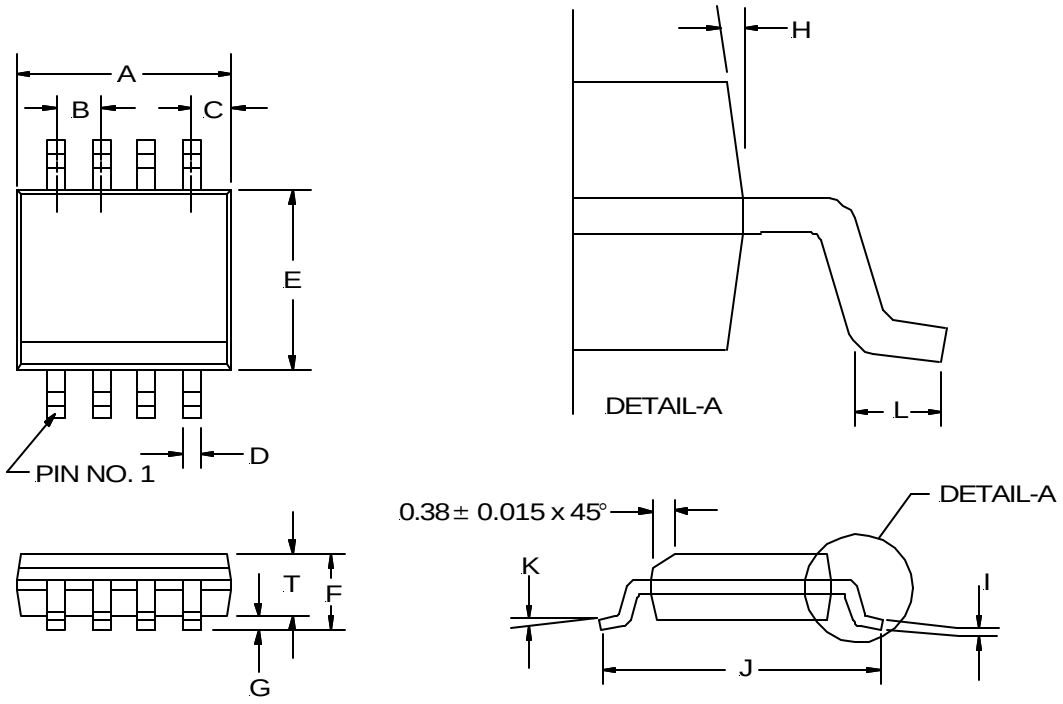
(S) SOIC Package
8-Pin Surface Mount, Narrow Body



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J	5.80	6.20
K	0°	8°
L	0.41	1.27
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NOTE: ALL MEASUREMENTS
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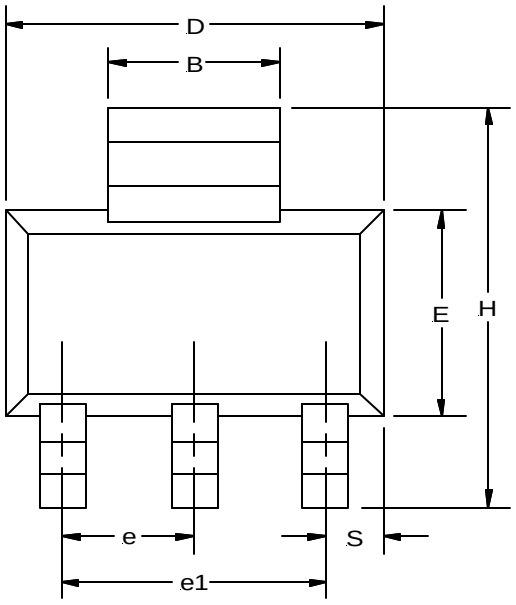
(Y) SOT-223 Package
3-Pin



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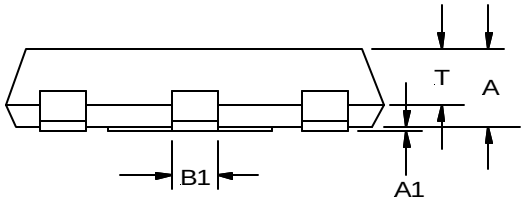

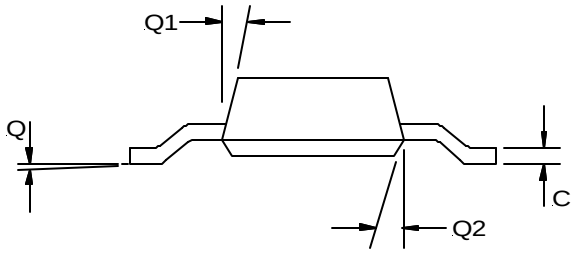

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S	SOIC, Narrow Body	8	95	2500	Fig C
Y	SOT-223	3	80	2500	Fig D

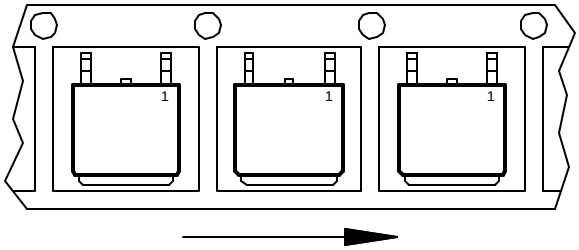

Figure A

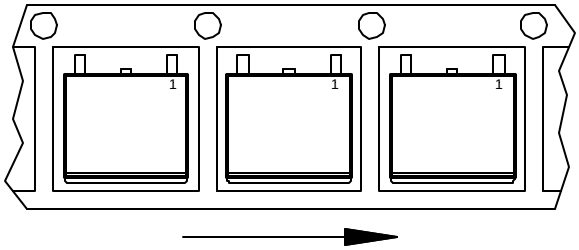

Figure B

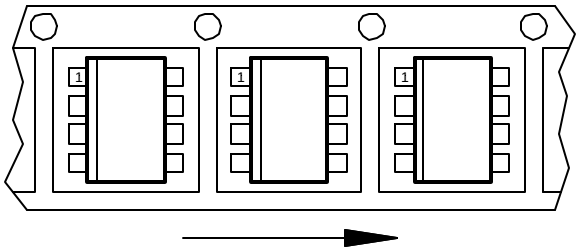

Figure C

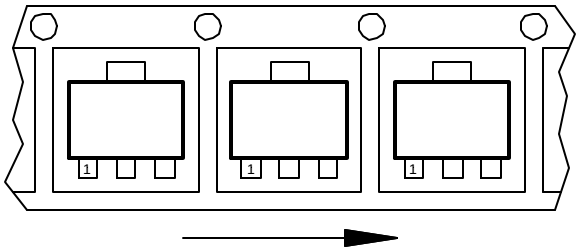

Figure D

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IOR Rectifier

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TAC Fax: (310) 252-7903
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IRU1010-25

1A LOW DROPOUT POSITIVE FIXED 2.5V REGULATOR

FEATURES

- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown
- Available in SOT-223, D-Pak, Ultra Thin-Pak™ and 8-Pin SOIC Surface-Mount Packages

APPLICATIONS

- Low Voltage IC Supply Applications
- PC Clock Supply Voltage

DESCRIPTION

The IRU1010-25 is a low dropout three-terminal fixed output regulator with minimum of 1A output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications as well as generating clock supply for PC applications. The IRU1010-25 is guaranteed to have <1.3V dropout at full load current making it ideal to provide well regulated with 3.8V input supply. The IRU1010-25 is specifically designed to be stable with low cost aluminum capacitors while maintaining stability with low ESR tantalum caps.

TYPICAL APPLICATION

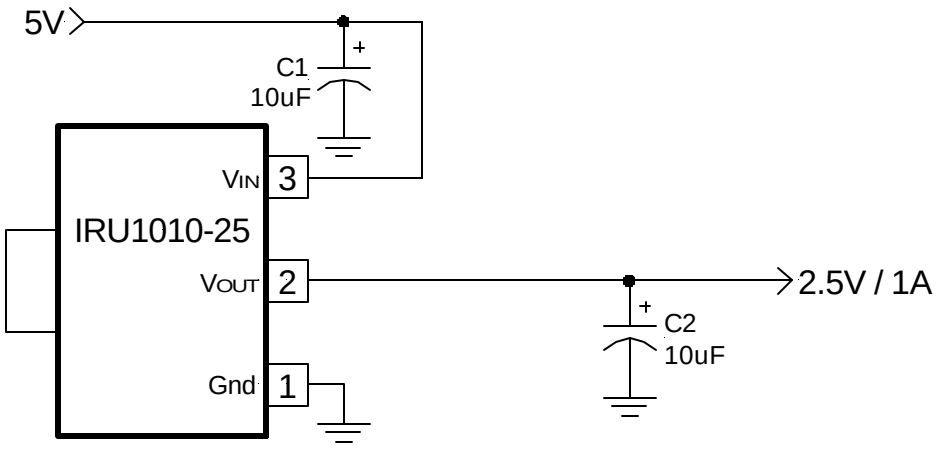


Figure 1 - Typical application of IRU1010-25 in a 5V to 2.5V regulator.

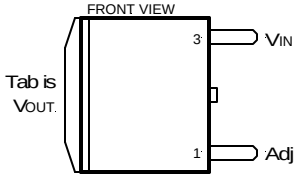
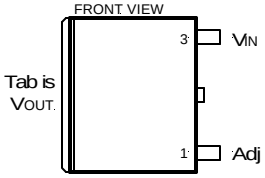
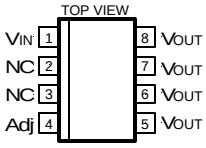
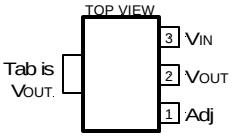
PACKAGE ORDER INFORMATION

T_J (°C)	2-PIN PLASTIC TO-252 (D-Pak)	2-PIN PLASTIC Ultra Thin-Pak™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SOT-223 (Y)
0 To 150	IRU1010-25CD	IRU1010-25CP	IRU1010-25CS	IRU1010-25CY

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)	2-PIN ULTRA THIN-PAK™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SO-223 (Y)
			
θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=55°C/W for 1" Sq pad	θ_{JA}=90°C/W for 0.4" Sq pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, V_{IN}=5V, C_{OUT}=10µF and T_J=0 to 125°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	Vo	Io=10mA, T_J=25°C	2.475	2.500	2.525	V
		Io=10mA	2.450	2.500	2.550	
Line Regulation		Io=10mA, 4.75V<V_{IN}<7V			7	mV
Load Regulation (Note 1)		10mA<Io<1A			17	mV
Dropout Voltage (Note 2)		Io=1A			1.3	V
Current Limit		ΔVo=100mV	1.1			A
Thermal Regulation		30ms Pulse, Io=1A		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum,				
		Io=0.5A	60	70		dB
Temperature Stability		Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%Vo

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Gnd	Ground pin. This pin must be connected to ground plane using a low inductance short connection.
2	V_{OUT}	The output of the regulator. This pin is also connected to the tab of the package. An output capacitor must be connected to this pin to insure stability of the regulator.
3	V_{IN}	Input pin of the regulator.

BLOCK DIAGRAM

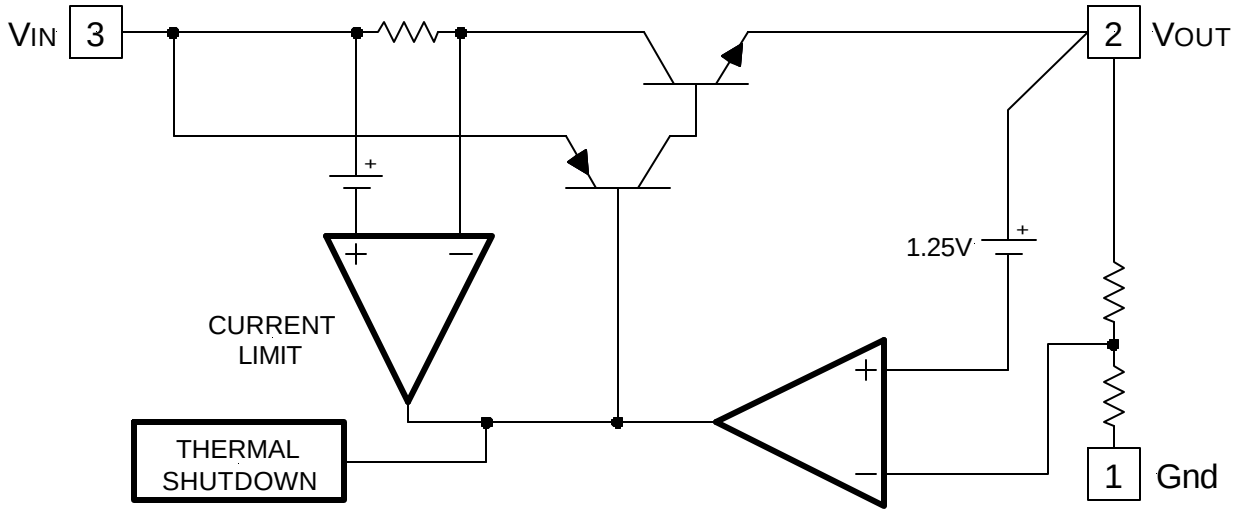


Figure 2 - Simplified block diagram of the IRU1010-25.

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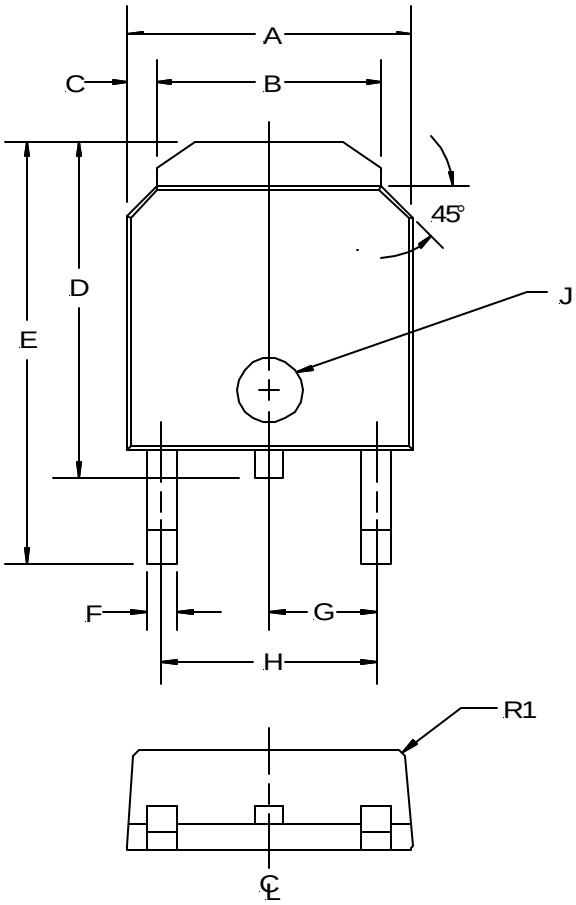
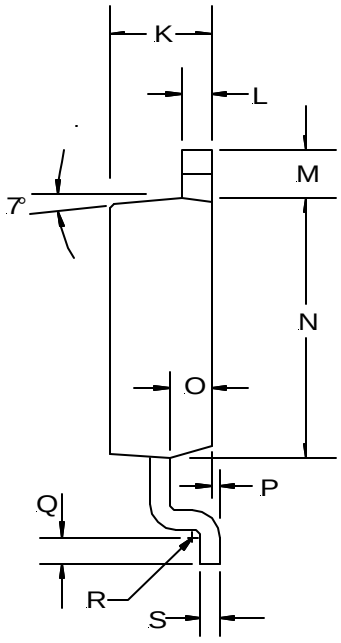
(D) TO-252 Package
2-Pin

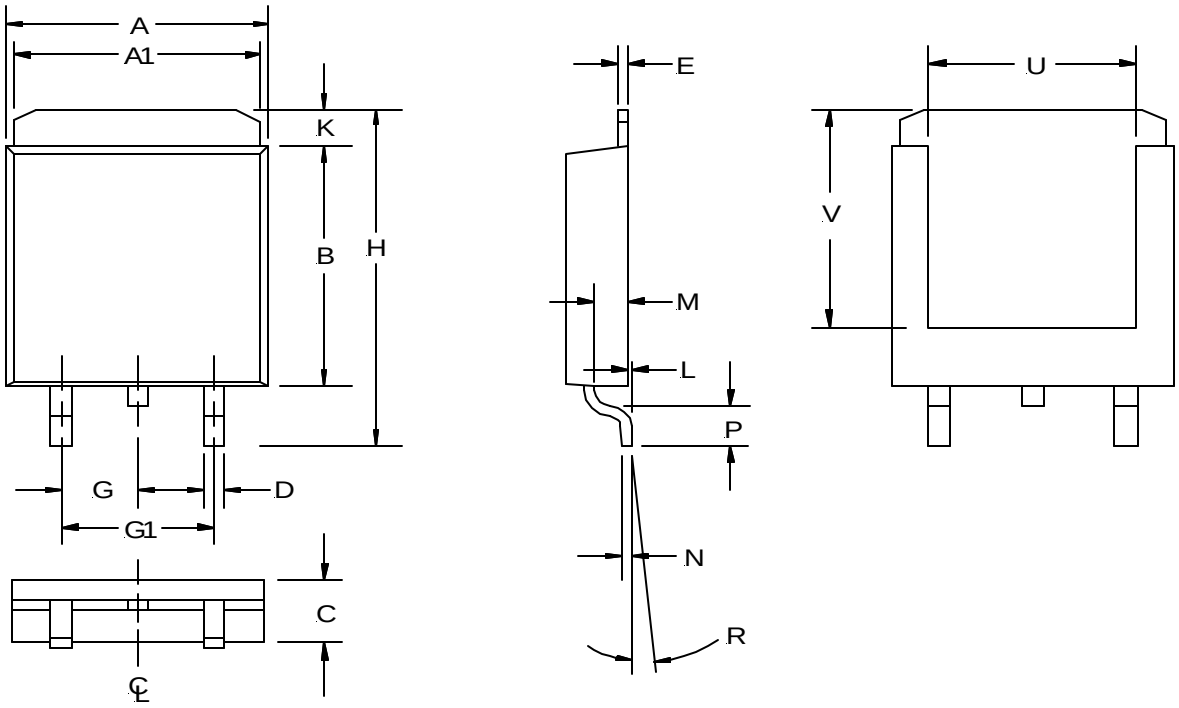




SYMBOL	MIN	MAX
A	6.477	6.731
B	5.004	5.207
C	0.686	0.838
D	7.417	8.179
E	9.703	10.084
F	0.635	0.889
G	2.286 BSC	
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

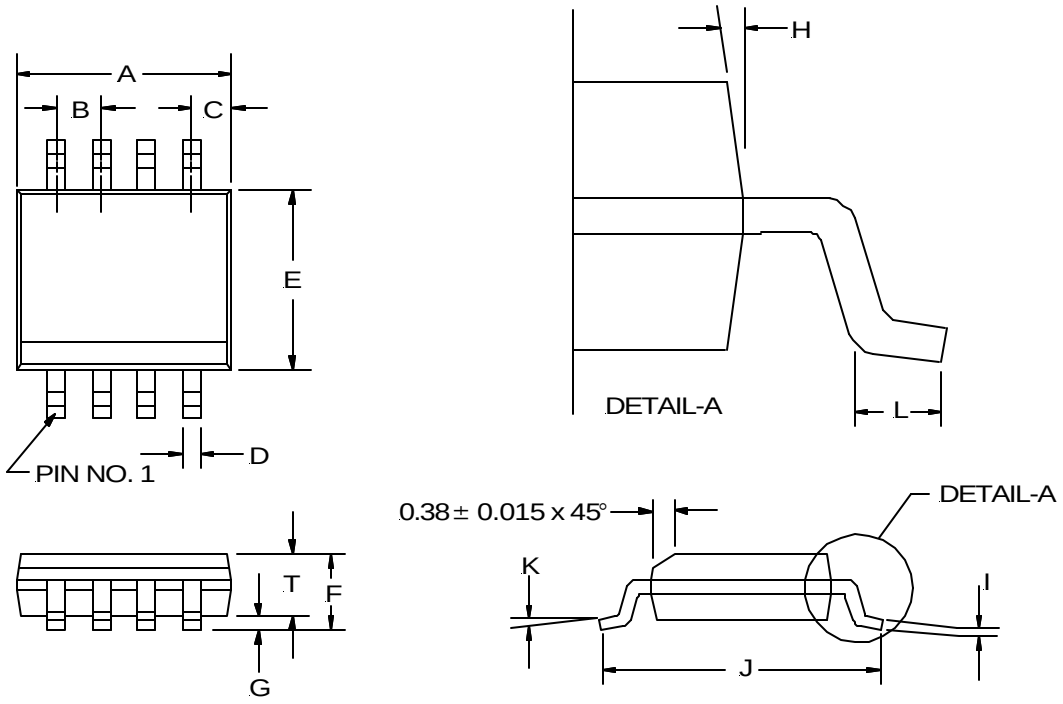
(P) Ultra Thin-Pak™
2-Pin



SYMBOL	MIN	MAX
A	5.91	6.17
A1	5.54	5.79
B	6.02	6.27
C	1.70	2.03
D	0.63	0.79
E	0.17	0.33
G	2.16	2.41
G1	4.45	4.70
H	9.42	9.68
K	0.76	1.27
L	0.02	0.13
M	0.89	1.14
N	0.25	0.25
P	0.94	1.19
R	2°	6°
U	2.92	3.30
V	5.08 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

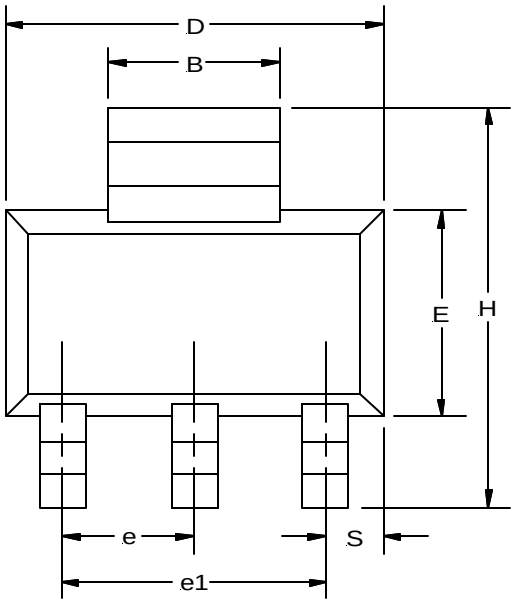
(S) SOIC Package
8-Pin Surface Mount, Narrow Body



8-PIN		
SYMBOL	**MIN**	**MAX**
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

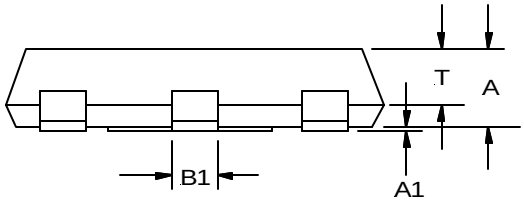
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

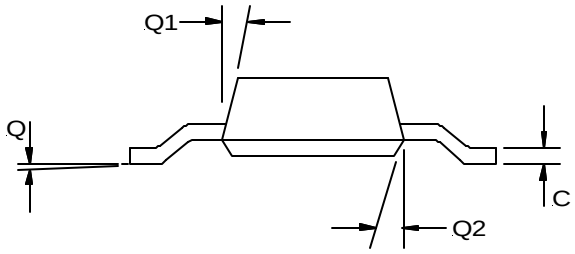
(Y) SOT-223 Package
3-Pin



SYMBOL	MIN	MAX
A	1.498	1.702
A1	0.02	0.11
B	2.895	3.15
B1	0.637	0.85
C	0.239	0.381
D	6.299	6.706
E	3.30	3.708
e	2.209	2.953
e1	4.496	4.699
H	6.70	7.30
Q	0°	10°
Q1	7°	16°
Q2	7°	16°
S	0.838	1.05
T	1.092	1.30

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.





PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
P	Ultra Thin-Pak™	2	75	2500	Fig B
S	SOIC, Narrow Body	8	95	2500	Fig C
Y	SOT-223	3	80	2500	Fig D

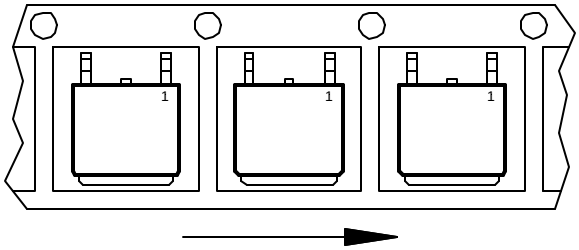


Figure A

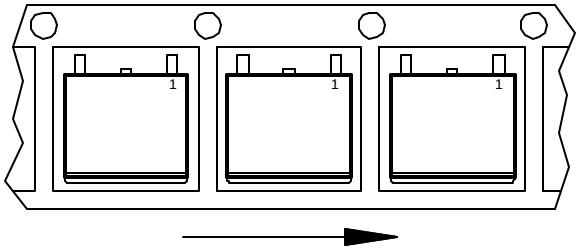


Figure B

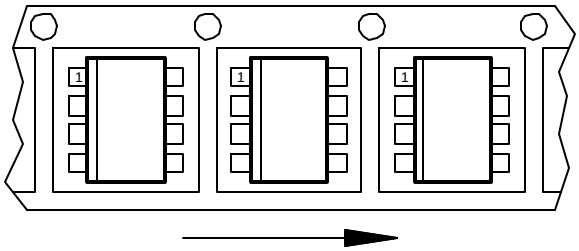


Figure C

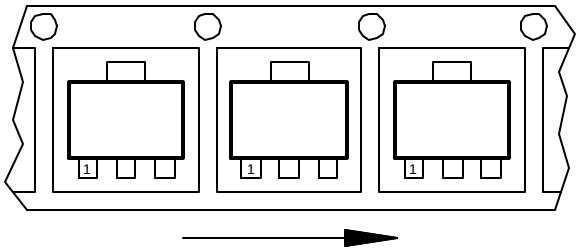


Figure D

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IRU1010-33

1A LOW DROPOUT POSITIVE FIXED 3.3V REGULATOR

FEATURES

- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- 1% Output Voltage Initial Accuracy
- Built-In Thermal Shutdown
- Available in SOT-223, D-Pak, Ultra Thin-Pak™ and 8-Pin SOIC Surface-Mount Packages

APPLICATIONS

- VGA & Sound Card Applications
- Standard 3.3V Chip Set and Logic Applications

DESCRIPTION

The IRU1010-33 is a low dropout three-terminal fixed output regulator with minimum of 1A output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications such as VGA, sound & DVD cards. The IRU1010-33 is guaranteed to have <1.3V dropout at full load current making it ideal to provide well regulated with 4.75V to 7V input supply. The IRU1010-33 is specifically designed to be stable with low cost aluminum capacitors while maintaining stability with low ESR tantalum caps.

TYPICAL APPLICATION

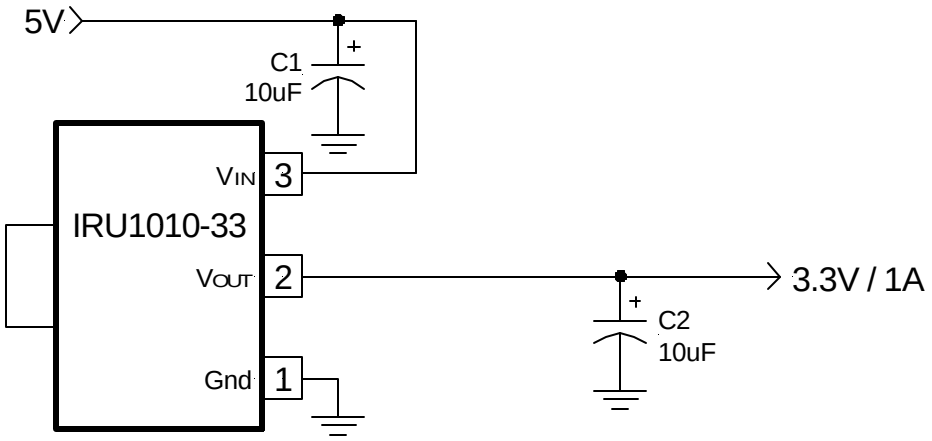


Figure 1 - Typical application of IRU1010-33 in a 5V to 3.3V regulator.

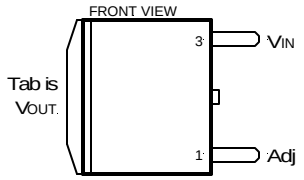
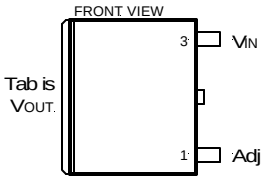
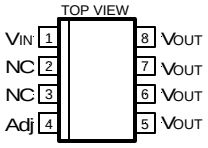
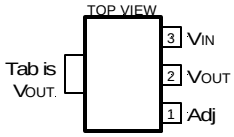
PACKAGE ORDER INFORMATION

T_J (°C)	2-PIN PLASTIC TO-252 (D-Pak)	2-PIN PLASTIC Ultra Thin-Pak™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SOT-223 (Y)
0 To 150	IRU1010-33CD	IRU1010-33CP	IRU1010-33CS	IRU1010-33CY

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)	2-PIN ULTRA THIN-PAK™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SOT-223 (Y)
			
θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=55°C/W for 1" Sq pad	θ_{JA}=90°C/W for 0.4" Sq pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, V_{IN}=5V, C_{OUT}=10µF, and T_J=0 to 125°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	Vo	Io=10mA, T_J=25°C	3.267	3.300	3.333	V
		Io=10mA	3.235	3.300	3.365	
Line Regulation		Io=10mA, 4.75V<V_{IN}<7V			7	mV
Load Regulation (Note 1)		10mA<Io<1A			17	mV
Dropout Voltage (Note 2)		Io=1A			1.3	V
Current Limit		ΔVo=100mV	1.1			A
Thermal Regulation		30ms Pulse, Io=1A		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum,				
		Io=0.5A	60	70		dB
Temperature Stability		Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%Vo

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Gnd	Ground pin. This pin must be connected to ground plane using a low inductance short connection.
2	V_{OUT}	The output of the regulator. This pin is also connected to the tab of the package. An output capacitor must be connected to this pin to insure stability of the regulator.
3	V_{IN}	Input pin of the regulator.

BLOCK DIAGRAM

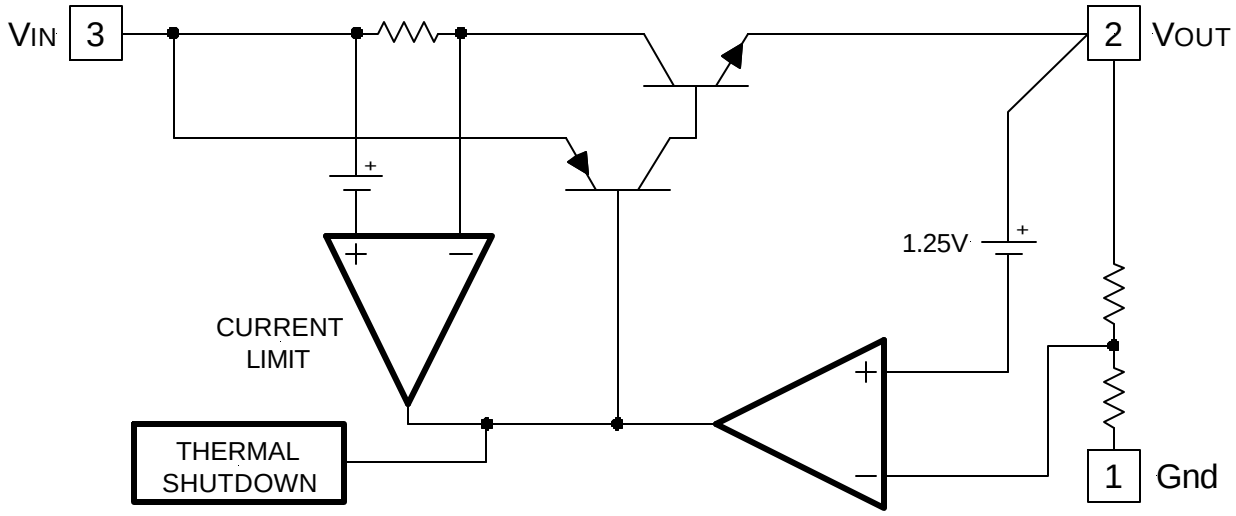


Figure 2 - Simplified block diagram of the IRU1010-33.

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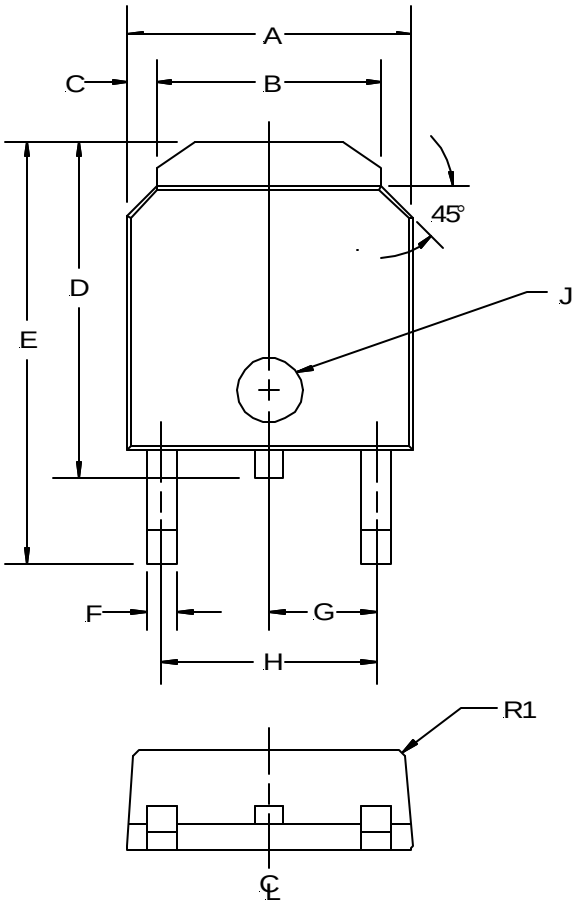
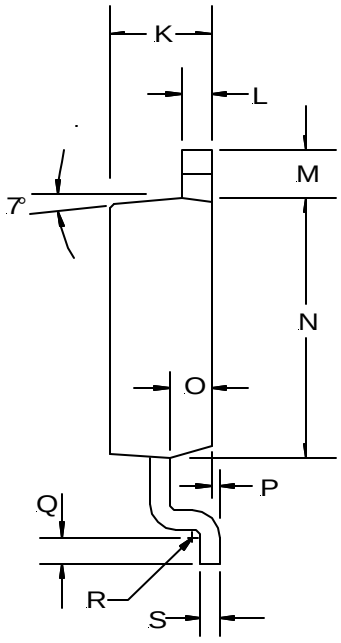
(D) TO-252 Package
2-Pin





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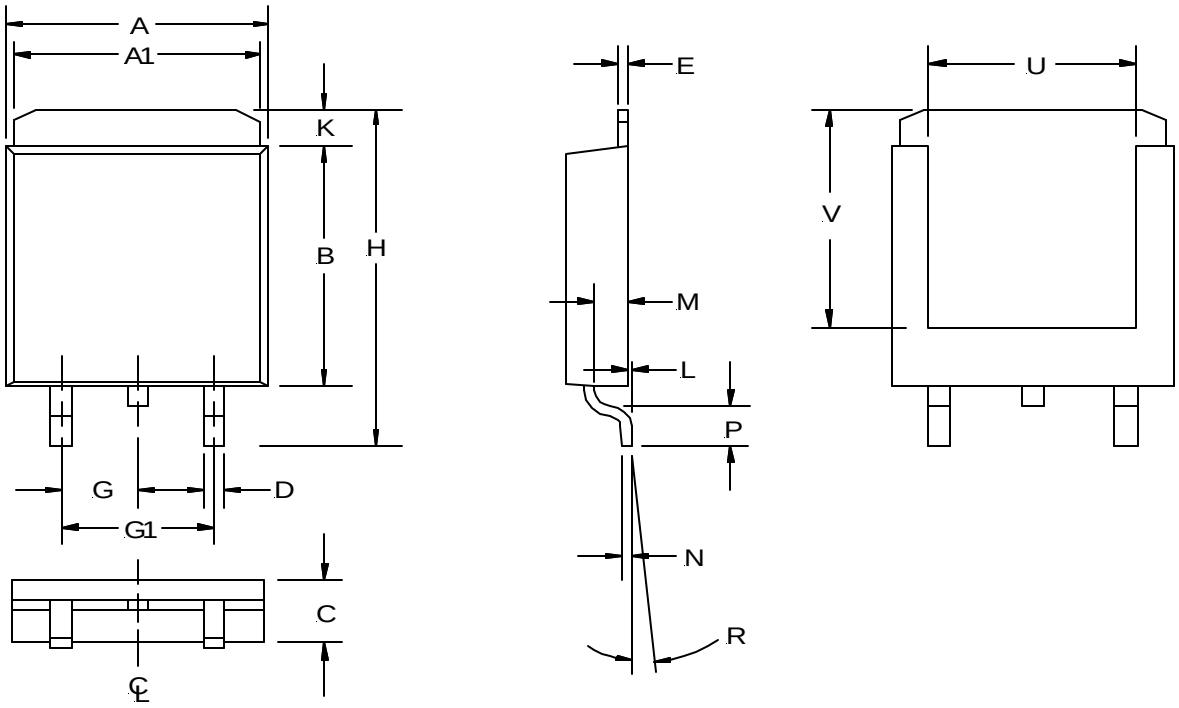
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

(P) Ultra Thin-Pak™
2-Pin



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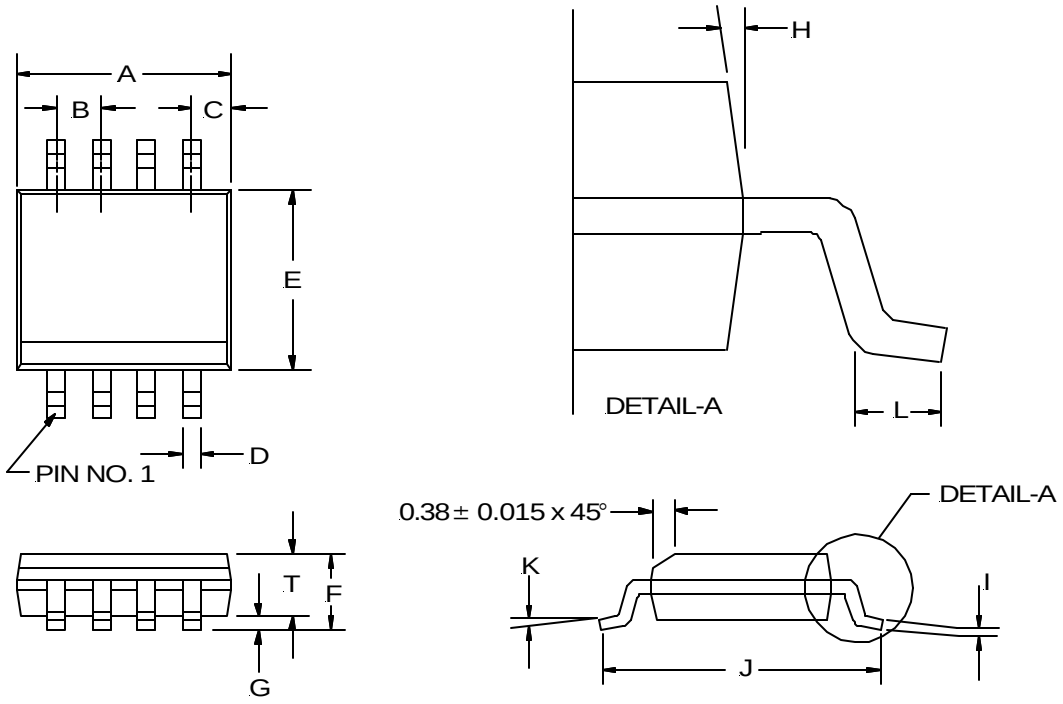
D	0.63	0.79
E	0.17	0.33
G	2.16	2.41
G1	4.45	4.70
H	9.42	9.68
K	0.76	1.27
L	0.02	0.13
M	0.89	1.14
N	0.25	0.25
P	0.94	1.19
R	2°	6°
U	2.92	3.30
V	5.08 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

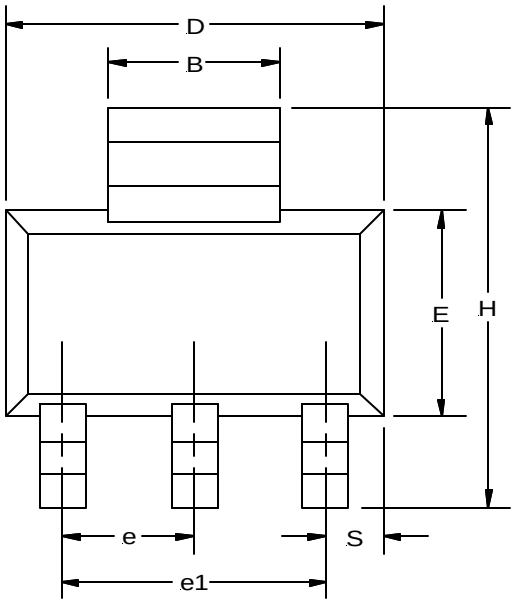
(S) SOIC Package
8-Pin Surface Mount, Narrow Body



8-PIN		
SYMBOL	**MIN**	**MAX**
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

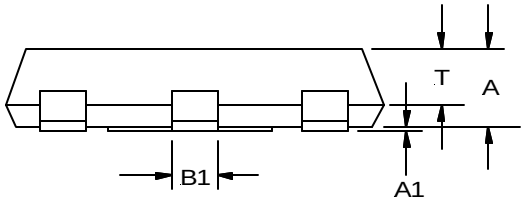
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

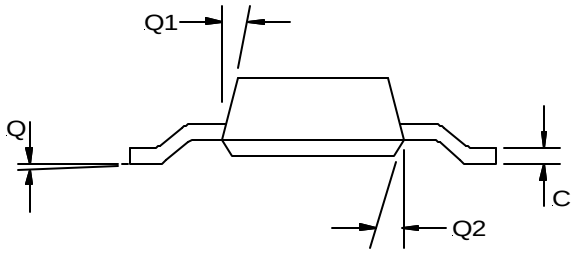
(Y) SOT-223 Package
3-Pin



SYMBOL	MIN	MAX
A	1.498	1.702
A1	0.02	0.11
B	2.895	3.15
B1	0.637	0.85
C	0.239	0.381
D	6.299	6.706
E	3.30	3.708
e	2.209	2.953
e1	4.496	4.699
H	6.70	7.30
Q	0°	10°
Q1	7°	16°
Q2	7°	16°
S	0.838	1.05
T	1.092	1.30

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.





PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
P	Ultra Thin-Pak™	2	75	2500	Fig B
S	SOIC, Narrow Body	8	95	2500	Fig C
Y	SOT-223	3	80	2500	Fig D

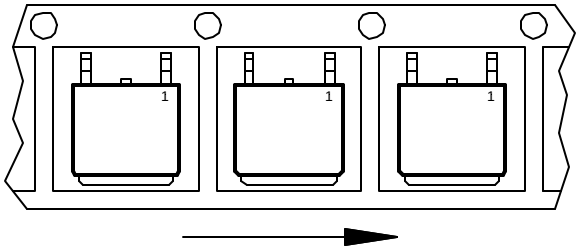


Figure A

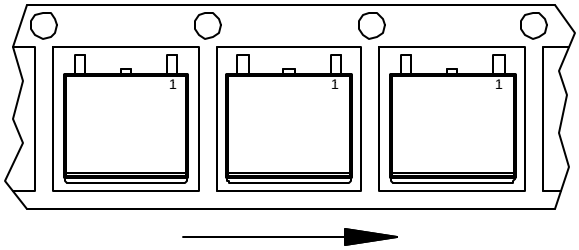


Figure B

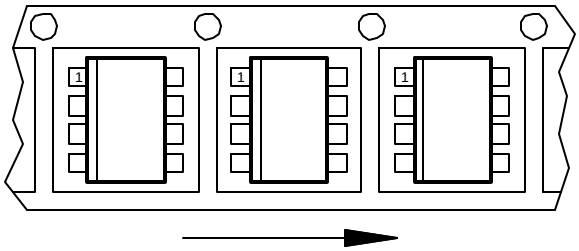


Figure C

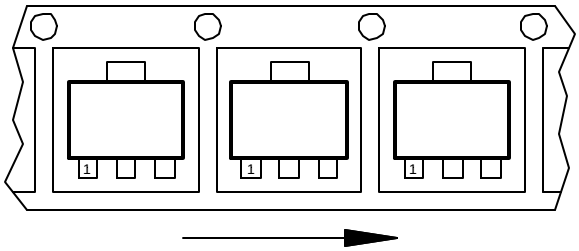


Figure D

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IRU1011-33

1.3A LOW DROPOUT POSITIVE FIXED REGULATOR

PRELIMINARY DATA SHEET

FEATURES

- **Stable with Ceramic Capacitor**
- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- Output Current Limiting
- Built-In Thermal Shutdown

APPLICATIONS

- High Efficiency Linear Regulator
- Hard Disk Drivers, CD-ROMs, DVDs
- ADSL and Cable Modems

DESCRIPTION

The IRU1011-33 is a fixed linear regulator and it is capable of supplying 1.3A of continuous current over line and temperature range. The IRU1011-33 is stable with low value ceramic capacitors, allowing designers flexibility in external component selection. The output is protected by both current limit and thermal shutdown.

TYPICAL APPLICATION

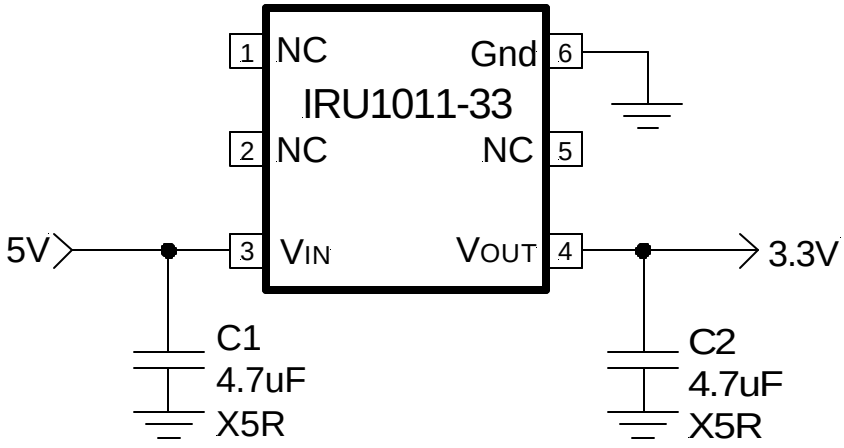


Figure 1 - Typical application of IRU1011-33.

PACKAGE ORDER INFORMATION

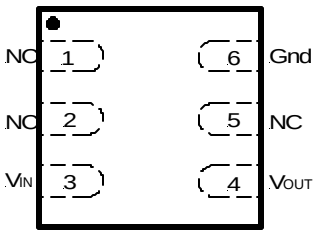
T_A (°C)	6-Pin MLPM 3x3 (H)	MLPM Marking
0 To 150	IRU1011-33CH	CM33

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 10V
Operating Junction Temperature Range ..... 0°C To 150°C
Operating Ambient Temperature Range ..... -40°C To 125°C
Storage Temperature Range ..... -65°C To 150°C

PACKAGE INFORMATION

6-PIN MLPM 3x3 (H)



θ_{JA}=32°C/W
For 1" Square Pad

Exposed Pad on underside is connected to Gnd

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V_{IN}=4.5V to 7V, I_{OUT}=2mA to 1.3A, C_{IN}=C_{OUT}=4.7µF and 0°C<T_J<150°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage 3.3V	$V_{O(3.3)}$	4.75V<V_{IN}<5.25V, 5mA≤I_O≤1.3A: T_J=25°C 0°C≤T_J≤150°C	 3.234 3.2175	 3.3 3.3	 3.366 3.3825	 V
Line Regulation	Reg_{LINE}	4.75V<V_{IN}<5.25V, I_O=10mA		5	15	mV
Load Regulation	Reg_{LOAD}	V_{IN}=4.75V, 10mA≤I_O≤1.3A		8	12	mV
Dropout Voltage ΔV_{OUT}= -1%	V_D	I_O=1.3A		1.1	1.3	V
Current Limit	I_S	V_{IN}=5.5V	1.3	1.9		A
Minimum Output Current	$I_{O(MIN)}$	Note 3, 5		0	2	mA
Temperature Stability	T_S	Note 4, 5		1.5		%
RMS Output Noise	V_N	T_J=25°C, 10Hz<BW<10KHz, Note 5		0.003		%Vo
Ripple Rejection (V_{IN} to Output)	R_A	V_{IN}=5V, Note 5, f=120Hz	60	65		dB
Thermal Shutdown	$T_{J(SD)}$	4.75V<V_{IN}<5.25V, 0mA≤I_O≤1.3A, Note 5	150	155		°C
Quiescent Current	I_{GND}	V_{IN}≤7V, 2mA≤I_O≤1.3A V_{IN}=5V, 0mA≤I_O≤50mA, T_J=25°C		4.3 <4.2	5	mA
Transient Response Change of V_{OUT} with Step Load Change	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	V_{IN}=5V, 10mA<I_O<1.3A, t_r ≥ 1µs V_{IN}=5V, 1.3A to 10mA, t_r ≥ 1µs C_{IN}=C_O=10µF, X7R & Note 5		5 5	±10 ±10	%
Transient Response Change of V_{OUT} with Application of V_{IN}	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	0 to 5V step input, t_r ≥ 1µs, 1mA≤I_O≤1.3A, C_{IN}=C_O=10µF, X7R, Note 5		1	±10	%
Transient Response Short Circuit Removal Response	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$ @I_O=Short	V_{IN}=5V, Short≤I_O≤10mA, C_{IN}=C_O=10µF, X7R, Note 5		1	±20	%

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation.

Note 4: Temperature stability is the change in output from nominal over the operating temperature range.

Note 5: Guaranteed by design, but not tested in production.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1,2,5	NC	No connection.
3	V_{IN}	The power input pin of the regulator. A minimum of input capacitance must be connected from this pin to ground to insure that the input voltage does not sag below the minimum dropout voltage during the load transient response. This pin must always be higher than the V_{OUT} pin by the amount of dropout voltage (see electrical specification) in order for the device to regulate properly.
4	V_{OUT}	The output of the regulator. A minimum of output capacitance must be connected from this pin to ground to insure stability.
6	Gnd	This pin is connected with ground. It is also the tab of the package.

BLOCK DIAGRAM

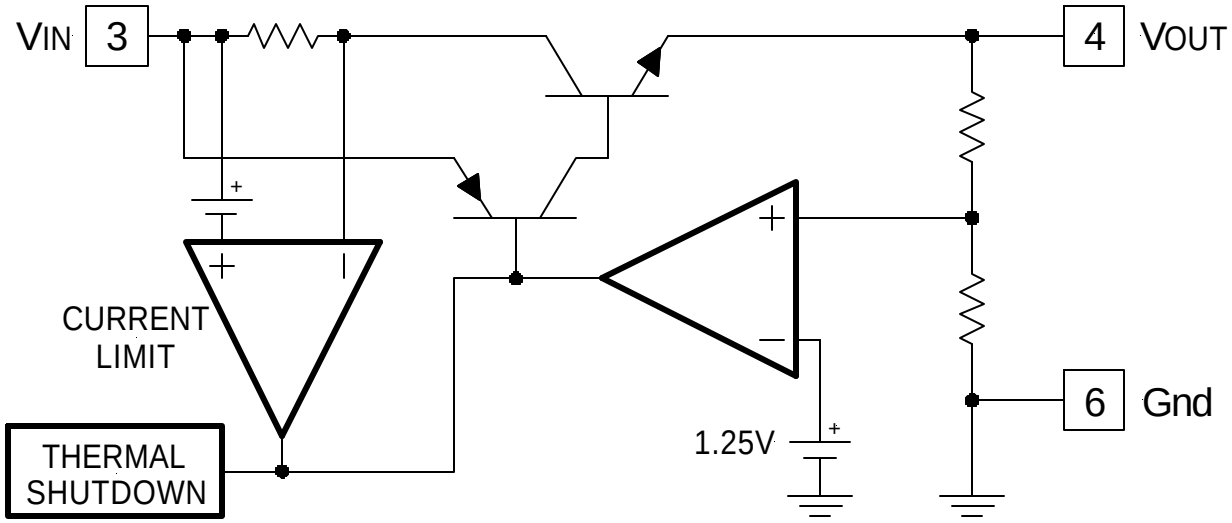


Figure 2 - Simplified block diagram of the IRU1011-33.

APPLICATION INFORMATION

Introduction
The IRU1011-33 regulator is a 3-terminal device offered in a fixed output of 3.3V and it is designed specifically to provide an extremely low dropout voltage.

The IRU1011-33 is designed to meet the fast current transient needs as well as providing an accurate initial voltage, reducing the overall system cost with the need for fewer number of output capacitors.

Thermal Protection
When the junction temperature exceeds 150°C, the internal thermal protection shuts the IRU1011-33 down.

Current Limit Protection
The IRU1011-33 provides Over Current Protection when the output current exceeds typically 2A. The output decreases to limit the power dissipation.

Stability
The IRU1011-33 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. A minimum input capacitance of 4.7μF and a minimum output capacitance 4.7μF Ceramic capacitor is needed for regulator stage as well as the specified minimum loads to guarantee stability.

Transient Response and PSRR
The input and output capacitors are critical in order to ensure good transient response and PSRR. The most important aspects of this are capacitor selection, placement and trace routing. Place each capacitor as close as physically possible to its corresponding regulator pin. Use wide traces for a low inductance path. Couple directly to the ground and power planes as possible. The use of low ESR capacitors is crucial to achieving good results. Larger capacitance and lower ESR will improve both PSRR and transient response.

Thermal Design
The IRU1011-33 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the allowable maximum junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. The example below shows the steps in selecting the proper surface mount package.

Assuming, the following conditions:

V_{OUT} = 3.3V
V_{IN} = 5V
I_{OUT} = 1A (DC Avg)

Calculate the maximum power dissipation using the following equation:

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT})$$

$$P_D = 1 \times (5 - 3.3) = 1.7W$$

For MLPM package, we have:

R_{THJA} = 32°C/W
T_A = 45°C
$\Delta T = P_D \times R_{THJA} = 1.7 \times 32 = 54.4$
$TJ = T_A + \Delta T = 99.4°C$

Layout Consideration
The IRU1011-33, like many other high-speed regulators, requires that the output capacitors be close to the device for stability. For power consideration, a ground plane pad of approximately one-inch square on the component side must be dedicated to the device where all Gnd pins are connected to dissipate the power. If a multilayer board is used, it is recommended that the inner layers of the board are also dedicated to the size of the pad for better thermal characteristics.

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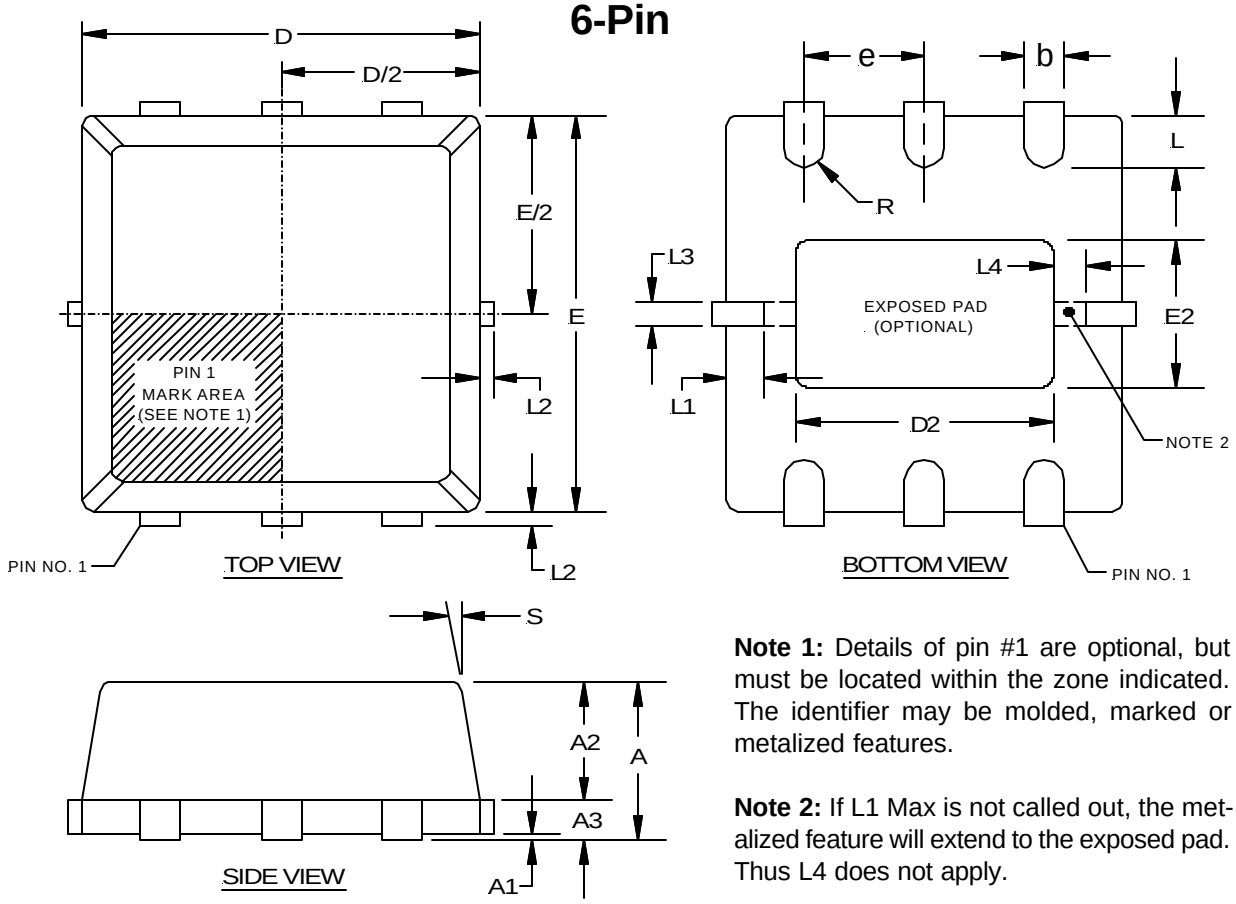
(H) MLPM Package
6-Pin



Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, marked or metalized features.

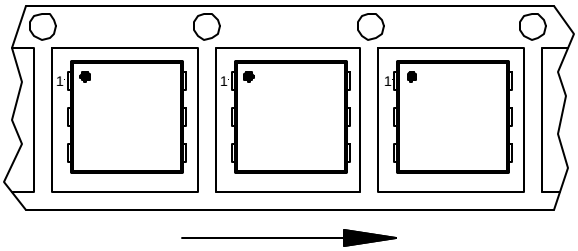
Note 2: If L1 Max is not called out, the metalized feature will extend to the exposed pad. Thus L4 does not apply.

SYMBOL DESIG	6-PIN 3x3		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.025	0.05
A2	0.65	0.70	0.75
A3	0.15	0.20	0.25
b	0.33	0.35	0.43
D	3.00 BSC		
D2	1.92	2.02	2.12
E	3.00 BSC		
E2	1.11	1.21	1.31
e	0.95		
L	0.20	0.29	0.45
L1	0.16	0.24	0.40
L2	---	---	0.125
L3	0.17	---	0.30
L4	0.17	---	---
R	0.127 REF		
S	0°	10°	12°

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
H	MLPM 3x3	6	---	3000	Fig A



Feed Direction
Figure A - Live Bug

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IRU1015

1.5A LOW DROPOUT POSITIVE ADJUSTABLE REGULATOR

FEATURES

- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Output Current Limiting
- Built-In Thermal Shutdown

APPLICATIONS

- 486DX4 Supply Voltage
- P55 I/O Supply Voltage
- VGA & Sound Card Applications
- Low Voltage High Speed Termination Applications
- Standard 3.3V Chip Set and Logic Applications

DESCRIPTION

The IRU1015 is a low dropout three-terminal adjustable regulator with minimum of 1.5A output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications such as 486DX4 processor, P55C™ I/O supply as well as high speed bus termination and low current 3.3V logic supply. The IRU1015 is also well suited for other applications such as VGA and sound card. The IRU1015 is guaranteed to have <1.3V dropout at full load current making it ideal to provide well regulated outputs of 2.5V to 3.3V with 4.75V to 7V input supply.

TYPICAL APPLICATION

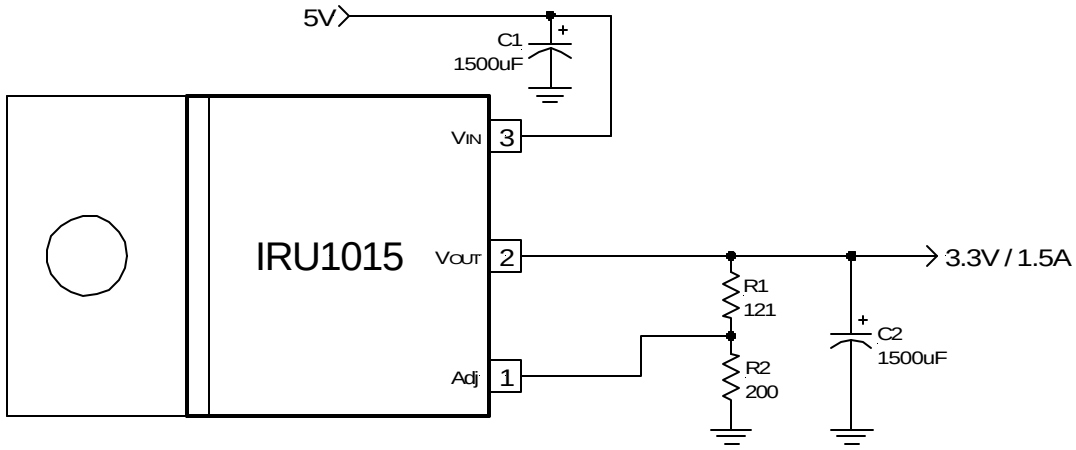


Figure 1 - Typical application of IRU1015 in a 5V to 3.3V regulator.

Note: P55C is trademark of Intel Corp.

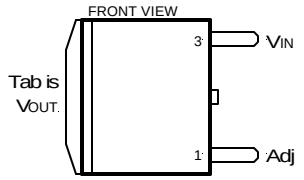
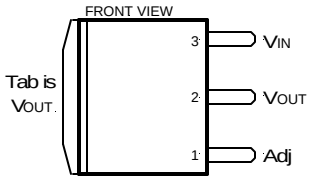
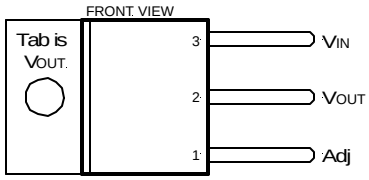
PACKAGE ORDER INFORMATION

T_J (°C)	2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC TO-263 (M)	3-PIN PLASTIC TO-220 (T)
0 To 150	IRU1015CD	IRU1015CM	IRU1015CT

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC TO-263 (M)	3-PIN PLASTIC TO-220 (T)
		
θ_{JA}=70°C/W for 0.5" Square pad	θ_{JA}=35°C/W for 1" Square pad	θ_{JT}=2.7°C/W θ_{JA}=60°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=10µF, and T_J=0 to 150°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	Io=10mA, T_J=25°C, (V_{IN}-Vo)=1.5V	1.238	1.250	1.262	V
		Io=10mA, (V_{IN}-Vo)=1.5V	1.225	1.250	1.275	
Line Regulation		Io=10mA, 1.3V<(V_{IN}-Vo)<7V			0.2	%
Load Regulation (Note 1)		V_{IN}=3.3V, V_{ADJ}=0, 10mA<Io<1.5A			0.4	%
Dropout Voltage (Note 2)	ΔV_O	Note 2, Io=1.5A		1.1	1.3	V
Current Limit		V_{IN}=3.3V, ΔVo=100mV	1.6			A
Minimum Load Current (Note 3)		V_{IN}=3.3V, V_{ADJ}=0V		5	10	mA
Thermal Regulation		30ms Pulse, V_{IN}-Vo=3V, Io=1.5A		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum,				
		Io=0.75A, V_{IN}-Vo=3V	60	70		dB
Adjust Pin Current	I_{ADJ}	Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C,				
		Io=10mA, V_{IN}-Vo=1.5V		55	120	µA
Adjust Pin Current Change		Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C		0.2	5	µA
Temperature Stability		V_{IN}=3.3V, V_{ADJ}=0V, Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%V_O

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor dividers are selected such that it automatically maintains this current.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	Adj	A resistor divider from this pin to the V_{OUT} pin and ground sets the output voltage.
2	V_{OUT}	The output of the regulator. A minimum of 10µF capacitor must be connected from this pin to ground to insure stability.
3	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be 1.3V higher than V_{OUT} in order for the device to regulate properly.

BLOCK DIAGRAM

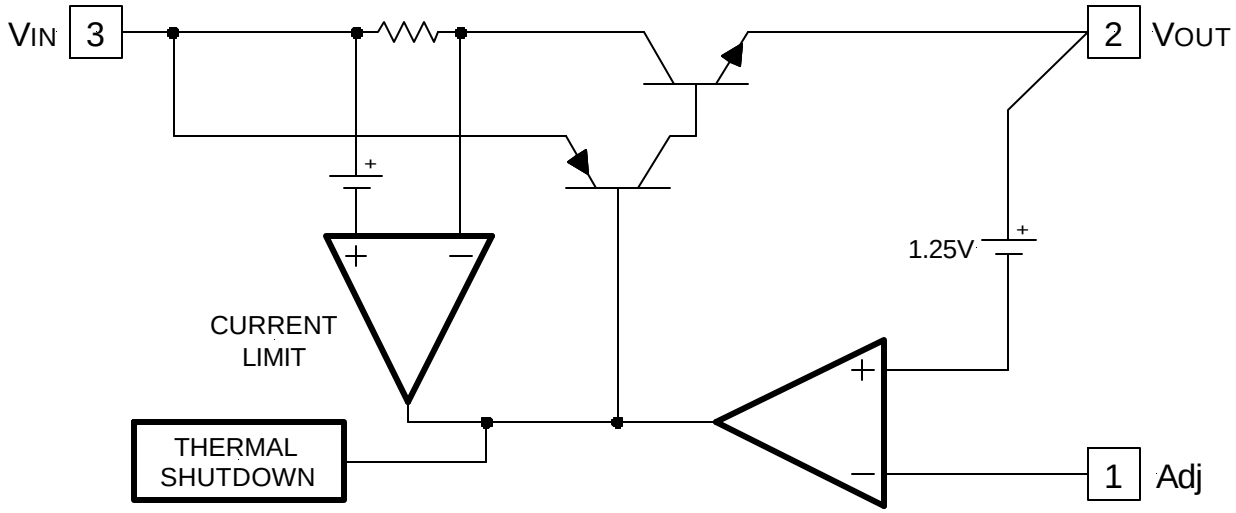


Figure 2 - Simplified block diagram of the IRU1015.

APPLICATION INFORMATION

Introduction

The IRU1015 adjustable Low Dropout (LDO) regulator is a three-terminal device which can easily be programmed with the addition of two external resistors to any voltages within the range of 1.25 to 5.5 V.This regulator unlike the first generation of the three-terminal regulators such as LM117 that required 3V differential between the input and the regulated output, only needs 1.3V differential to maintain output regulation. This is a key requirement for today's microprocessors that need typically 3.3V supply and are often generated from the 5V supply. Another major requirement of these microprocessors is the need to switch the load current from zero to full load in tens of nanoseconds at their pins, which translates to an approximately 300 to 500ns current step at the regulator. In addition, the output voltage tolerances are sometimes tight and they include the transient response as part of the specification.

The IRU1015 is specifically designed to meet the fast current transient needs as well as provide an accurate initial voltage, reducing the overall system cost with the need for fewer output capacitors.

Output Voltage Setting

The IRU1015 can be programmed to any voltages in the range of 1.25V to 5.5V with the addition of R1 and R2 external resistors according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) + I_{ADJ} \times R2$$

Where:

V_{REF} = 1.25V Typically

I_{ADJ} = 50μA Typically

R1 and R2 as shown in Figure 3:

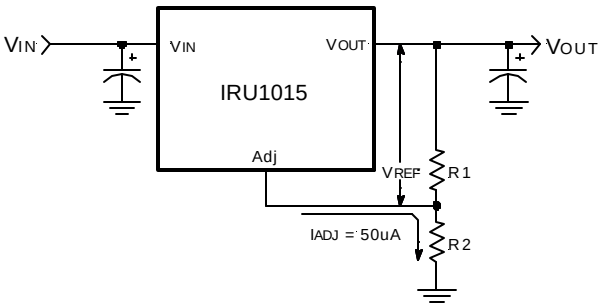


Figure 3 - Typical application of the IRU1015 for programming the output voltage.

The IRU1015 keeps a constant 1.25V between the output pin and the adjust pin. By placing a resistor R1 across these two pins a constant current flows through R1, adding to the I_{ADJ} current and into the R2 resistor producing a voltage equal to the $(1.25/R1) \times R2 + I_{ADJ} \times R2$ which will be added to the 1.25V to set the output voltage. This is summarized in the above equation. Since the minimum load current requirement of the IRU1015 is 10mA, R1 is typically selected to be 121Ω resistor so that it automatically satisfies the minimum current requirement. Notice that since I_{ADJ} is typically in the range of 50μA it only adds a small error to the output voltage and should only be considered when a very precise output voltage setting is required. For example, in a typical 3.3V application where R1=121Ω and R2=200Ω the error due to I_{ADJ} is only 0.3% of the nominal set point.

Load Regulation

Since the IRU1015 is only a three-terminal device, it is not possible to provide true remote sensing of the output voltage at the load. Figure 4 shows that the best load regulation is achieved when the bottom side of R2 is connected to the load and the top side of R1 resistor is connected directly to the case or the V_{OUT} pin of the regulator and not to the load. In fact, if R1 is connected to the load side, the effective resistance between the regulator and the load is gained up by the factor of (1+ R2/R1),or the effective resistance will be $R_{P(eff)} = R_P \times (1+ R2/R1)$. It is important to note that for high current applications, this can represent a significant percentage of the overall load regulation and one must keep the path from the regulator to the load as short as possible to minimize this effect.

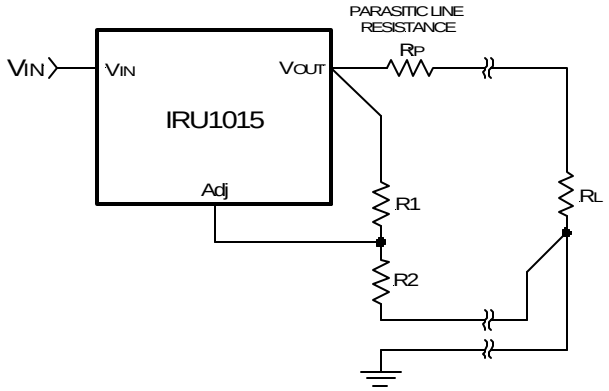


Figure 4 - Schematic showing connection for best load regulation.

Stability

The IRU1015 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for microprocessor applications use standard electrolytic capacitors with a typical ESR in the range of 50 to 100mΩ and an output capacitance of 500 to 1000μF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1015 takes advantage of this phenomena in making the overall regulator loop stable. For most applications a minimum of 100μF aluminum electrolytic capacitor such as Sanyo MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response.

Thermal Design

The IRU1015 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the maximum allowable junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. The example below shows the steps in selecting the proper regulator heat sink for an AMD 486DX4-120 MHz processor.

Assuming the following specifications:

V_{IN} = 5V
V_{OUT} = 3.45V
$I_{OUT(MAX)}$ = 1.2A
T_A = 35°C

The steps for selecting a proper heat sink to keep the junction temperature below 135°C is given as:

1) Calculate the maximum power dissipation using:

$P_D = I_{OUT} \times (V_{IN} - V_{OUT})$

$P_D = 1.2 \times (5 - 3.45) = 1.86W$

2) Select a package from the regulator data sheet and record its junction to case (or Tab) thermal resistance.

Selecting TO-220 package gives us:

θ_{JC} = 2.7°C/W

3) Assuming that the heat sink is black anodized, calculate the maximum Heat sink temperature allowed:

Assume, θcs=0.05°C/W (heat-sink-to-case thermal resistance for black anodized)

$T_S = T_J - P_D \times (\theta_{JC} + \theta_{CS})$

$T_S = 135 - 1.86 \times (2.7 + 0.05) = 129°C$

4) With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance (θ_{SA}) is calculated by first calculating the temperature rise above the ambient as follows:

$\Delta T = T_S - T_A = 129 - 35 = 94°C$

ΔT = Temperature Rise Above Ambient

$$\theta_{SA} = \frac{\Delta T}{P_D} = \frac{94}{1.86} = 50°C/W$$

5) Next, a heat sink with lower θ_{SA} than the one calculated in step 4 must be selected. One way to do this is to simply look at the graphs of the "Heat Sink Temp Rise Above the Ambient" vs. the "Power Dissipation" and select a heat sink that results in lower temperature rise than the one calculated in the previous step. The following heat sinks from AAVID and Thermalloy meet this criteria.

	Air Flow (LFM)	
	0	100
Thermalloy	6041PB	No HS Required
AAVID	574602	No HS Required

Note: For further information regarding the above companies and their latest product offerings and application support contact your local representative or the numbers listed below:

AAVID Thermalloy.....PH# (603) 528-3400

Designing for Microprocessor Applications

As it was mentioned before the IRU1015 is designed specifically to provide power for the new generation of the low voltage processors requiring voltages in the range of 2.5V to 3.6V generated by stepping down the 5V supply. These processors demand a fast regulator that supports their large load current changes. The worst case current step seen by the regulator is anywhere in the range of 1 to 7A with the slew rate of 300 to 500ns which could happen when the processor transitions from “Stop Clock” mode to the “Full Active” mode. The load current step at the processor is actually much faster, in the order of 15 to 20ns, however, the de-coupling capacitors placed in the cavity of the processor socket handle this transition until the regulator responds to the load current levels. Because of this requirement, the selection of high frequency low ESR and low ESL output capacitor is imperative in the design of these regulator circuits.

Figure 5 shows the effects of a fast transient on the output voltage of the regulator. As shown in this figure, the ESR of the output capacitor produces an instantaneous drop equal to the ($\Delta V_{ESR} = ESR \times \Delta I$) and the ESL effect will be equal to the rate of change of the output current times the inductance of the capacitor ($\Delta V_{ESL} = L \times \Delta I/\Delta t$). The output capacitance effect is a droop in the output voltage proportional to the time it takes for the regulator to respond to the change in the current ($\Delta V_C = \Delta t \times \Delta I/C$) where Δt is the response time of the regulator.

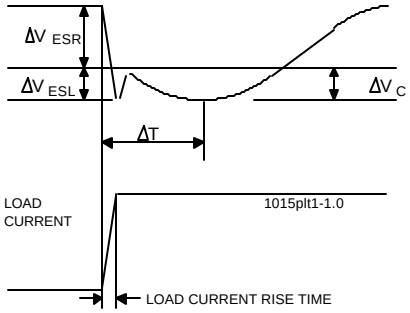


Figure 5 - Typical regulator response to the fast load current step.

An example of a regulator design to meet the AMD specification for 486DX4-120MHz is given below.

Assume the specification for the processor as shown in Table 1:

Type of Processor	V_{OUT} Nominal	I_{MAX}	Max Allowed Output Tolerance
AMD 486DX4	3.45 V	1.2 A	±150 mV

Table 1 - GTL+ specification for Pentium Pro

The first step is to select the voltage step allowed in the output due to the output capacitor's ESR:

1) Assuming the regulator's initial accuracy plus the resistor divider tolerance is ≈ ±86mV (±2.5% of 3.45V nominal), then the total step allowed for the ESR and the ESL, is -64mV.

   Assuming that the ESL drop is -10mV, the remaining ESR step will be -54mV. Therefore the output capacitor ESR must be:

$$ESR \le \frac{54}{1.2} = 45m\Omega$$

   The Sanyo MVGX series is a good choice to achieve both price and performance goals. The 6MV1500GX, 1500μF, 6.3V has an ESR of less than 36mΩ typical. Selecting a single capacitor achieves our design goal.

   The next step is to calculate the drop due to the capacitance discharge and make sure that this drop in voltage is less than the selected ESL drop in the previous step.

2) With the output capacitance being 1500μF:

$$\Delta Vc = \frac{\Delta t \times \Delta I}{C} = \frac{2 \times 1.2}{1500} = 1.6mV$$

   Where:
   $\Delta t = 2\mu s$ is the regulator response time

To set the output voltage, we need to select R1 and R2:

3) Assuming R1=121Ω, 1%

$$R2 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R1 = \left(\frac{3.45}{1.25} - 1\right) \times 121 = 213\Omega$$

   Select R2 = 215Ω, 1%

   Selecting both R1 and R2 resistors to be 1% tolerance results in the least amount of error introduced by the resistor dividers leaving a ≈ ±2.5% error budget for the IRU1015 reference which is well within the initial accuracy of the device.

Finally, the input capacitor is selected as follows:

4) Assuming that the input voltage can drop 150mV before the main power supply responds, and that the main power supply response time is ≈ 50ms, then the minimum input capacitance for a 1.2A load step is given by:

$$C_{IN} = \frac{1.2 \times 50}{0.15} = 400\mu F$$

   The ESR should be less than:

$$ESR = \frac{(V_{IN} - V_{OUT} - \Delta V - V_{DROP})}{\Delta I}$$

   Where:
   V_{DROP} **L** Input voltage drop allowed in step 4
   ΔV **L** Maximum regulator dropout voltage
   ΔI **L** Load current step

$$ESR = \frac{(5 - 3.45 - 1.2 - 0.15)}{1.2} = 0.167\Omega$$

   Select a single 1500μF the same type as the output capacitors exceeds our requirements. Figure 6 shows the completed schematic for our example.

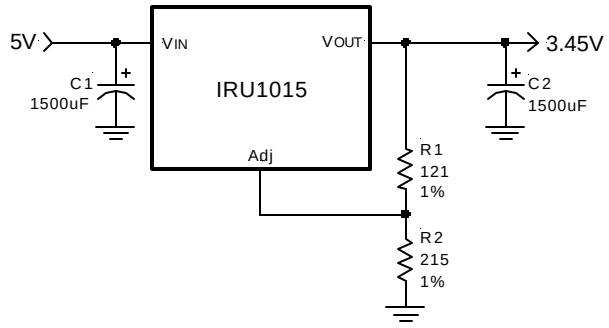


Figure 6 - Final schematic for the regulator design.

Layout Consideration

The output capacitors must be located as close to the V_{OUT} terminal of the device as possible. It is recommended to use a section of a layer of the PC board as a plane to connect the V_{OUT} pin to the output capacitors to prevent any high frequency oscillation that may result from excessive trace inductance.

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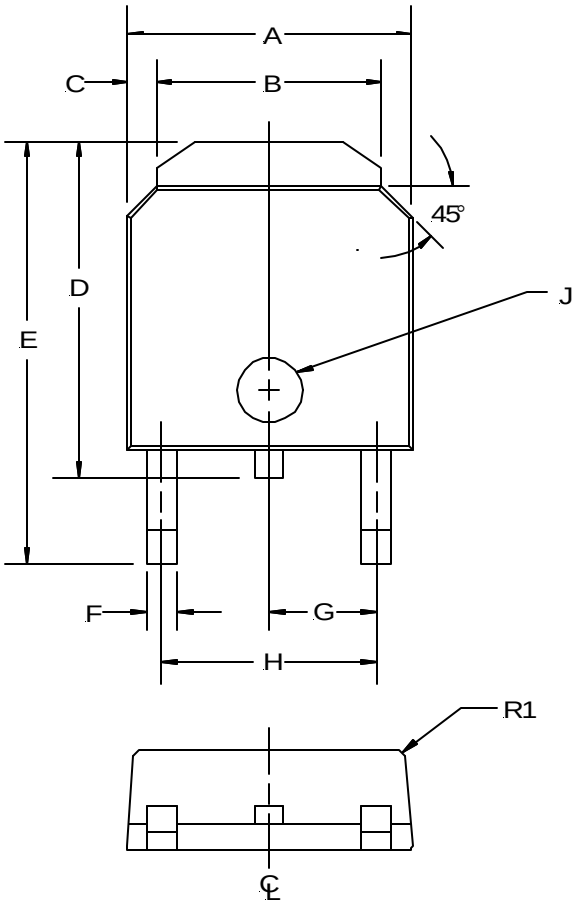
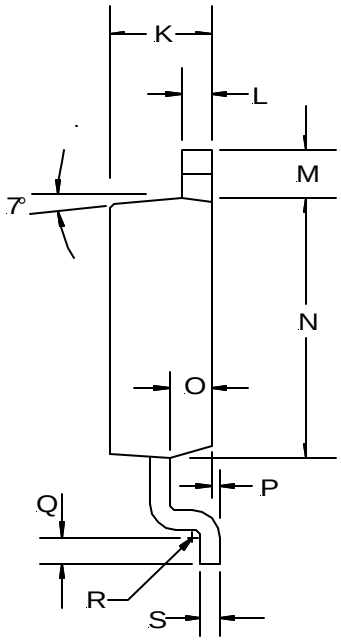
(D) TO-252 Package
2-Pin

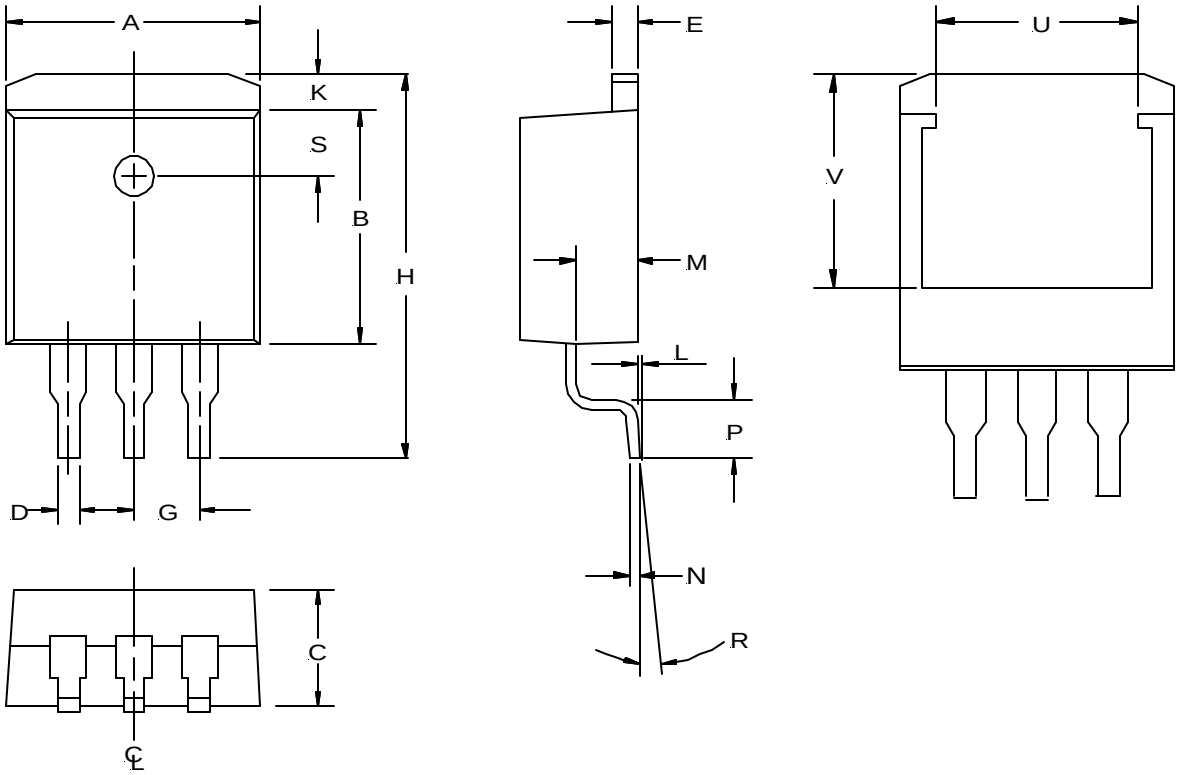




SYMBOL	MIN	MAX
A	6.477	6.731
B	5.004	5.207
C	0.686	0.838
D	7.417	8.179
E	9.703	10.084
F	0.635	0.889
G	2.286 BSC	
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

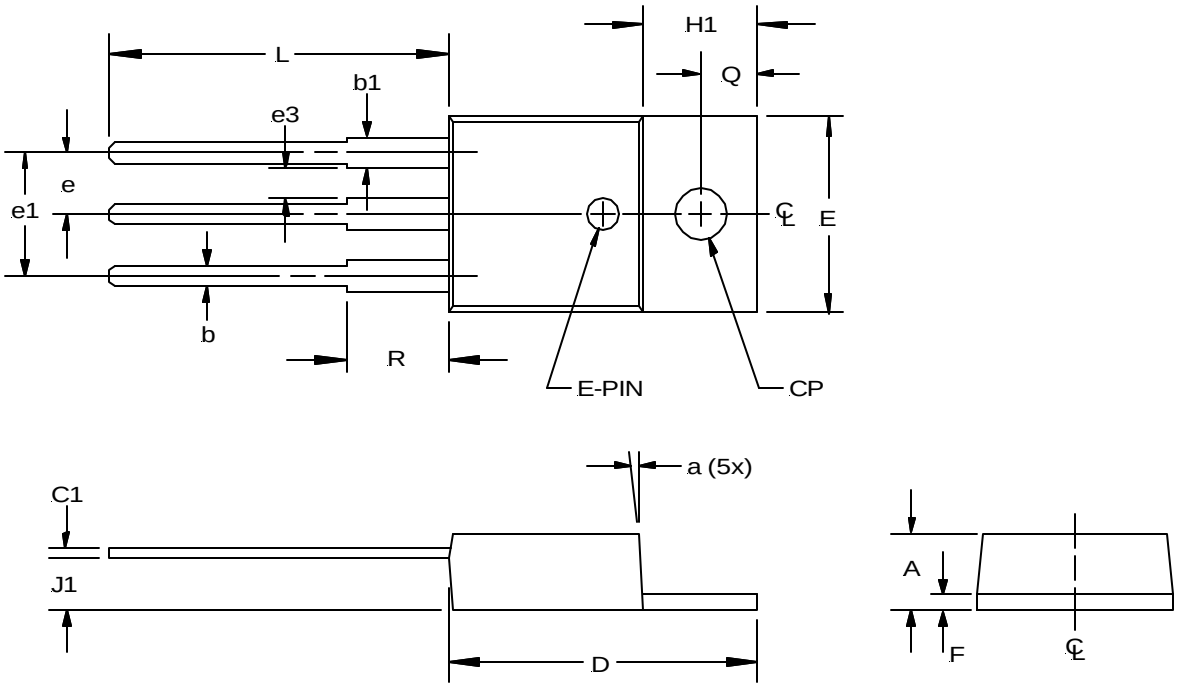
(M) TO-263 Package
3-Pin



SYMBOL	MIN	MAX
A	10.05	10.312
B	8.28	8.763
C	4.31	4.572
D	0.66	0.91
E	1.14	1.40
G	2.54 REF	
H	14.73	15.75
K	1.40	1.68
L	0.00	0.254
M	2.49	2.74
N	0.33	0.58
P	2.286	2.794
R	0°	8°
S	2.41	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(T) TO-220 Package
3-Pin

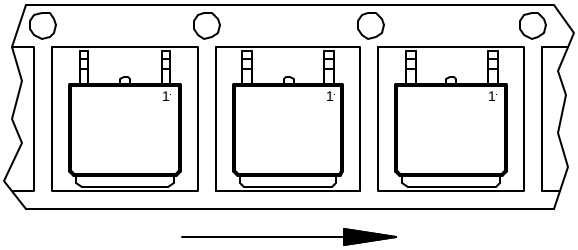


SYMBOL	MIN	MAX
A	4.06	4.83
a	3°	7.5°
b	0.63	1.02
b1	1.14	1.52
C1	0.38	0.56
CP	3.71D	3.96D
D	14.22	15.062
E	9.78	10.54
e	2.29	2.79
e1	4.83	5.33
e3	1.14	1.40
F	1.14	1.40
H1	5.94	6.55
J1	2.29	2.92
L	13.716	14.22
Q	2.62	2.87
R	5.588	6.17

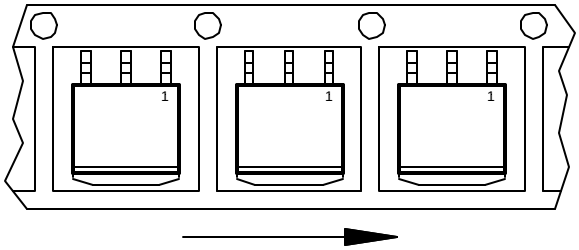
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
M	TO-263	3	50	750	Fig B
T	TO-220	3	50	---	---



Feed Direction
Figure A



Feed Direction
FigureB

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IRU1015-33

1.5A LOW DROPOUT POSITIVE FIXED 3.3V REGULATOR

FEATURES

- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Output Current Limiting
- Built-In Thermal Shutdown

APPLICATIONS

- Standard 3.3V Chip Set and Logic Applications

DESCRIPTION

The IRU1015-33 is a low dropout three terminal fixed 3.3V output regulator with minimum of 1.5A output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications requiring 3.3V output. The IRU1015-33 is guaranteed to have <1.3V dropout at full load current making it ideal to provide well regulated output with supply voltage as low as 4.6V input.

TYPICAL APPLICATION

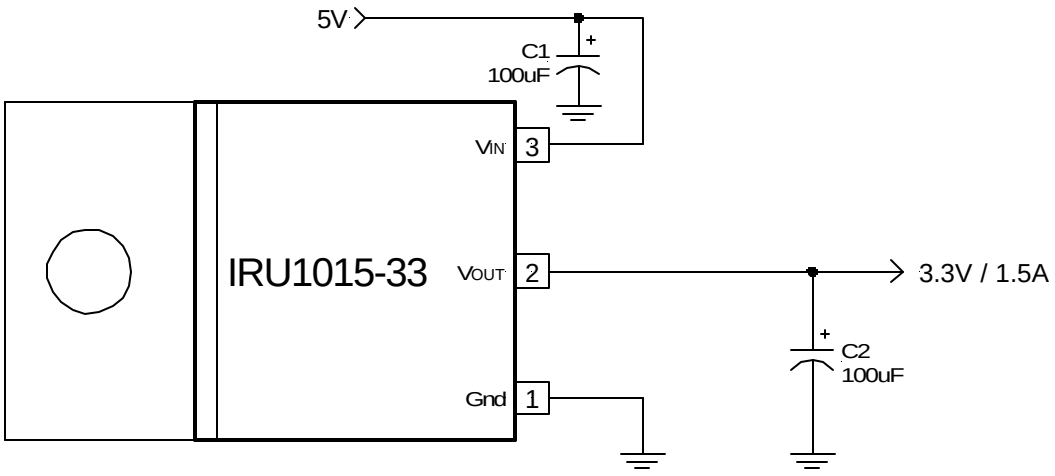


Figure 1 - Typical application of IRU1015-33.

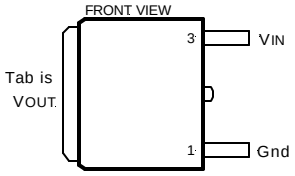
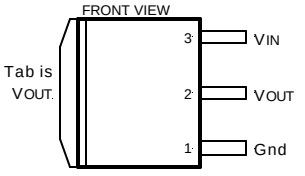
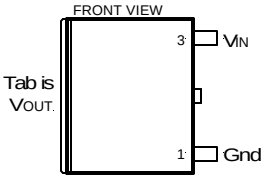
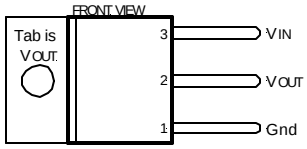
PACKAGE ORDER INFORMATION

T_J (°C)	2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC TO-263 (M)	2-PIN PLASTIC Ultra Thin-Pak™ (P)	3-PIN PLASTIC TO-220 (T)
0 To 150	IRU1015-33CD	IRU1015-33CM	IRU1015-33CP	IRU1015-33CT

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC TO-263 (M)	2-PIN PLASTIC ULTRA THIN-PAK™ (P)	3-PIN PLASTIC TO-220 (T)
			
θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=35°C/W for 1" Square pad	θ_{JA}=70°C/W for 1" Square pad	θ_{JT}=2.7°C/W θ_{JA}=60°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=10µF, and T_J=0 to 150°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	Vo	Io=10mA, T_J=25°C, V_{IN}=5V	3.267	3.300	3.333	V
		Io=10mA, V_{IN}=5V	3.234	3.300	3.366	
Line Regulation		Io=10mA, 4.7V<V_{IN}<7V			0.2	%
Load Regulation (Note 1)		V_{IN}=5V, V_{ADJ}=0, 10mA<Io<1.5A			0.4	%
Dropout Voltage (Note 2)	ΔVo	Note 2, Io=1.5A		1.1	1.3	V
Current Limit		V_{IN}=5V, ΔVo=100mV	1.6			A
Minimum Load Current (Note 3)		V_{IN}=5V		5	10	mA
Thermal Regulation		30ms Pulse, V_{IN}-Vo=3V, Io=1.5A		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum, Io=0.75A, V_{IN}-Vo=3V	60	70		dB
Adjust Pin Current Change		Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C		0.2	5	µA
Temperature Stability		V_{IN}=5V, V_{ADJ}=0V, Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%Vo

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor dividers are selected such that this current is automatically maintained.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	Gnd	This pin must be connected to ground plane using a low inductance short connection.
2	V_{OUT}	The output of the regulator. A minimum of 10μF capacitor must be connected from this pin to ground to insure stability.
3	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be 1.3V higher than V_{OUT} in order for the device to regulate properly.

BLOCK DIAGRAM

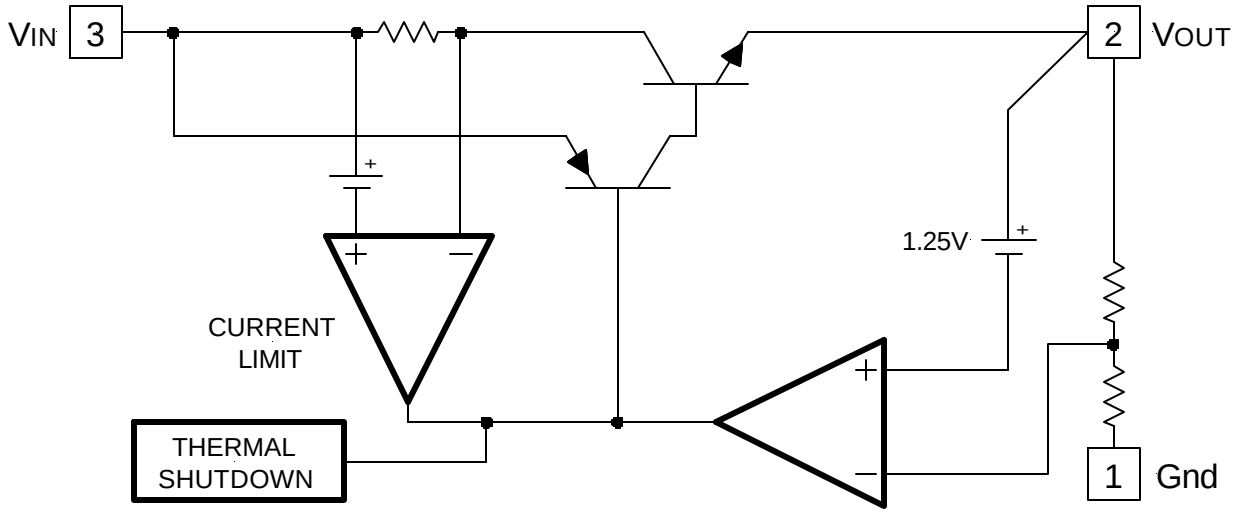


Figure 2 - Simplified block diagram of the IRU1015-33.

APPLICATION INFORMATION

Stability

The IRU1015-33 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for microprocessor applications use standard electrolytic capacitors with a typical ESR in the range of 50 to 100mΩ and an output capacitance of 500 to 1000μF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1015-33 takes advantage of this phenomena in making the overall regulator loop stable. For most applications a minimum of 100μF aluminum electrolytic capacitor such as Sanyo MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response.

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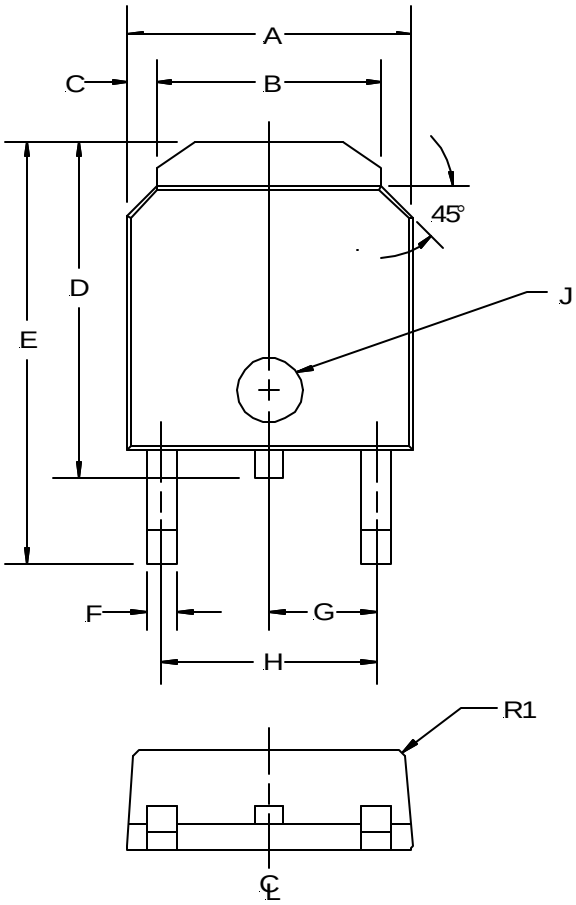
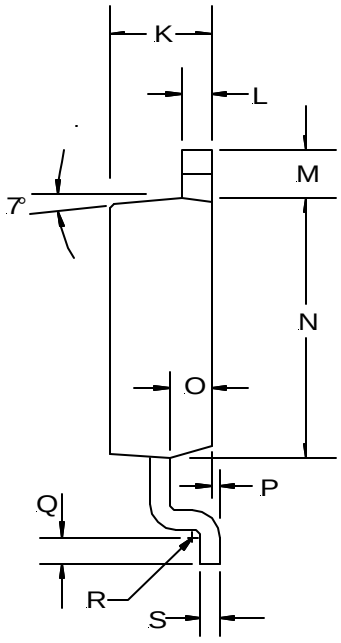
(D) TO-252 Package
2-Pin





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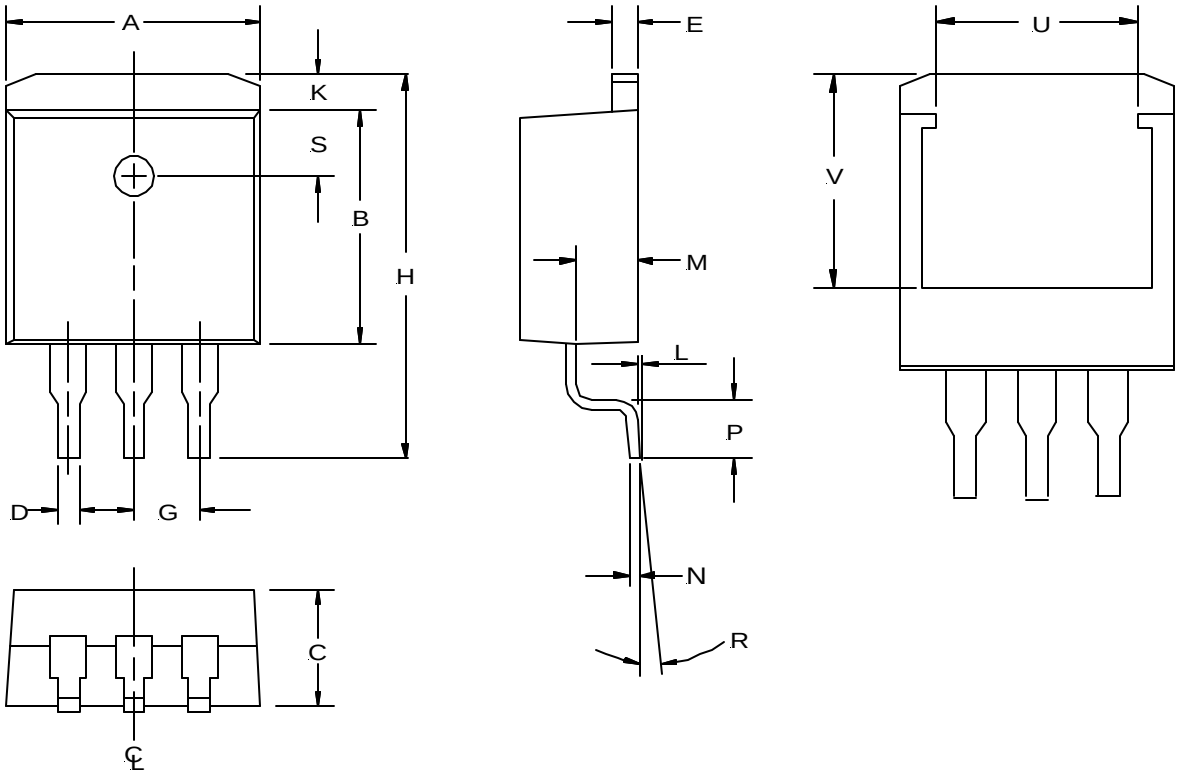
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

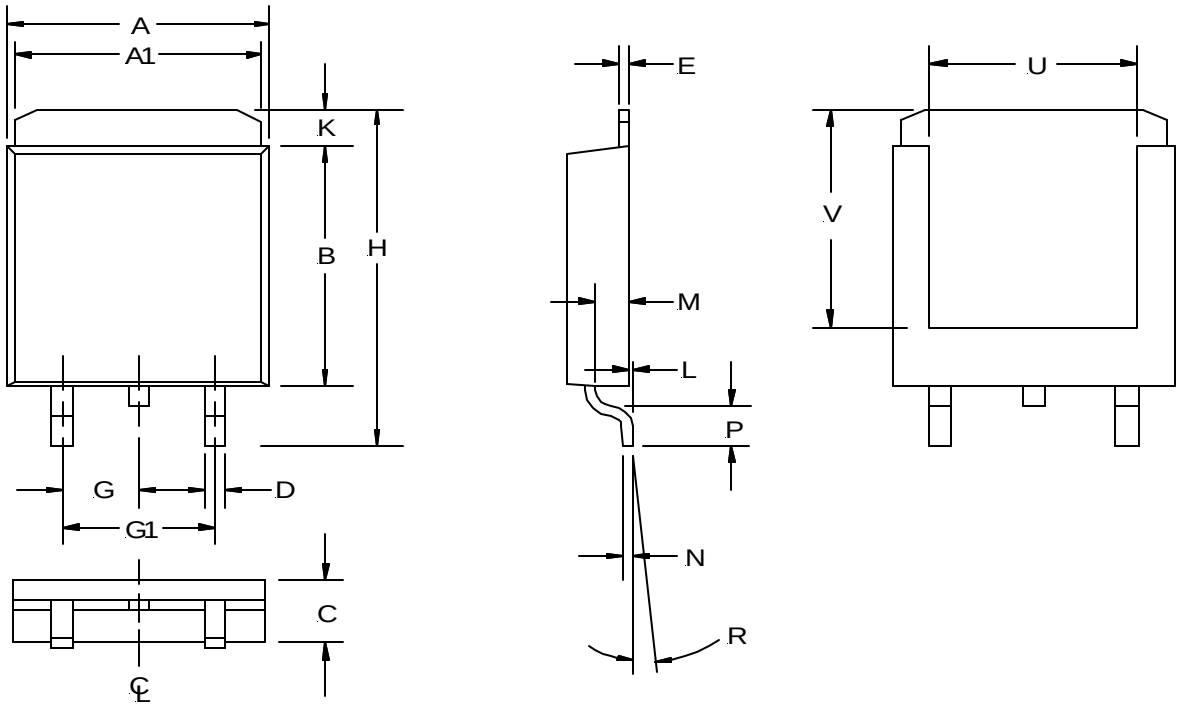
(M) TO-263 Package
3-Pin



SYMBOL	MIN	MAX
A	10.05	10.312
B	8.28	8.763
C	4.31	4.572
D	0.66	0.91
E	1.14	1.40
G	2.54 REF	
H	14.73	15.75
K	1.40	1.68
L	0.00	0.254
M	2.49	2.74
N	0.33	0.58
P	2.286	2.794
R	0°	8°
S	2.41	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

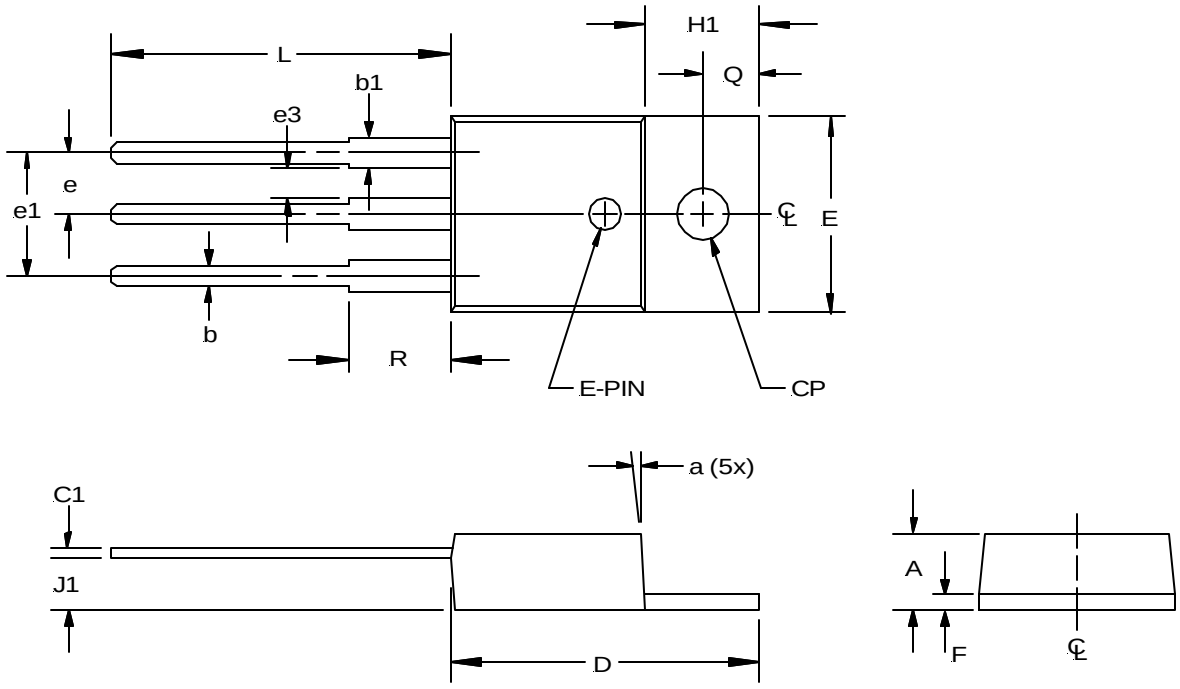
(P) Ultra Thin-Pak™
2-Pin



SYMBOL	MIN	MAX
A	5.91	6.17
A1	5.54	5.79
B	6.02	6.27
C	1.70	2.03
D	0.63	0.79
E	0.17	0.33
G	2.16	2.41
G1	4.45	4.70
H	9.42	9.68
K	0.76	1.27
L	0.02	0.13
M	0.89	1.14
N	0.25	0.25
P	0.94	1.19
R	2°	6°
U	2.92	3.30
V	5.08 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(T) TO-220 Package
3-Pin

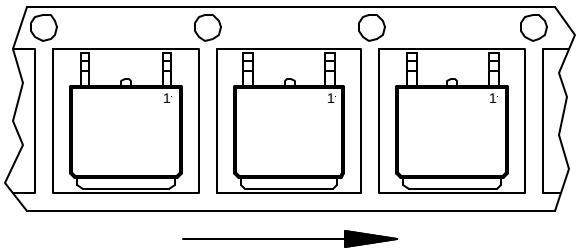


SYMBOL	MIN	MAX
A	4.06	4.83
a	3°	7.5°
b	0.63	1.02
b1	1.14	1.52
C1	0.38	0.56
CP	3.71D	3.96D
D	14.22	15.062
E	9.78	10.54
e	2.29	2.79
e1	4.83	5.33
e3	1.14	1.40
F	1.14	1.40
H1	5.94	6.55
J1	2.29	2.92
L	13.716	14.22
Q	2.62	2.87
R	5.588	6.17

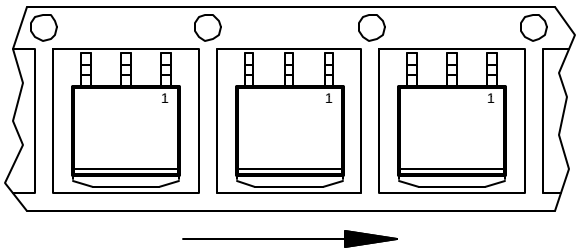
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

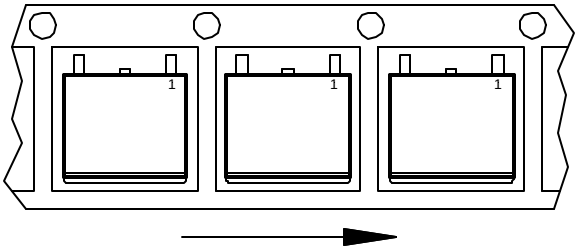
PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
M	TO-263	3	50	750	Fig B
P	Ultra Thin-Pak™	2	75	2500	Fig C
T	TO-220	3	50	---	---



Feed Direction
Figure A



Feed Direction
FigureB



Feed Direction
FigureC

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information

IRU1030

3A LOW DROPOUT POSITIVE ADJUSTABLE REGULATOR

FEATURES

- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Output Current Limiting
- Built-In Thermal Shutdown

APPLICATIONS

- Low Voltage Processor Applications such as: P54C™, P55C™, Cyrix M2™, POWER PC™, AMD
- GTL+ Termination PENTIUM PRO™, KLAMATH™
- Low Voltage Memory Termination Applications
- Standard 3.3V Chip Set and Logic Applications

DESCRIPTION

The IRU1030 is a low dropout three-terminal adjustable regulator with minimum of 3A output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications such as Pentium™ P54C™, P55C™ as well as GTL+ termination for Pentium Pro™ and Klamath™ processor applications. The IRU1030 is also well suited for other processors such as Cyrix™, AMD and Power PC™ applications. The IRU1030 is guaranteed to have <1.3V dropout at full load current making it ideal to provide well regulated outputs of 2.5V to 3.3V with 4.75V to 7V input supply.

TYPICAL APPLICATION

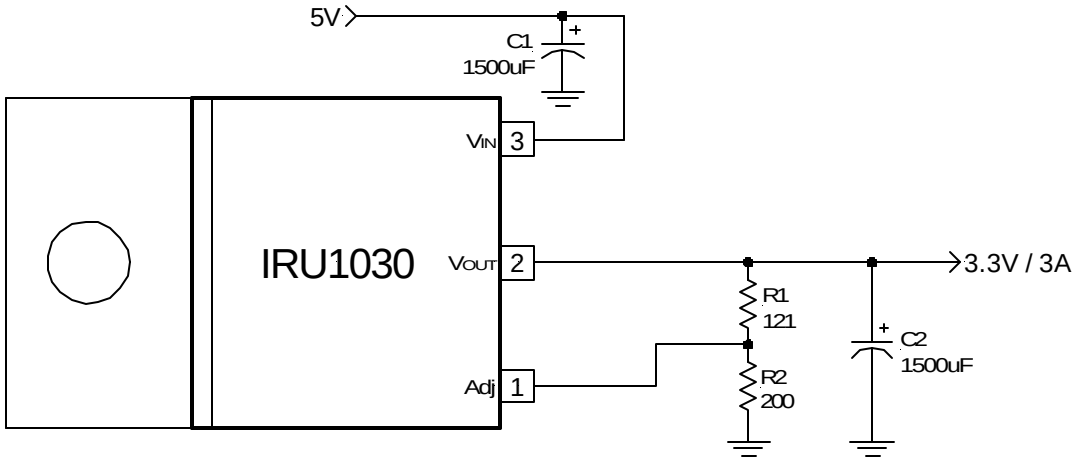


Figure 1 - Typical Application of IRU1030 in a 5V to 3.3V regulator.

Notes: Pentium P54C, P55C, Klamath, Pentium Pro, VRE are trademarks of Intel Corp.Cyrix M2 is trademark of Cyrix Corp. Power PC is trademark of IBM Corp.

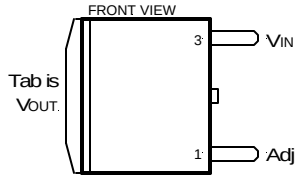
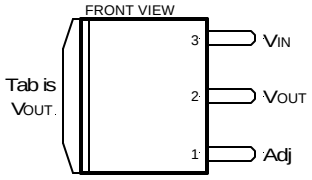
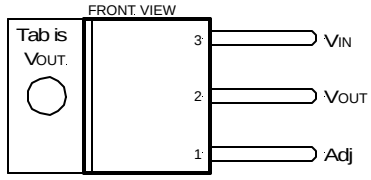
PACKAGE ORDER INFORMATION

T_J (°C)	2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC TO-263 (M)	3-PIN PLASTIC TO-220 (T)
0 To 150	IRU1030CD	IRU1030CM	IRU1030CT

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC TO-263 (M)	3-PIN PLASTIC TO-220 (T)
		
θ_{JA}=70°C/W for 0.5" Square pad	θ_{JA}=35°C/W for 1" Square pad	θ_{JT}=2.7°C/W θ_{JA}=60°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=10µF, and T_J=0 to 150°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	Io=10mA, T_J=25°C, (V_{IN}-Vo)=1.5V	1.238	1.250	1.262	V
		Io=10mA, (V_{IN}-Vo)=1.5V	1.225	1.250	1.275	
Line Regulation		Io=10mA, 1.3V<(V_{IN}-Vo)<7V			0.2	%
Load Regulation (Note 1)		V_{IN}=3.3V, V_{ADJ}=0, 10mA<Io<3A			0.4	%
Dropout Voltage (Note 2)	ΔV_O	Note 2, Io=3A		1.1	1.3	V
Current Limit		V_{IN}=3.3V, ΔVo=100mV	3.1			A
Minimum Load Current (Note 3)		V_{IN}=3.3V, V_{ADJ}=0V		5	10	mA
Thermal Regulation		30ms Pulse, V_{IN}-Vo=3V, Io=3A		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum,				
		Io=1.5A, V_{IN}-Vo=3V	60	70		dB
Adjust Pin Current	I_{ADJ}	Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C,				
		Io=10mA, V_{IN}-Vo=1.5V		55	120	µA
Adjust Pin Current Change		Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C		0.2	5	µA
Temperature Stability		V_{IN}=3.3V, V_{ADJ}=0V, Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%V_O

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor dividers are selected such that this current is automatically maintained.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	Adj	A resistor divider from V_{OUT} to Adj pin to ground sets the output voltage.
2	V_{OUT}	The output of the regulator. A minimum of 10µF capacitor must be connected from this pin to ground to insure stability.
3	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be 1.3V higher than V_{OUT} in order for the device to regulate properly.

BLOCK DIAGRAM

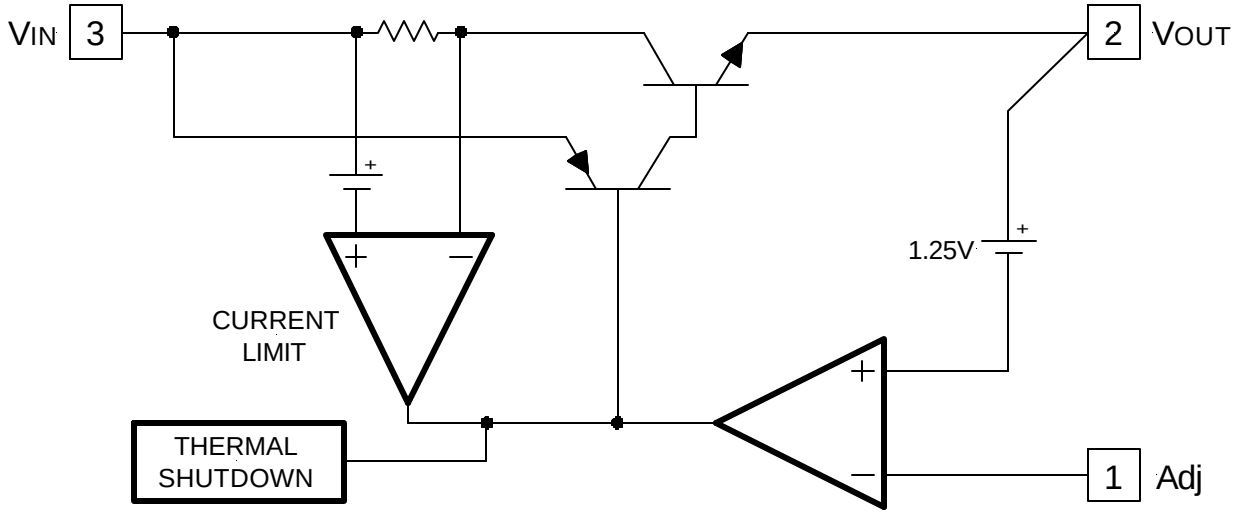


Figure 2 - Simplified block diagram of the IRU1030.

APPLICATION INFORMATION

Introduction

The IRU1030 adjustable Low Dropout (LDO) regulator is a three-terminal device which can easily be programmed with the addition of two external resistors to any voltages within the range of 1.25 to 5.5V. This regulator unlike the first generation of the three-terminal regulators such as LM117 that required 3V differential between the input and the regulated output, only needs 1.3V differential to maintain output regulation. This is a key requirement for today's microprocessors that need typically 3.3V supply and are often generated from the 5V supply. Another major requirement of these microprocessors such as the Intel P54C™ is the need to switch the load current from zero to several amps in tens of nanoseconds at the processor pins, which translates to an approximately 300 to 500ns current step at the regulator. In addition, the output voltage tolerances are also extremely tight and they include the transient response as part of the specification. For example Intel VRE™ specification calls for a total of ±100mV including initial tolerance, load regulation and 0 to 4.6A load step.

The IRU1030 is specifically designed to meet the fast current transient needs as well as providing an accurate initial voltage, reducing the overall system cost with the need for fewer output capacitors.

Output Voltage Setting

The IRU1030 can be programmed to any voltages in the range of 1.25V to 5.5V with the addition of R1 and R2 external resistors according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) + I_{ADJ} \times R2$$

Where:
V_{REF} = 1.25V Typically
I_{ADJ} = 50µA Typically
R1 and R2 as shown in Figure 3:

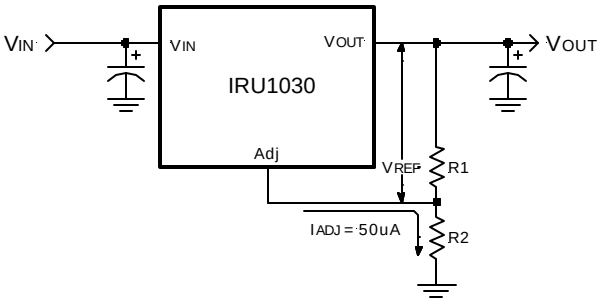


Figure 3 - Typical application of the IRU1030 for programming the output voltage.

The IRU1030 keeps a constant 1.25V between the output pin and the adjust pin. By placing a resistor R1 across these two pins a constant current flows through R1, adding to the I_{ADJ} current and into the R2 resistor producing a voltage equal to the $(1.25/R1) \times R2 + I_{ADJ} \times R2$ which will be added to the 1.25V to set the output voltage. This is summarized in the above equation. Since the minimum load current requirement of the IRU1030 is 10mA, R1 is typically selected to be 121Ω resistor so that it automatically satisfies the minimum current requirement. Notice that since I_{ADJ} is typically in the range of 50µA it only adds a small error to the output voltage and should only be considered when a very precise output voltage setting is required. For example, in a typical 3.3V application where R1=121Ω and R2=200Ω the error due to I_{ADJ} is only 0.3% of the nominal set point.

Load Regulation

Since the IRU1030 is only a three-terminal device, it is not possible to provide true remote sensing of the output voltage at the load. Figure 4 shows that the best load regulation is achieved when the bottom side of R2 is connected to the load and the top side of R1 resistor is connected directly to the case or the V_{OUT} pin of the regulator and not to the load. In fact, if R1 is connected to the load side, the effective resistance between the regulator and the load is gained up by the factor of (1+R2/R1), or the effective resistance will be $R_{P(eff)} = R_P \times (1+R2/R1)$. It is important to note that for high current applications, this can represent a significant percentage of the overall load regulation and one must keep the path from the regulator to the load as short as possible to minimize this effect.

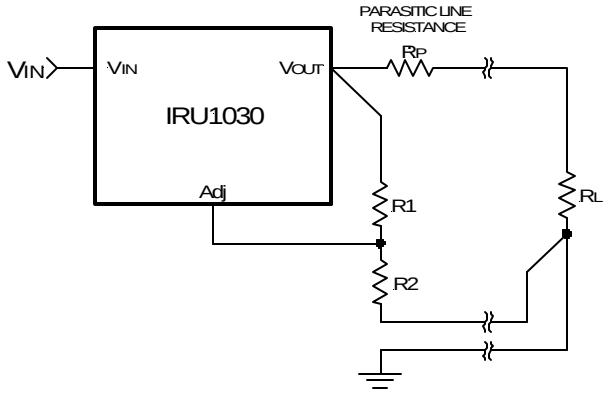


Figure 4 - Schematic showing connection for best load regulation.

Stability

The IRU1030 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for microprocessor applications use standard electrolytic capacitors with a typical ESR in the range of 50 to 100mΩ and an output capacitance of 500 to 1000µF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1030 takes advantage of this phenomena in making the overall regulator loop stable. For most applications a minimum of 100µF aluminum electrolytic capacitor such as Sanyo MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response.

Thermal Design

The IRU1030 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the maximum allowable junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. The example below shows the steps in selecting the proper regulator heat sink for the GTL+ terminator using a separate regulator for each end.

Assuming the following specifications:

V_{IN} = 3.3V
V_{OUT} = 1.5V
$I_{OUT(MAX)}$ = 2.7A
T_A = 35°C

The steps for selecting a proper heat sink to keep the junction temperature below 135°C is given as:

1) Calculate the maximum power dissipation using:

$P_D = I_{OUT} \times (V_{IN} - V_{OUT})$

$P_D = 2.7 \times (3.3 - 1.5) = 4.86W$

2) Select a package from the regulator data sheet and record its junction to case (or tab) thermal resistance.

Selecting TO-220 package gives us:

θ_{JC} = 2.7°C/W

3) Assuming that the heat sink is black anodized, calculate the maximum heat sink temperature allowed:

Assume, θcs=0.05°C/W (heat-sink-to-case thermal resistance for black anodized)

$T_S = T_J - P_D \times (\theta_{JC} + \theta_{CS})$

$T_S = 135 - 4.86 \times (2.7 + 0.05) = 121.7°C$

4) With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance (θ_{SA}) is calculated by first calculating the temperature rise above the ambient as follows:

$\Delta T = T_S - T_A = 121.7 - 35 = 86.7°C$

ΔT=Temperature Rise Above Ambient

$$\theta_{SA} = \frac{\Delta T}{P_D} = \frac{86.7}{4.86} = 17.8°C/W$$

5) Next, a heat sink with lower θ_{SA} than the one calculated in step 4 must be selected. One way to do this is to simply look at the graphs of the "Heat Sink Temp Rise Above the Ambient" vs. the "Power Dissipation" and select a heat sink that results in lower temperature rise than the one calculated in the previous step. The following heat sinks from AAVID and Thermalloy meet this criteria.

	Air Flow (LFM)			
	0	**100**	**200**	**300**
Thermalloy	6109PB	6110PB	7141	7178
AAVID	575002	507302	576802B	577102

Note: For further information regarding the above companies and their latest product offerings and application support contact your local representative or the numbers listed below:

AAVID.....PH# (603) 528 3400
Thermalloy.....PH# (214) 243-4321

Designing for Microprocessor Applications

As it was mentioned before the IRU1030 is designed specifically to provide power for the new generation of the low voltage processors requiring voltages in the range of 2.5V to 3.6V generated by stepping down the 5V supply. These processors demand a fast regulator that supports their large load current changes. The worst case current step seen by the regulator is anywhere in the range of 1 to 7A with the slew rate of 300 to 500ns which could happen when the processor transitions from "Stop Clock" mode to the "Full Active" mode. The load current step at the processor is actually much faster, in the order of 15 to 20ns, however the decoupling capacitors placed in the cavity of the processor socket handle this transition until the regulator responds to the load current levels. Because of this requirement the selection of high frequency low ESR and low ESL output capacitors is imperative in the design of these regulator circuits.

Figure 5 shows the effects of a fast transient on the output voltage of the regulator. As shown in this figure, the ESR of the output capacitor produces an instantaneous drop equal to the ($\Delta V_{ESR} = ESR \times \Delta I$) and the ESL effect will be equal to the rate of change of the output current times the inductance of the capacitor. ($\Delta V_{ESL} = L \times \Delta I/\Delta t$). The output capacitance effect is a droop in the output voltage proportional to the time it takes for the regulator to respond to the change in the current, ($\Delta Vc = \Delta t \times \Delta I/C$) where Δt is the response time of the regulator.

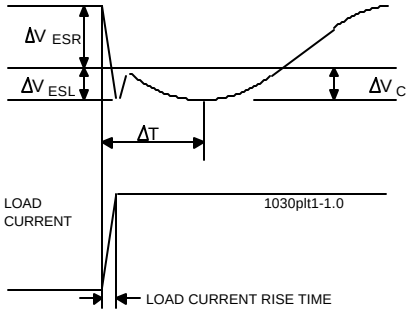


Figure 5 - Typical regulator response to the fast load current step.

An example of a regulator design to meet the Intel Pentium Pro GTL+ specification is given below.

Assume the specification for the processor as shown in Table 1:

Type of Processor	V_{OUT} Nominal	I_{MAX}	Max Allowed Output Tolerance
Pentium Pro	1.50 V	2.7 A	±150 mV

Table 1 - GTL+ Specification for Pentium Pro

The first step is to select the voltage step allowed in the output due to the output capacitor's ESR:

1) Assuming the regulator's initial accuracy plus the resistor divider tolerance is ≈ ±30mV (±2% of 1.5V nominal), then the total step allowed for the ESR and the ESL, is –120 mV.

Assuming that the ESL drop is –10mV, the remaining ESR step will be –110mV. Therefore the output capacitor ESR must be:

$$ESR \leq \frac{110}{2.7} = 40m\Omega$$

The Sanyo MVGX series is a good choice to achieve both price and performance goals. The 6MV1500GX, 1500μF, 6.3V has an ESR of less than 36mΩ typ. Selecting a single capacitor achieves our design goal.

The next step is to calculate the drop due to the capacitance discharge and make sure that this drop in voltage is less than the selected ESL drop in the previous step.

2) With the output capacitance being 1500μF:

$$\Delta Vc = \frac{\Delta t \times \Delta I}{C} = \frac{2 \times 2.7}{1500} = 3.6mV$$

Where:
$\Delta t = 2\mu s$ is the regulator response time

To set the output DC voltage, we need to select R1 and R2:

3) Assuming R1 = 121Ω, 0.5%:

$$R2 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R1 = \left(\frac{1.5}{1.25} - 1\right) \times 121 = 24.2\Omega$$

Select R2 = 24.3Ω, 0.5%

Selecting both R1 and R2 resistors to be 0.5% tolerance, results in the least amount of error introduced by the resistor dividers leaving ≈ ±1.3% error budget for the IRU1030 reference which is within the initial accuracy of the device.

Finally, the input capacitor is selected as follows:

4) Assuming that the input voltage can drop 150mV before the main power supply responds, and that the main power supply response time is ≈ 50μs, then the minimum input capacitance for a 2.7A load step is given by:

$$C_{IN} = \frac{2.7 \times 50}{0.15} = 900\mu F$$

The ESR should be less than:

$$ESR = \frac{(V_{IN} - V_{OUT} - \Delta V - V_{DROP})}{\Delta I}$$

Where:
V_{DROP} **L** Input voltage drop allowed in step 4
ΔV **L** Maximum regulator dropout voltage
ΔI **L** Load current step

$$ESR = \frac{(3.3 - 1.5 - 1.2 - 0.15)}{2.7} = 0.16\Omega$$

Selecting a single 1500μF the same type as the output capacitors exceeds our requirements. However, the same input capacitor can also support the second regulator for the other end of termination.

Figure 6 shows the completed schematic for our example.

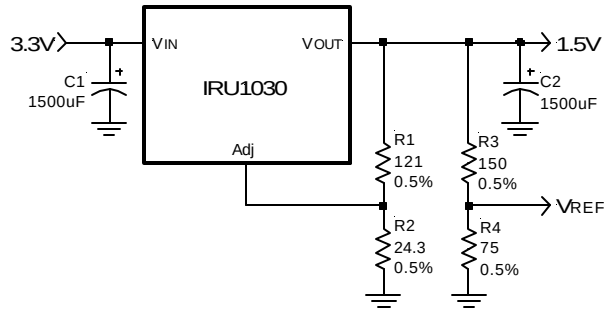


Figure 6 - Final schematic for half of the GTL+ termination regulator.

Layout Consideration

The output capacitors must be located as close to the V_{OUT} terminal of the device as possible. It is recommended to use a section of a layer of the PC board as a plane to connect the V_{OUT} pin to the output capacitors to prevent any high frequency oscillation that may result due to excessive trace inductance.

International
IOR Rectifier

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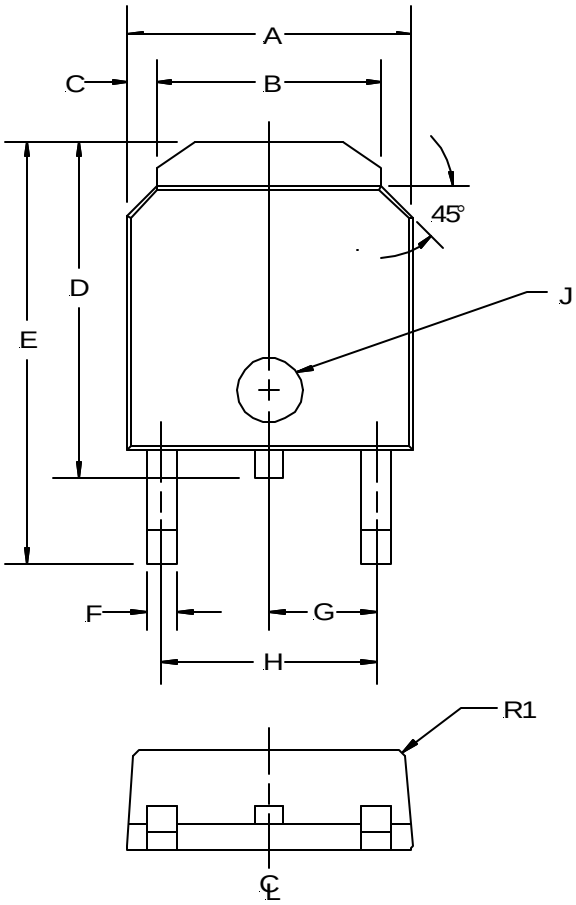
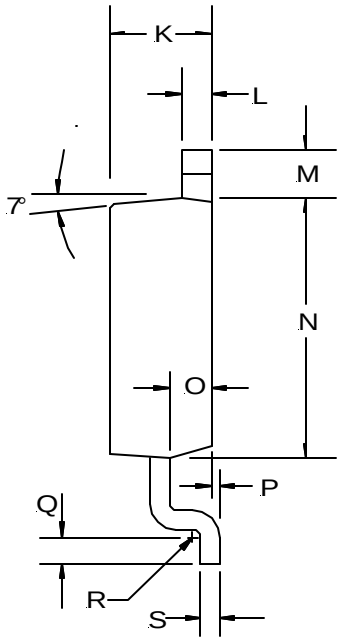
(D) TO-252 Package
2-Pin

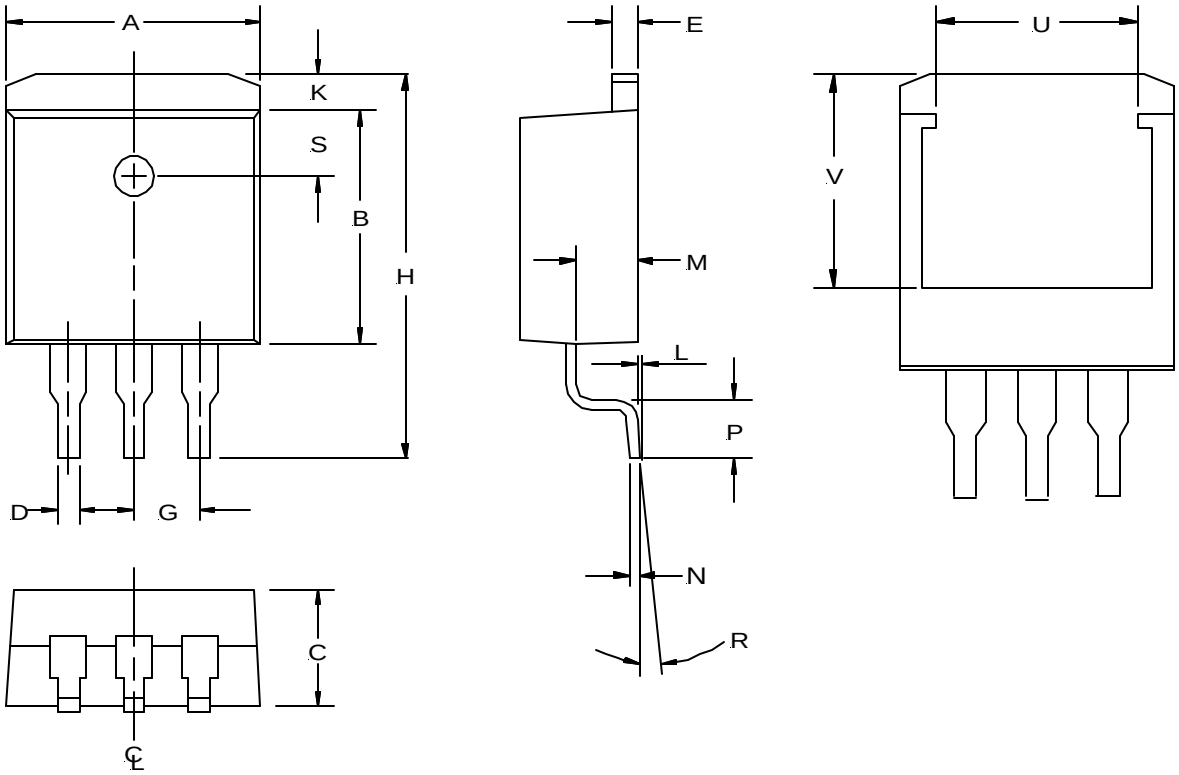




SYMBOL	MIN	MAX
A	6.477	6.731
B	5.004	5.207
C	0.686	0.838
D	7.417	8.179
E	9.703	10.084
F	0.635	0.889
G	2.286 BSC	
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

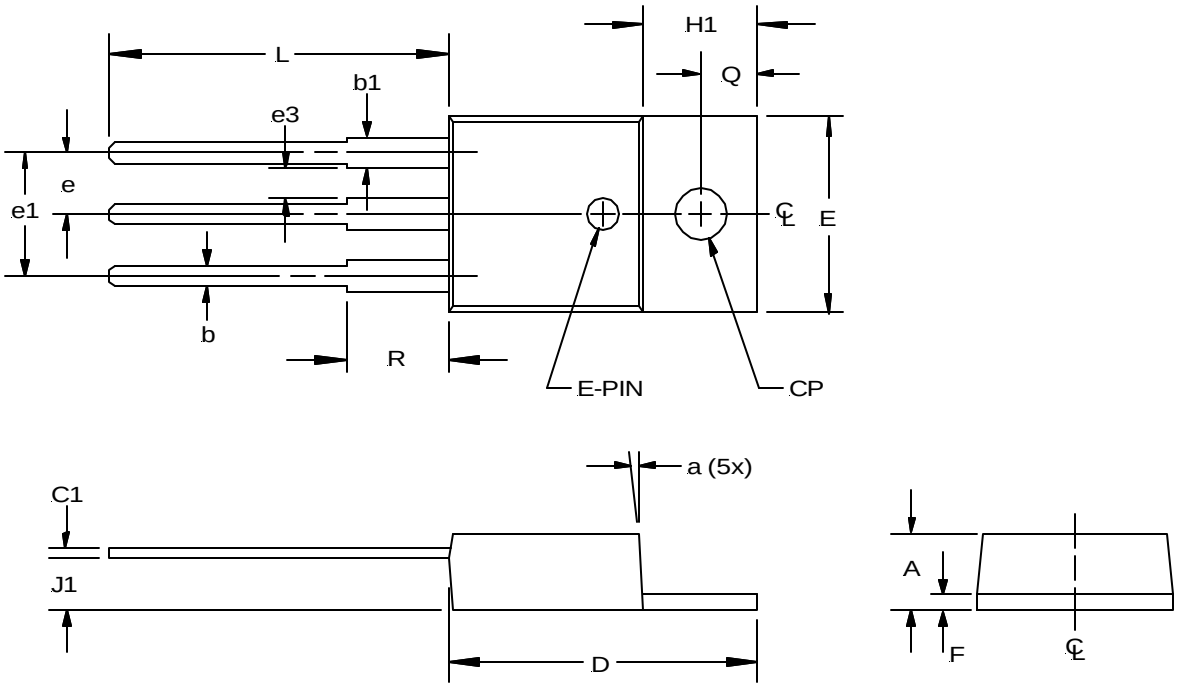
(M) TO-263 Package
3-Pin



SYMBOL	MIN	MAX
A	10.05	10.312
B	8.28	8.763
C	4.31	4.572
D	0.66	0.91
E	1.14	1.40
G	2.54 REF	
H	14.73	15.75
K	1.40	1.68
L	0.00	0.254
M	2.49	2.74
N	0.33	0.58
P	2.286	2.794
R	0°	8°
S	2.41	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(T) TO-220 Package
3-Pin

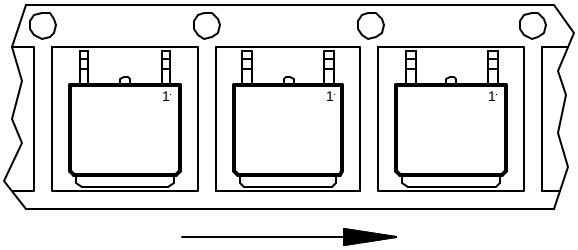


SYMBOL	MIN	MAX
A	4.06	4.83
a	3°	7.5°
b	0.63	1.02
b1	1.14	1.52
C1	0.38	0.56
CP	3.71D	3.96D
D	14.22	15.062
E	9.78	10.54
e	2.29	2.79
e1	4.83	5.33
e3	1.14	1.40
F	1.14	1.40
H1	5.94	6.55
J1	2.29	2.92
L	13.716	14.22
Q	2.62	2.87
R	5.588	6.17

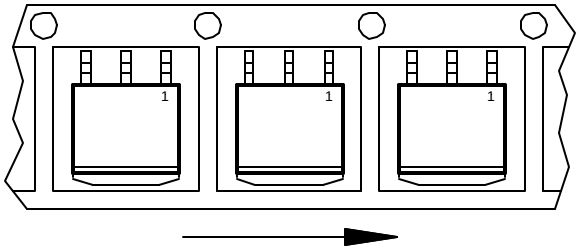
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
M	TO-263	3	50	750	Fig B
T	TO-220	3	50	---	---



Feed Direction
Figure A



Feed Direction
FigureB

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IRU1030-33

3A LOW DROPOUT POSITIVE FIXED 3.3V REGULATOR

FEATURES

- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Output Current Limiting
- Built-In Thermal Shutdown

APPLICATIONS

- Standard 3.3V Chip Set and Logic Applications

DESCRIPTION

The IRU1030-33 is a low dropout three-terminal fixed 3.3V output regulator with minimum of 3A output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications requiring 3.3V output. The IRU1030-33 is guaranteed to have <1.3V dropout at full load current making it ideal to provide well regulated output with supply voltage as low as 4.6V input.

TYPICAL APPLICATION

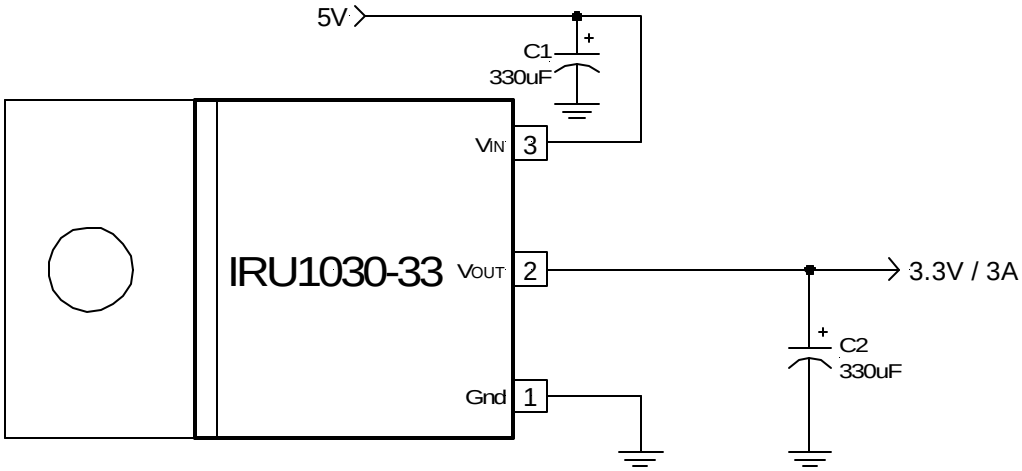


Figure 1 - Typical application of IRU1030-33.

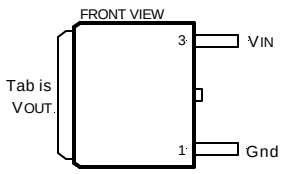
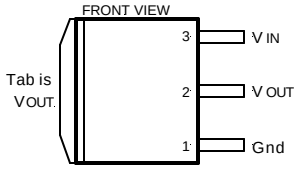
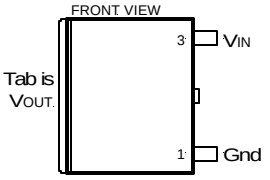
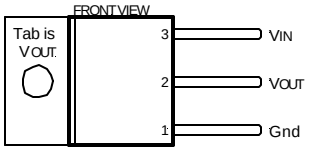
TYPICAL APPLICATION

T_J (°C)	2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC TO-263 (M)	2-PIN PLASTIC Ultra Thin-Pak™ (P)	3-PIN PLASTIC TO-220 (T)
0 To 150	IRU1030-33CD	IRU1030-33CM	IRU1030-33CP	IRU1030-33CT

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC TO-263 (M)	2-PIN PLASTIC ULTRA THIN-PAK™ (P)	3-PIN PLASTIC TO-220 (T)
			
θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=35°C/W for 1" Square pad	θ_{JA}=70°C/W for 1" Square pad	θ_{JT}=2.7°C/W θ_{JA}=60°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=10µF, and T_J=0 to 150°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	V_O	Io=10mA,T_J=25°C,V_{IN}=5V	3.267	3.300	3.333	V
		Io=10mA, V_{IN}=5V	3.234	3.300	3.366	
Line Regulation		Io=10mA, 4.7V<V_{IN}<7V			0.2	%
Load Regulation (Note 1)		V_{IN}=5V, V_{ADJ}=0, 10mA<Io<3A			0.4	%
Dropout Voltage (Note 2)	ΔV_O	Note 2, Io=3A		1.1	1.3	V
Current Limit		V_{IN}=5V, ΔVo=100mV	3.1			A
Minimum Load Current (Note 3)		V_{IN}=5V		5	10	mA
Thermal Regulation		30ms Pulse, V_{IN}-Vo=3V, Io=3A		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum, Io=1.5A, V_{IN}-Vo=3V	60	70		dB
Adjust Pin Current Change		Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C		0.2	5	µA
Temperature Stability		V_{IN}=5V, V_{ADJ}=0V,Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%V_O

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor dividers are selected such that it automatically maintains this current.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	Gnd	This pin must be connected to ground plane using a low inductance short connection.
2	V_{OUT}	The output of the regulator. A minimum of 10µF capacitor must be connected from this pin to ground to insure stability.
3	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be 1.3V higher than V_{OUT} in order for the device to regulate properly.

BLOCK DIAGRAM

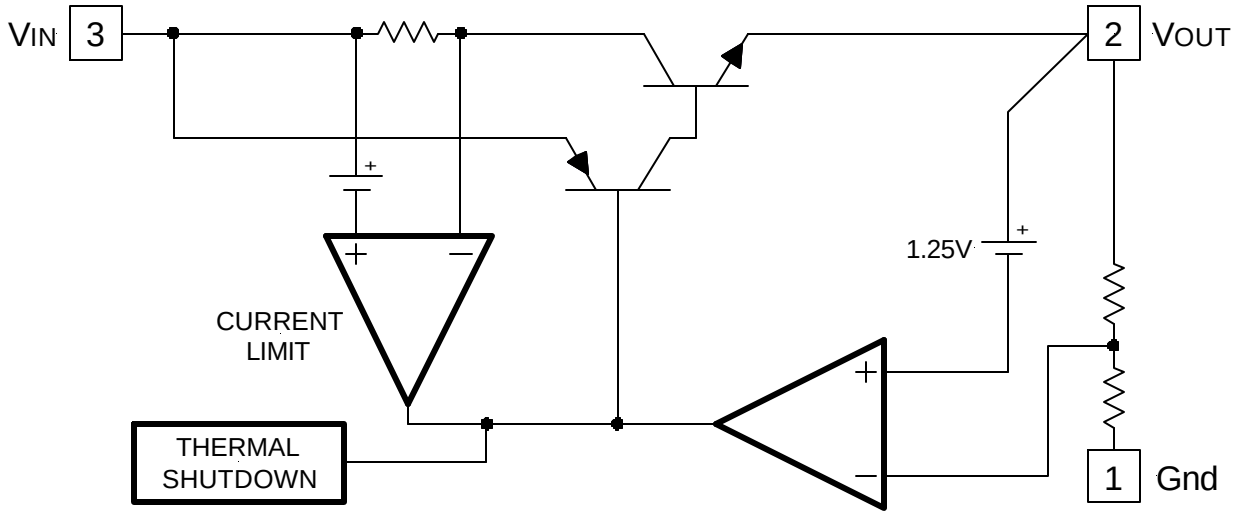


Figure 2 - Simplified block diagram of the IRU1030-33.

APPLICATION INFORMATION

Stability

The IRU1030-33 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for microprocessor applications use standard electrolytic capacitors with a typical ESR in the range of 50 to 100mΩ and an output capacitance of 500 to 1000µF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1030-33 takes advantage of this phenomena in making the overall regulator loop stable. For most applications a minimum of 100µF aluminum electrolytic capacitor such as Sanyo MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response.

International
IOR Rectifier

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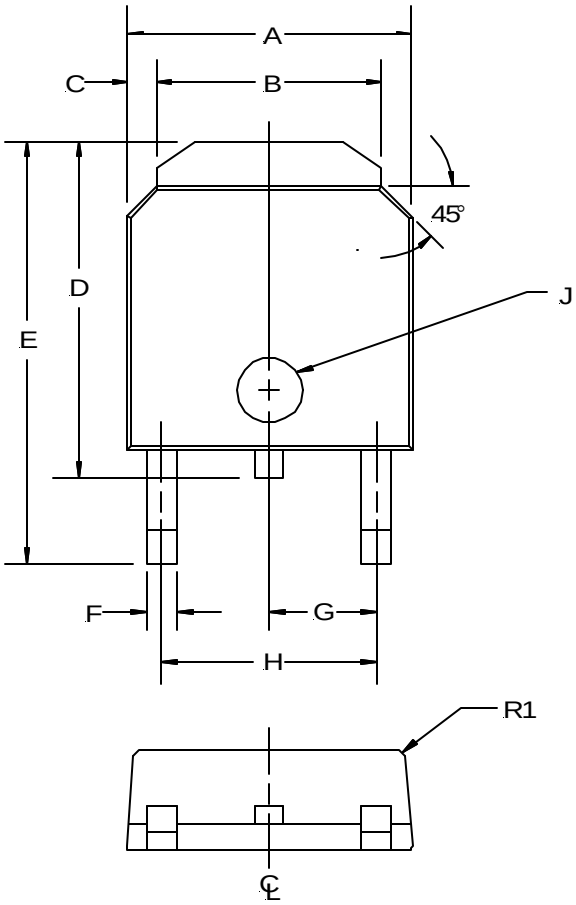
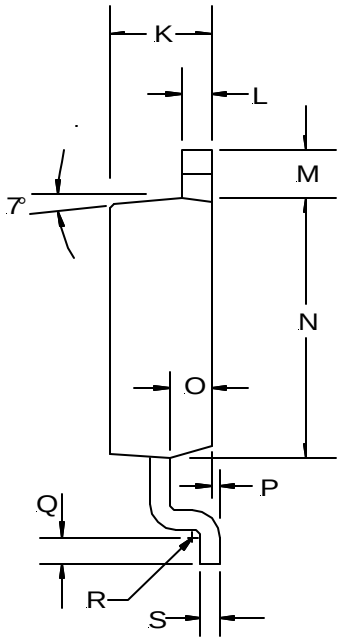
(D) TO-252 Package
2-Pin

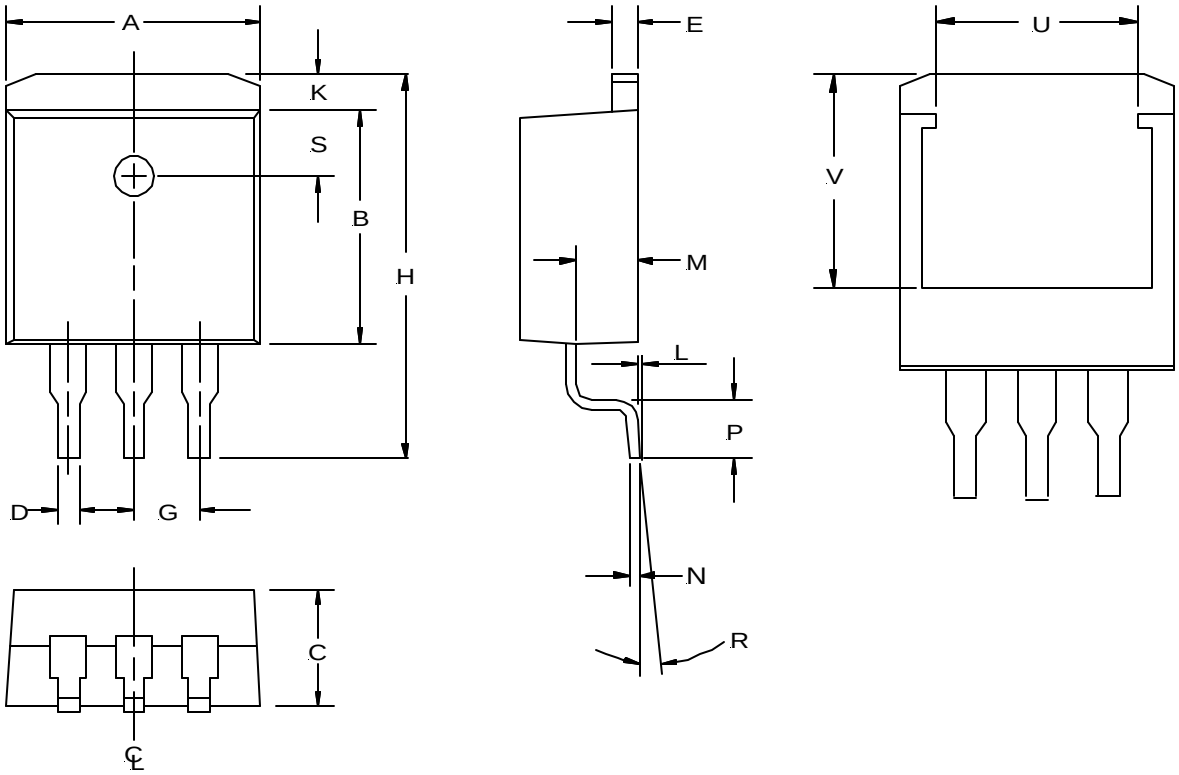




SYMBOL	MIN	MAX
A	6.477	6.731
B	5.004	5.207
C	0.686	0.838
D	7.417	8.179
E	9.703	10.084
F	0.635	0.889
G	2.286 BSC	
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

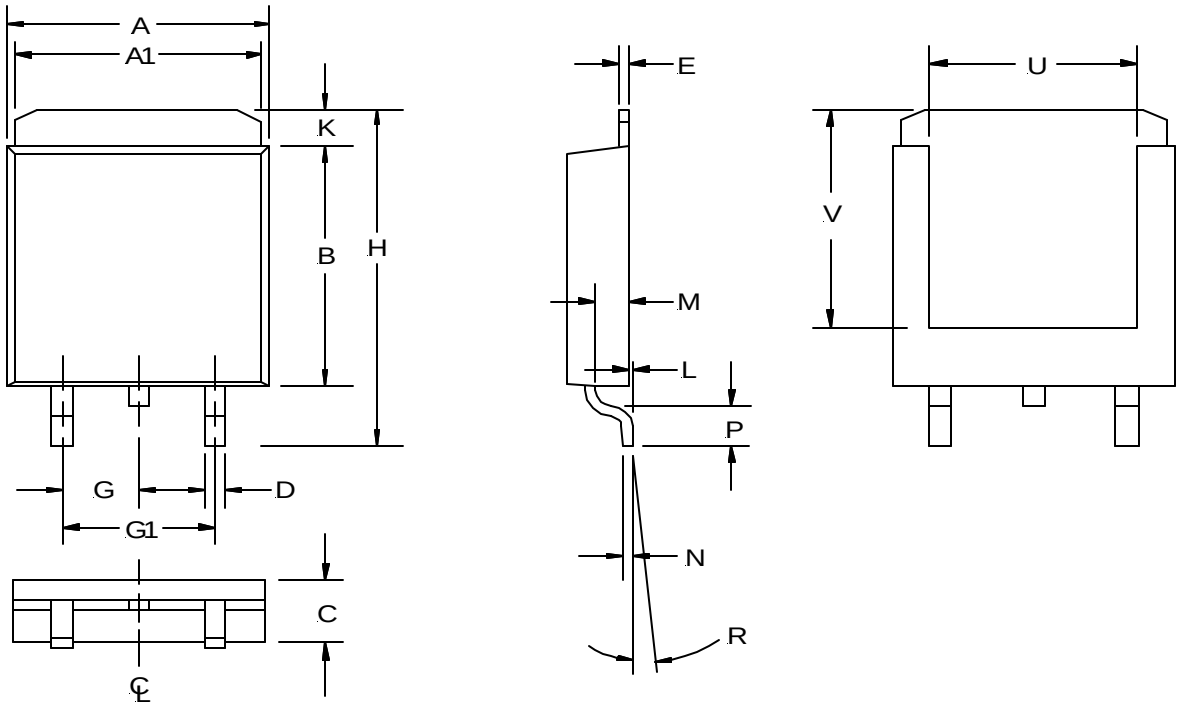
(M) TO-263 Package
3-Pin



SYMBOL	MIN	MAX
A	10.05	10.312
B	8.28	8.763
C	4.31	4.572
D	0.66	0.91
E	1.14	1.40
G	2.54 REF	
H	14.73	15.75
K	1.40	1.68
L	0.00	0.254
M	2.49	2.74
N	0.33	0.58
P	2.286	2.794
R	0°	8°
S	2.41	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

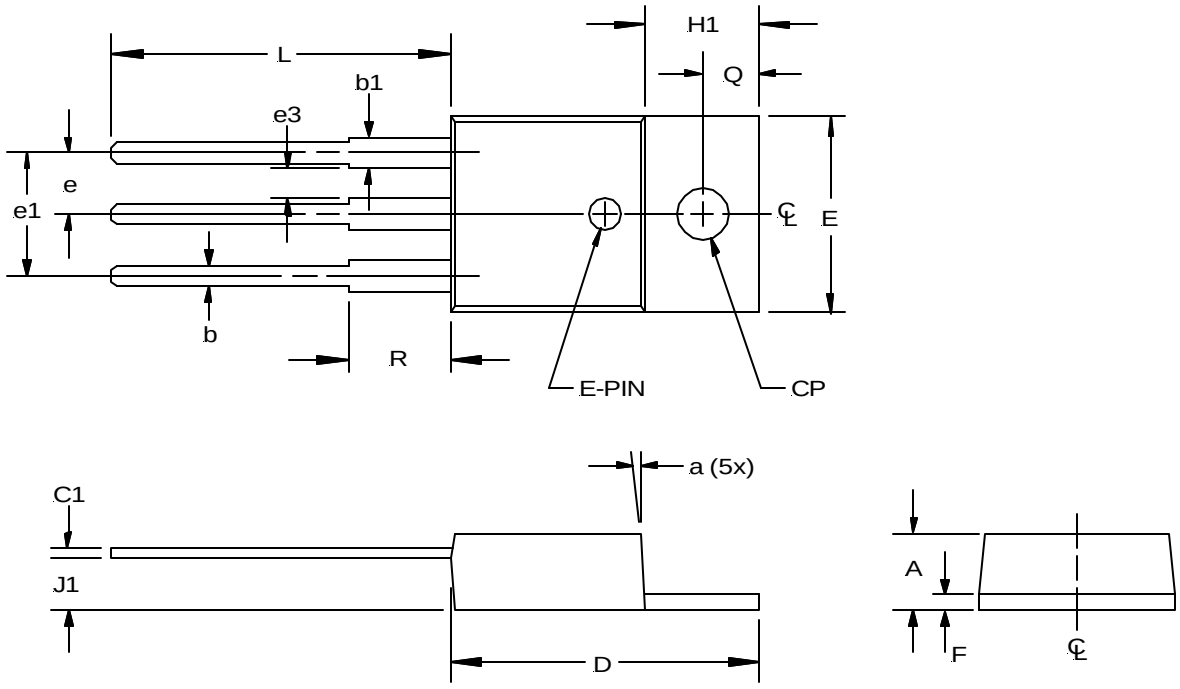
(P) Ultra Thin-Pak™
2-Pin



SYMBOL	MIN	MAX
A	5.91	6.17
A1	5.54	5.79
B	6.02	6.27
C	1.70	2.03
D	0.63	0.79
E	0.17	0.33
G	2.16	2.41
G1	4.45	4.70
H	9.42	9.68
K	0.76	1.27
L	0.02	0.13
M	0.89	1.14
N	0.25	0.25
P	0.94	1.19
R	2°	6°
U	2.92	3.30
V	5.08 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(T) TO-220 Package
3-Pin

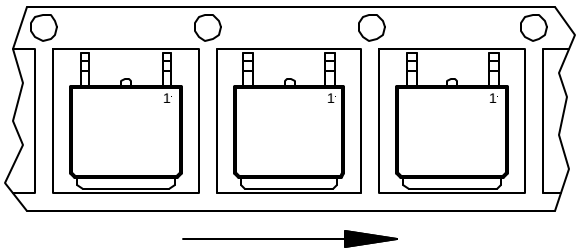


SYMBOL	MIN	MAX
A	4.06	4.83
a	3°	7.5°
b	0.63	1.02
b1	1.14	1.52
C1	0.38	0.56
CP	3.71D	3.96D
D	14.22	15.062
E	9.78	10.54
e	2.29	2.79
e1	4.83	5.33
e3	1.14	1.40
F	1.14	1.40
H1	5.94	6.55
J1	2.29	2.92
L	13.716	14.22
Q	2.62	2.87
R	5.588	6.17

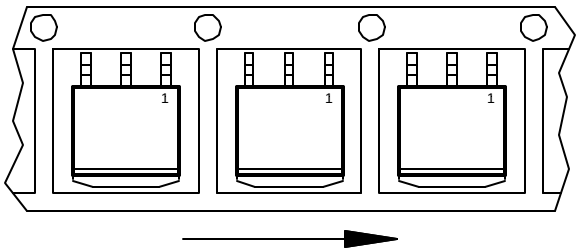
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

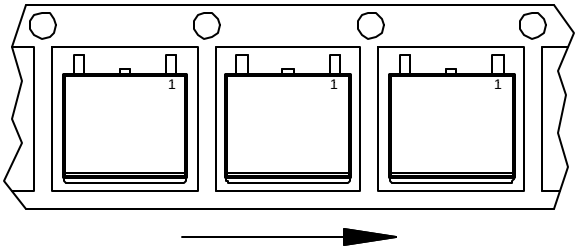
PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
M	TO-263	3	50	750	Fig B
P	Ultra Thin-Pak™	2	75	2500	Fig C
T	TO-220	3	50	---	---



Feed Direction
Figure A



Feed Direction
FigureB



Feed Direction
FigureC

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IRU1050

5A LOW DROPOUT POSITIVE ADJUSTABLE REGULATOR

FEATURES

- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Output Current Limiting
- Built-In Thermal Shutdown

APPLICATIONS

- Low Voltage Processor Applications such as: P54C™, P55C™, Cyrix M2™, POWER PC™, AMD
- GTL+ Termination PENTIUM PRO™, KLAMATH™
- Low Voltage Memory Termination Applications
- Standard 3.3V Chip Set and Logic Applications

DESCRIPTION

The IRU1050 is a low dropout three-terminal adjustable regulator with minimum of 5A output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications such as Pentium™ P54C™,P55C™ as well as GTL+ termination for Pentium Pro™ and Klamath™ processor applications. The IRU1050 is also well suited for other processors such as Cyrix™, AMD and Power PC™ applications. The IRU1050 is guaranteed to have <1.3V dropout at full load current making it ideal to provide well regulated outputs of 2.5V to 3.3V with 4.75V to 7V input supply.

TYPICAL APPLICATION

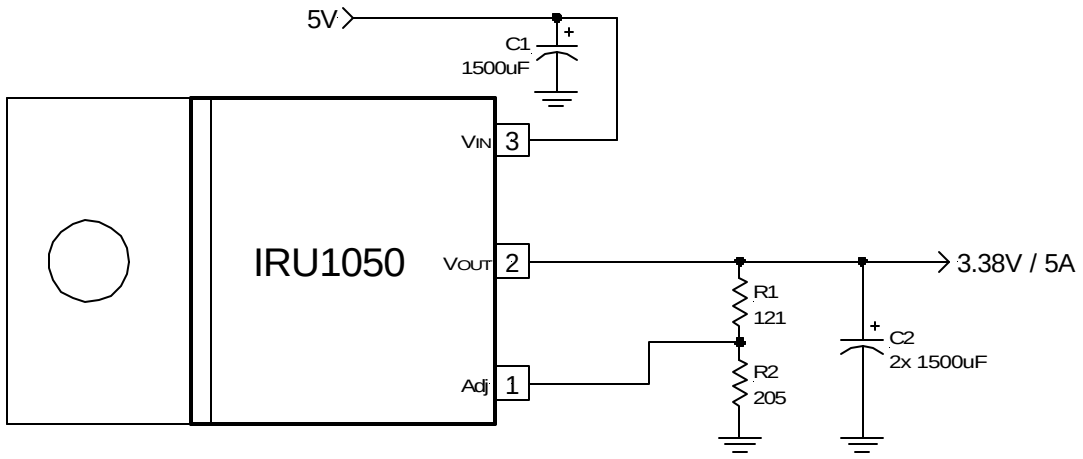


Figure 1 - Typical Application of IRU1050 in a 5V to 3.38V regulator designed to meet the Intel P54C ™ processors.

Notes: Pentium P54C, P55C, Klamath, Pentium Pro,VRE are trademarks of Intel Corp. Cyrix M2 is trademark of Cyrix Corp. Power PC is trademark of IBM Corp.

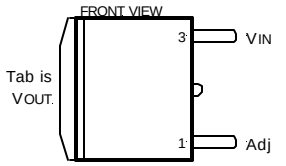
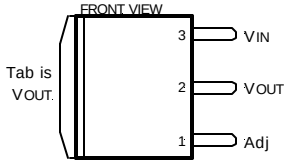
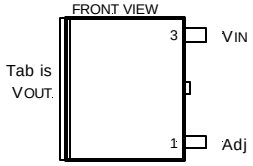
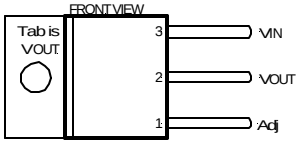
PACKAGE ORDER INFORMATION

T_J (°C)	2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC TO-263 (M)	2-PIN PLASTIC Ultra Thin-Pak™ (P)	3-PIN PLASTIC TO-220 (T)
0 To 150	IRU1050CD	IRU1050CM	IRU1050CP	IRU1050CT

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

2-Pin Plastic TO-252 (D-Pak)	3-Pin Plastic TO-263 (M)	2-Pin Plastic ULTRA THIN-PAK™ (P)	3-Pin Plastic TO-220 (T)
			
θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=35°C/W for 1" Square pad	θ_{JA}=70°C/W for 1" Square pad	θ_{JT}=2.7°C/W θ_{JA}=60°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=10µF, and T_J=0 to 150°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	Io=10mA, T_J=25°C, V_{IN}-Vo=1.5V	1.238	1.25	1.262	V
		Io=10mA, V_{IN}-Vo=1.5	1.225	1.25	1.275	
Line Regulation		Io=10mA, 1.3V<(V_{IN}-Vo)<7V			0.2	%
Load Regulation (Note 1)		V_{IN}=3.3V, V_{ADJ}=0V, 10mA<Io<5A			0.4	%
Dropout Voltage (Note 2)	ΔVo	Note 2, Io=4A			1.2	V
		Io=5A		1.1	1.3	
Current Limit		V_{IN}=3.3V, ΔVo=100mV	5.1			A
Minimum Load Current (Note 3)		V_{IN}=3.3V, V_{ADJ}=0V		5	10	mA
Thermal Regulation		30ms Pulse, V_{IN}-Vo=3V, Io=5A		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum,				
		Io=2.5A, V_{IN}-Vo=3V	60	70		dB
Adjust Pin Current	I_{ADJ}	Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C,				
		Io=10mA, V_{IN}-Vo=1.5V		55	120	µA
Adjust Pin Current Change		Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C		0.2	5	µA
Temperature Stability		V_{IN}=3.3V, V_{ADJ}=0V, Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%Vo

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor dividers are selected such that it automatically maintains this current.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	Adj	A resistor divider from this pin to the V_{OUT} pin and ground sets the output voltage.
2	V_{OUT}	The output of the regulator. A minimum of 10µF capacitor must be connected from this pin to ground to insure stability.
3	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be 1.3V higher than V_{OUT} in order for the device to regulate properly.

BLOCK DIAGRAM

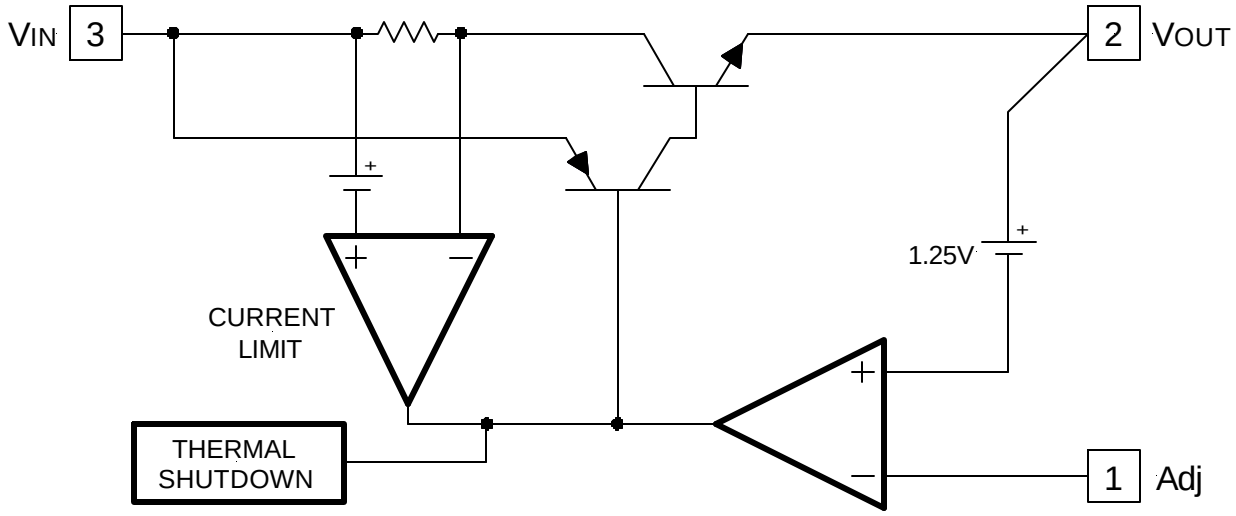


Figure 2 - Simplified block diagram of the IRU1050.

APPLICATION INFORMATION

Introduction

The IRU1050 adjustable Low Dropout (LDO) regulator is a three-terminal device which can easily be programmed with the addition of two external resistors to any voltages within the range of 1.25 to 5.5 V. This regulator unlike the first generation of the three-terminal regulators such as LM117 that required 3V differential between the input and the regulated output, only needs 1.3V differential to maintain output regulation. This is a key requirement for today's microprocessors that need typically 3.3V supply and are often generated from the 5V supply. Another major requirement of these microprocessors such as the Intel P54C™ is the need to switch the load current from zero to several amps in tens of nanoseconds at the processor pins, which translates to an approximately 300 to 500ns current step at the regulator. In addition, the output voltage tolerances are also extremely tight and they include the transient response as part of the specification.For example Intel VRE™ specification calls for a total of ±100mV including initial tolerance, load regulation and 0 to 4.6A load step.

The IRU1050 is specifically designed to meet the fast current transient needs as well as providing an accurate initial voltage, reducing the overall system cost with the need for fewer output capacitors.

Output Voltage Setting

The IRU1050 can be programmed to any voltages in the range of 1.25V to 5.5V with the addition of R1 and R2 external resistors according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) + I_{ADJ} \times R2$$

Where:
V_{REF} = 1.25V Typically
I_{ADJ} = 50µA Typically
R1 and R2 as shown in Figure 3:

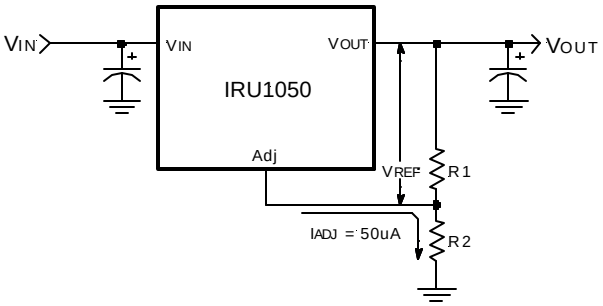


Figure 3 - Typical application of the IRU1050 for programming the output voltage.

The IRU1050 keeps a constant 1.25V between the output pin and the adjust pin. By placing a resistor R1 across these two pins a constant current flows through R1, adding to the I_{ADJ} current and into the R2 resistor producing a voltage equal to the $(1.25/R1) \times R2 + I_{ADJ} \times R2$ which will be added to the 1.25V to set the output voltage. This is summarized in the above equation. Since the minimum load current requirement of the IRU1050 is 10mA, R1 is typically selected to be 121Ω resistor so that it automatically satisfies the minimum current requirement. Notice that since I_{ADJ} is typically in the range of 50µA it only adds a small error to the output voltage and should only be considered when a very precise output voltage setting is required. For example, in a typical 3.3V application where R1=121Ω and R2=200Ω the error due to I_{ADJ} is only 0.3% of the nominal set point.

Load Regulation

Since the IRU1050 is only a three-terminal device, it is not possible to provide true remote sensing of the output voltage at the load. Figure 4 shows that the best load regulation is achieved when the bottom side of R2 is connected to the load and the top side of R1 resistor is connected directly to the case or the V_{OUT} pin of the regulator and not to the load. In fact, if R1 is connected to the load side, the effective resistance between the regulator and the load is gained up by the factor of (1+R2/R1), or the effective resistance will be $R_{P(eff)} = R_P \times (1+R2/R1)$. It is important to note that for high current applications, this can represent a significant percentage of the overall load regulation and one must keep the path from the regulator to the load as short as possible to minimize this effect.

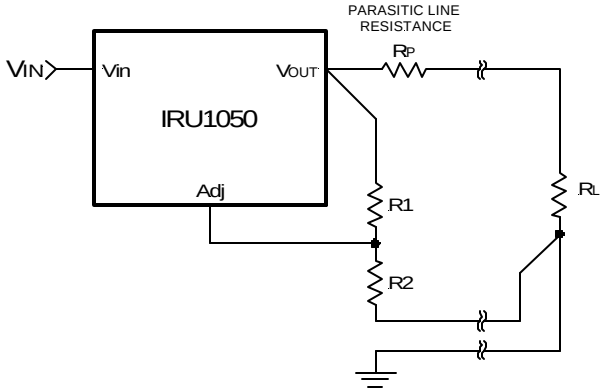


Figure 4 - Schematic showing connection for best load regulation.

Stability

The IRU1050 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for microprocessor applications use standard electrolytic capacitors with a typical ESR in the range of 50 to 100mΩ and an output capacitance of 500 to 1000µF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1050 takes advantage of this phenomena in making the overall regulator loop stable. For most applications a minimum of 100µF aluminum electrolytic capacitor such as Sanyo MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response.

Thermal Design

The IRU1050 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the maximum allowable junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. The example below shows the steps in selecting the proper regulator heat sink for the worst case current consumption using Intel 200MHz microprocessor as the load.

Assuming the following specifications:

V_{IN} = 5V
V_{OUT} = 3.5V
$I_{OUT(MAX)}$ = 4.6A
T_A = 35°C

The steps for selecting a proper heat sink to keep the junction temperature below 135°C is given as:

1) Calculate the maximum power dissipation using:

$P_D = I_{OUT} \times (V_{IN} - V_{OUT})$

$P_D = 4.6 \times (5 - 3.5) = 6.9W$

2) Select a package from the regulator data sheet and record its junction to case (or tab) thermal resistance.

Selecting TO-220 package gives us:

θ_{JC} = 2.7°C/W

3) Assuming that the heat sink is black anodized, calculate the maximum heat sink temperature allowed:

Assume, θcs=0.05°C/W (heat-sink-to-case thermal resistance for black anodized)

$T_S = T_J - P_D \times (\theta_{JC} + \theta_{CS})$

$T_S = 135 - 6.9 \times (27 + 0.05) = 116°C$

4) With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance (θ_{SA}) is calculated by first calculating the temperature rise above the ambient as follows:

$\Delta T = T_S - T_A = 116 - 35 = 81°C$

ΔT = Temperature Rise Above Ambient

$\theta_{SA} = \frac{\Delta T}{P_D} = \frac{81}{6.9} = 11.7°C/W$

5) Next, a heat sink with lower θ_{SA} than the one calculated in Step 4 must be selected. One way to do this is to simply look at the graphs of the "Heat Sink Temp Rise Above the Ambient" vs. the "Power Dissipation" and select a heat sink that results in lower temperature rise than the one calculated in previous step. The following heat sinks from AAVID and Thermalloy meet this criteria.

	Air Flow (LFM)				
	0	100	200	300	400
Thermalloy	6021PB	6021PB	6073PB	6109PB	7141D
AAVID	534202B	534202B	507302	575002	576802B

Note: For further information regarding the above companies and their latest product offerings and application support contact your local representative or the numbers listed below:

AAVID.....PH# (603) 528 3400
Thermalloy.....PH# (214) 243-4321

Designing for Microprocessor Applications

As it was mentioned before, the IRU1050 is designed specifically to provide power for the new generation of the low voltage processors requiring voltages in the range of 2.5V to 3.6V generated by stepping down the 5V supply. These processors demand a fast regulator that supports their large load current changes. The worst case current step seen by the regulator is anywhere in the range of 1 to 7A with the slew rate of 300 to 500ns which could happen when the processor transitions from "Stop Clock" mode to the "Full Active" mode. The load current step at the processor is actually much faster, in the order of 15 to 20ns, however, the decoupling capacitors placed in the cavity of the processor socket handle this transition until the regulator responds to the load current levels. Because of this requirement the selection of high frequency low ESR and low ESL output capacitor is imperative in the design of these regulator circuits.

Figure 5 shows the effects of a fast transient on the output voltage of the regulator. As shown in this figure, the ESR of the output capacitor produces an instantaneous drop equal to the (ΔV_{ESR}=ESR$\times\Delta$I) and the ESL effect will be equal to the rate of change of the output current times the inductance of the capacitor. (ΔV_{ESL} =L$\times\Delta$I/Δt). The output capacitance effect is a droop in the output voltage proportional to the time it takes for the regulator to respond to the change in the current, (ΔVc=Δt$\times\Delta$I/C) where Δt is the response time of the regulator.

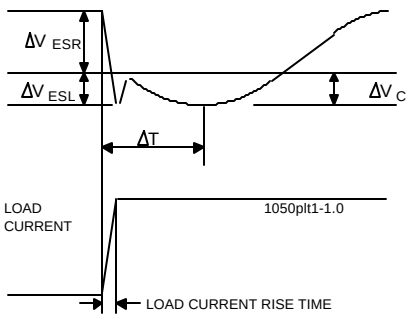


Figure 5 - Typical regulator response to the fast load current step.

An example of a regulator design to meet the Intel P54C™ VRE specification is given below.

Assume the specification for the processor as shown in Table 1:

Type of Processor	V_{OUT} Nominal	I_{MAX}	Max Allowed Output Tolerance
Intel-P54C VRE	3.50 V	4.6 A	±100 mV

Table 1 - Processor Specification

The first step is to select the voltage step allowed in the output due to the output capacitor's ESR:

1) Assuming the regulator's initial accuracy plus the resistor divider tolerance is ≈ ±53mV (±1.5% of 3.5V nominal), then the total step allowed for the ESR and the ESL is –47mV.

Assuming that the ESL drop is –10mV, the remaining ESR step will be –37mV. Therefore the output capacitor ESR must be:

$$ESR \leq \frac{37}{4.6} = 8m\Omega$$

The Sanyo MVGX series is a good choice to achieve both price and performance goals. The 6MV1500GX, 1500μF, 6.3V has an ESR of less than 36mΩ typical. Selecting 5 of these capacitors in parallel has an ESR of ≈ 7.2mΩ which achieves our design goal.

The next step is to calculate the drop due to the capacitance discharge and make sure that this drop in voltage is less than the selected ESL drop in the previous step.

2) The output capacitance is 5×1500μF = 7500μF

$$\Delta Vc = \frac{\Delta t \times \Delta I}{C} = \frac{2 \times 4.6}{7500} = 1.2mV$$

Where:
Δt = 2μs is the regulator response time

To set the output DC voltage, we need to select R1 and R2:

3) Assuming R1=121Ω, 0.1%:

$$R2 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R1 = \left(\frac{3.5}{1.25} - 1\right) \times 121 = 217.8\Omega$$

Select R2=218Ω, 0.1%

Selecting both R1 and R2 resistors to be 0.1% tolerance, results in the least amount of error introduced by the resistor dividers leaving ≈ ±1.3% error budget for the IRU1050 reference which is within the initial accuracy of the device.

Finally, the input capacitor is selected as follows:

4) Assuming that the input voltage can drop 150mV before the main power supply responds, and that the main power supply response time is ≈ 50μs, then the minimum input capacitance for a 4.6A load step is given by:

$$C_{IN} = \frac{4.6 \times 50}{0.15} = 1530\mu F$$

The ESR should be less than:

$$ESR = \frac{(V_{IN} - V_{OUT} - \Delta V - V_{DROP})}{\Delta I}$$

Where:
V_{DROP} **L** Input voltage drop allowed in step 4
ΔV **L** Maximum regulator dropout voltage
ΔI **L** Load current step

$$ESR = \frac{(5 - 3.5 - 1.2 - 0.15)}{4.6} = 0.032\Omega$$

Selecting two Sanyo 1500μF, the same type as the output capacitors, meets our requirements.

Figure 6 shows the completed schematic for our example.

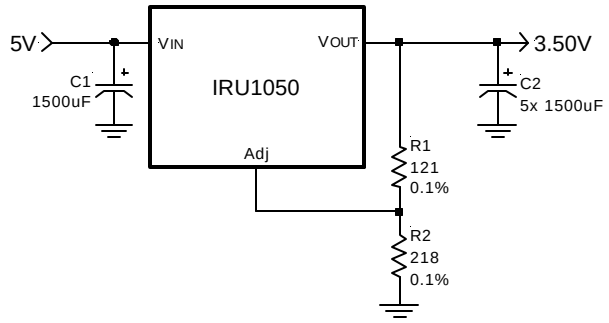


Figure 6 - Final schematic for the Intel VRE application.

Layout Consideration

The output capacitors must be located as close to the V_{OUT} terminal of the device as possible. It is recommended to use a section of a layer of the PC board as a plane to connect the V_{OUT} pin to the output capacitors to prevent any high frequency oscillation that may result due to excessive trace inductance.

International
IOR Rectifier

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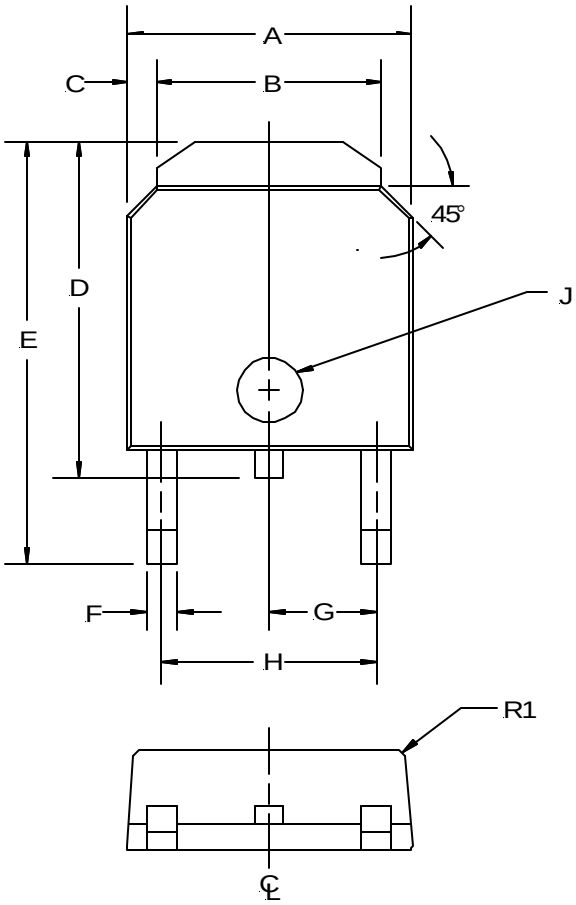
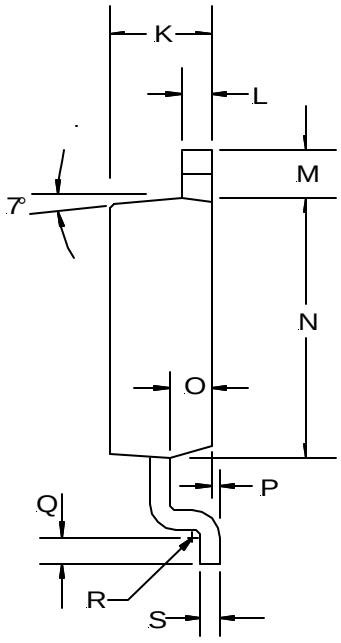
(D) TO-252 Package
2-Pin

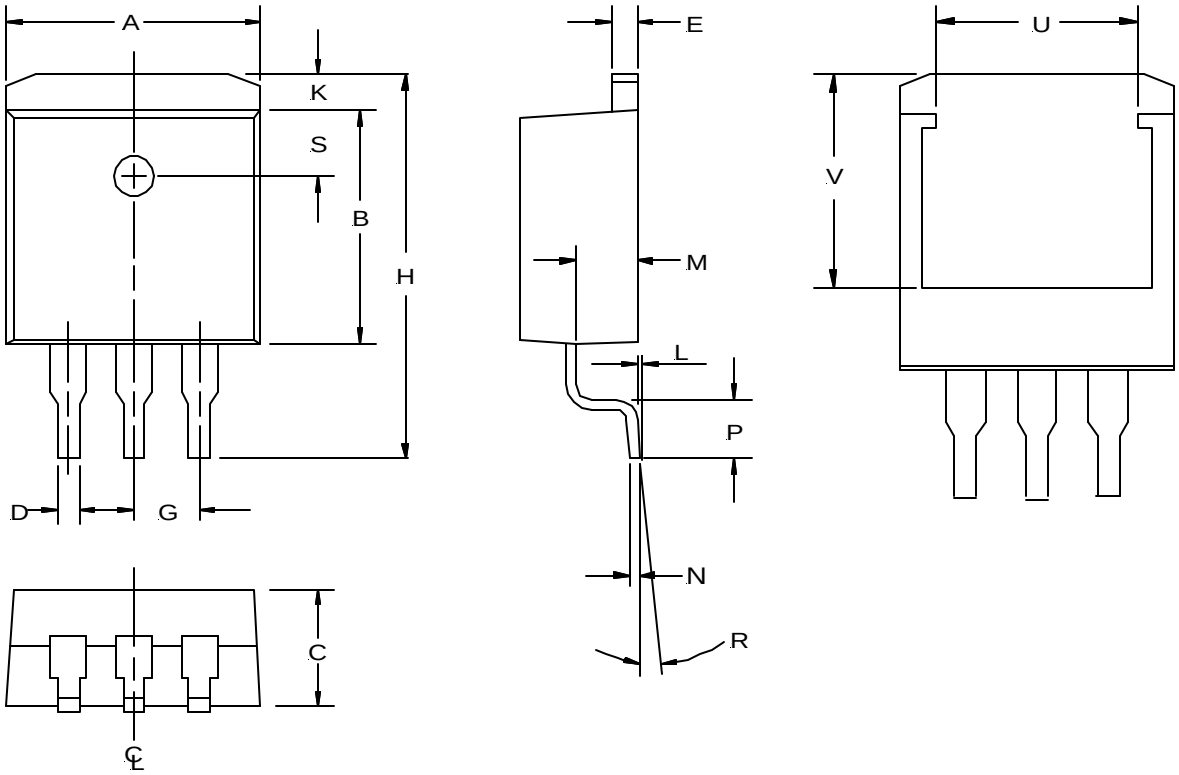




SYMBOL	MIN	MAX
A	6.477	6.731
B	5.004	5.207
C	0.686	0.838
D	7.417	8.179
E	9.703	10.084
F	0.635	0.889
G	2.286 BSC	
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

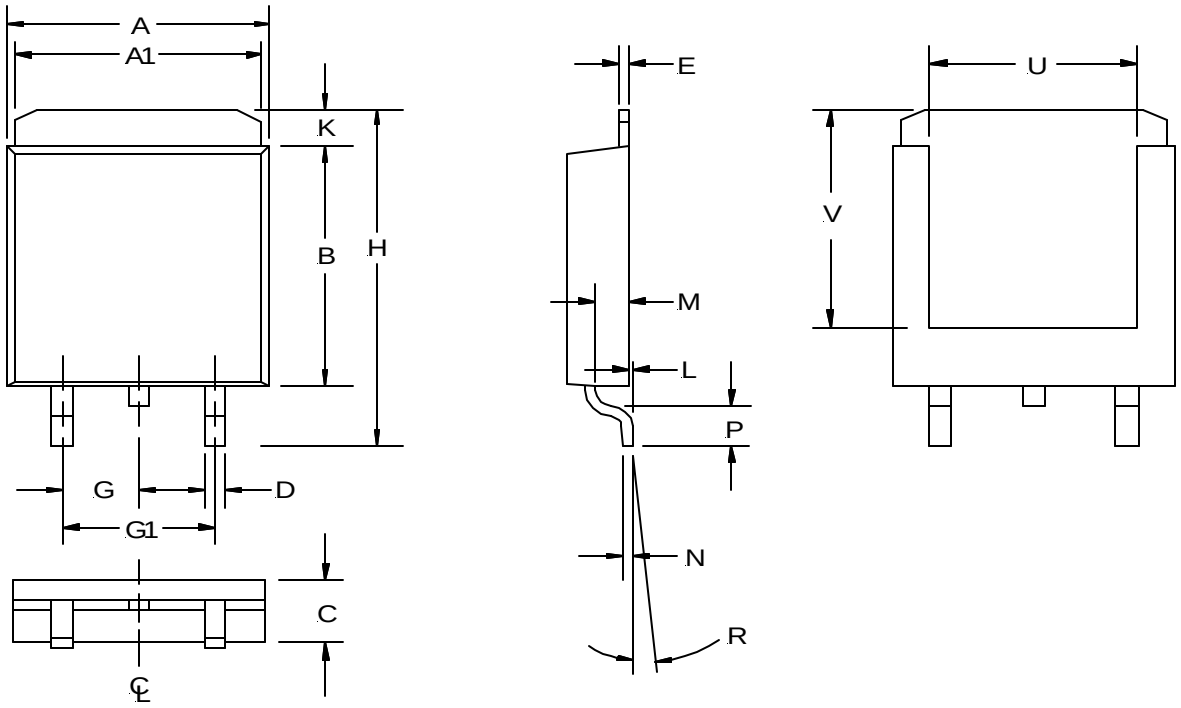
(M) TO-263 Package
3-Pin



SYMBOL	MIN	MAX
A	10.05	10.312
B	8.28	8.763
C	4.31	4.572
D	0.66	0.91
E	1.14	1.40
G	2.54 REF	
H	14.73	15.75
K	1.40	1.68
L	0.00	0.254
M	2.49	2.74
N	0.33	0.58
P	2.286	2.794
R	0°	8°
S	2.41	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

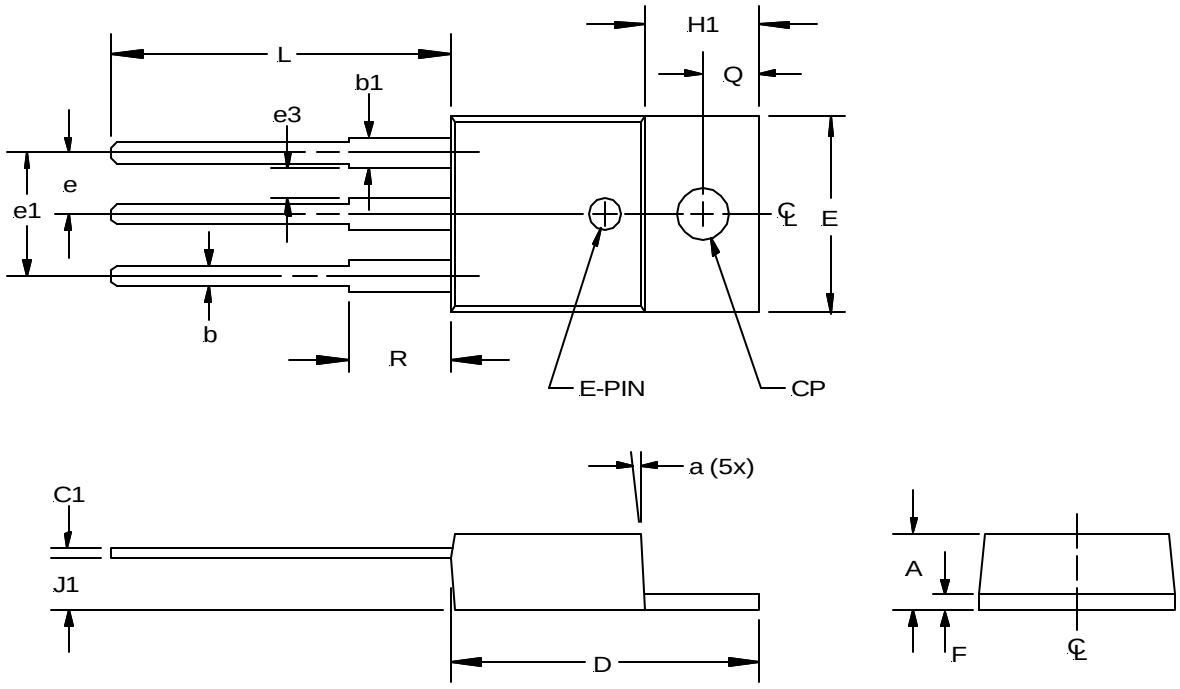
(P) Ultra Thin-Pak™
2-Pin



SYMBOL	MIN	MAX
A	5.91	6.17
A1	5.54	5.79
B	6.02	6.27
C	1.70	2.03
D	0.63	0.79
E	0.17	0.33
G	2.16	2.41
G1	4.45	4.70
H	9.42	9.68
K	0.76	1.27
L	0.02	0.13
M	0.89	1.14
N	0.25	0.25
P	0.94	1.19
R	2°	6°
U	2.92	3.30
V	5.08 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(T) TO-220 Package
3-Pin

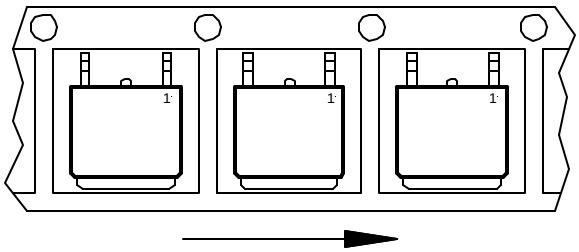


SYMBOL	MIN	MAX
A	4.06	4.83
a	3°	7.5°
b	0.63	1.02
b1	1.14	1.52
C1	0.38	0.56
CP	3.71D	3.96D
D	14.22	15.062
E	9.78	10.54
e	2.29	2.79
e1	4.83	5.33
e3	1.14	1.40
F	1.14	1.40
H1	5.94	6.55
J1	2.29	2.92
L	13.716	14.22
Q	2.62	2.87
R	5.588	6.17

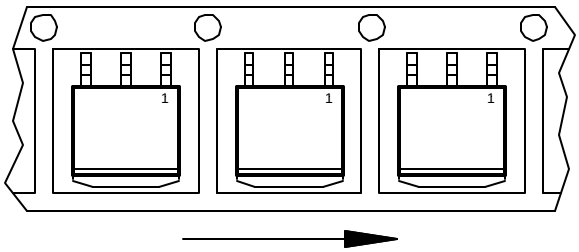
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

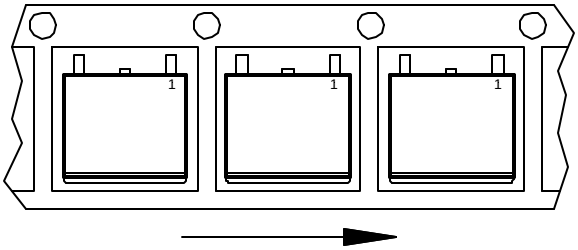
PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
M	TO-263	3	50	750	Fig B
P	Ultra Thin-Pak™	2	75	2500	Fig C
T	TO-220	3	50	---	---



Feed Direction
Figure A



Feed Direction
FigureB



Feed Direction
FigureC

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IRU1050-33

5A LOW DROPOUT POSITIVE FIXED 3.3V REGULATOR

FEATURES

- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Output Current Limiting
- Built-In Thermal Shutdown

APPLICATIONS

- Standard 3.3V Chip Set and Logic Applications

DESCRIPTION

The IRU1050-33 is a low dropout three-terminal fixed 3.3V output regulator with minimum of 5A output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications requiring 3.3V output. The IRU1050-33 is guaranteed to have <1.3V dropout at full load current making it ideal to provide well regulated output with supply voltage as low as 4.6V input.

TYPICAL APPLICATION

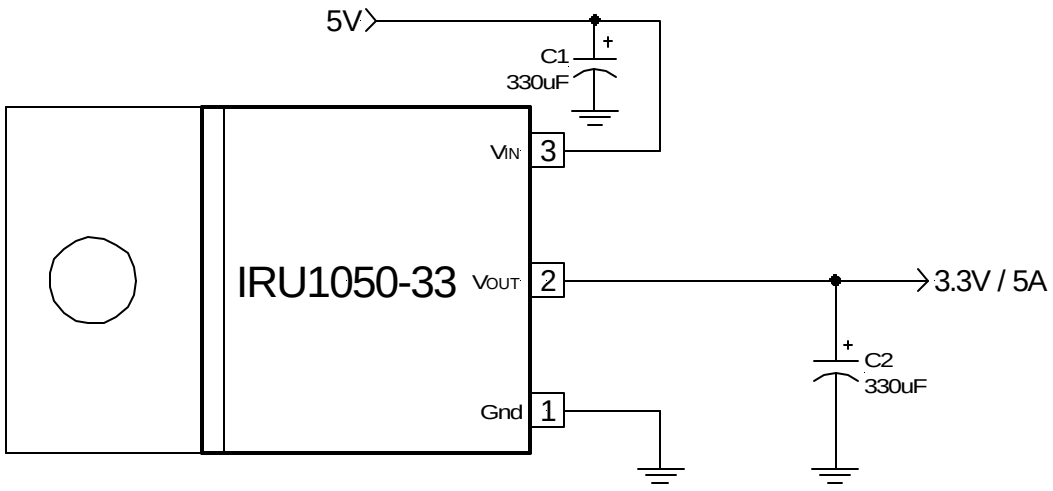


Figure 1 - Typical application of IRU1050-33.

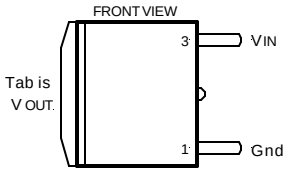
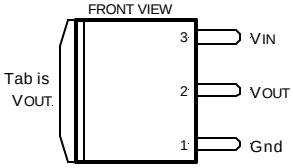
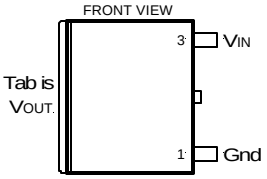
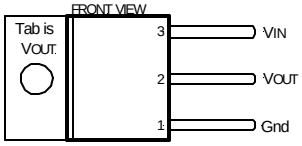
PACKAGE ORDER INFORMATION

T_J (°C)	2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC TO-263 (M)	2-PIN PLASTIC Ultra Thin-Pak™ (P)	3-PIN PLASTIC T0-220 (T)
0 To 150	IRU1050-33CD	IRU1050-33CM	IRU1050-33CP	IRU1050-33CT

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

2-Pin Plastic TO-252 (D-Pak)	3-Pin Plastic TO-263 (M)	2-Pin Plastic ULTRA THIN-PAK™ (P)	3-Pin Plastic TO-220 (T)
			
θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=35°C/W for 1" Square pad	θ_{JA}=70°C/W for 1" Square pad	θ_{JT}=2.7°C/W θ_{JA}=60°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=10µF, and T_J=0 to 150°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	Vo	Io=10mA, T_J=25°C, V_{IN}=5V	3.267	3.3	3.333	V
		Io=10mA, V_{IN}=5V	3.234	3.3	3.366	
Line Regulation		Io=10mA, 4.7V<V_{IN}<7V			0.2	%
Load Regulation (Note 1)		V_{IN}=3.3V, 10mA<Io<5A			0.4	%
Dropout Voltage (Note 2)	ΔVo	Note 2, Io=5A		1.1	1.3	V
Current Limit		V_{IN}=5V, ΔVo=100mV	5.1			A
Minimum Load Current (Note 3)		V_{IN}=5V		5	10	mA
Thermal Regulation		30ms Pulse, V_{IN}-Vo=3V, Io=5A		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum,				
		Io=2.5A, V_{IN}-Vo=3V	60	70		dB
Temperature Stability		V_{IN}=5V, Io=10mA		0.5		%
Long Term Stability		T_J=25°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%Vo

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor dividers are selected such that it automatically maintains this current.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	Gnd	This pin must be connected to ground plane using a low inductance short connection.
2	V_{OUT}	The output of the regulator. A minimum of 10µF capacitor must be connected from this pin to ground to insure stability.
3	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum dropout voltage during the load transient response. This pin must always be 1.3V higher than V_{OUT} in order for the device to regulate properly.

BLOCK DIAGRAM

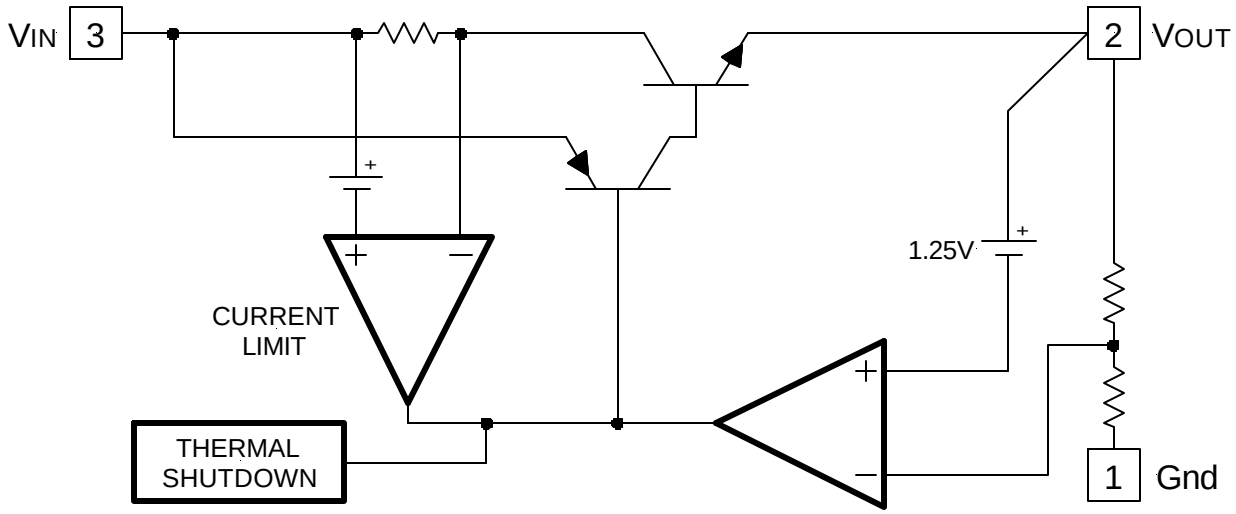


Figure 1 - Simplified block diagram of the IRU1050-33.

APPLICATION INFORMATION

Stability

The IRU1050-33 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for microprocessor applications use standard electrolytic capacitors with a typical ESR in the range of 50 to 100mΩ and an output capacitance of 500 to 1000µF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1050-33 takes advantage of this phenomena in making the overall regulator loop stable. For most applications a minimum of 100µF aluminum electrolytic capacitor such as Sanyo MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response.

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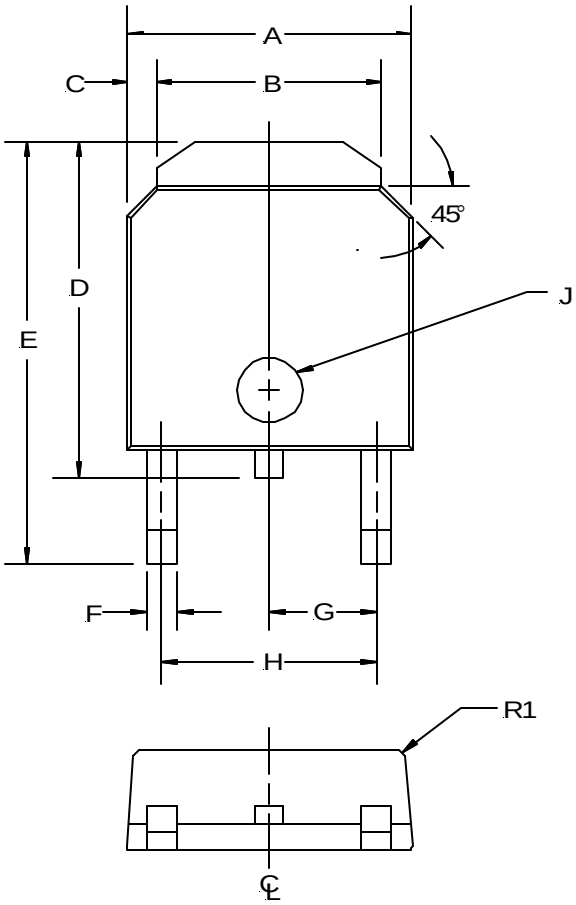
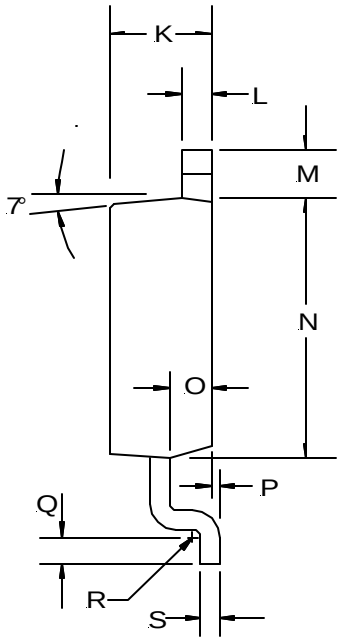
(D) TO-252 Package
2-Pin

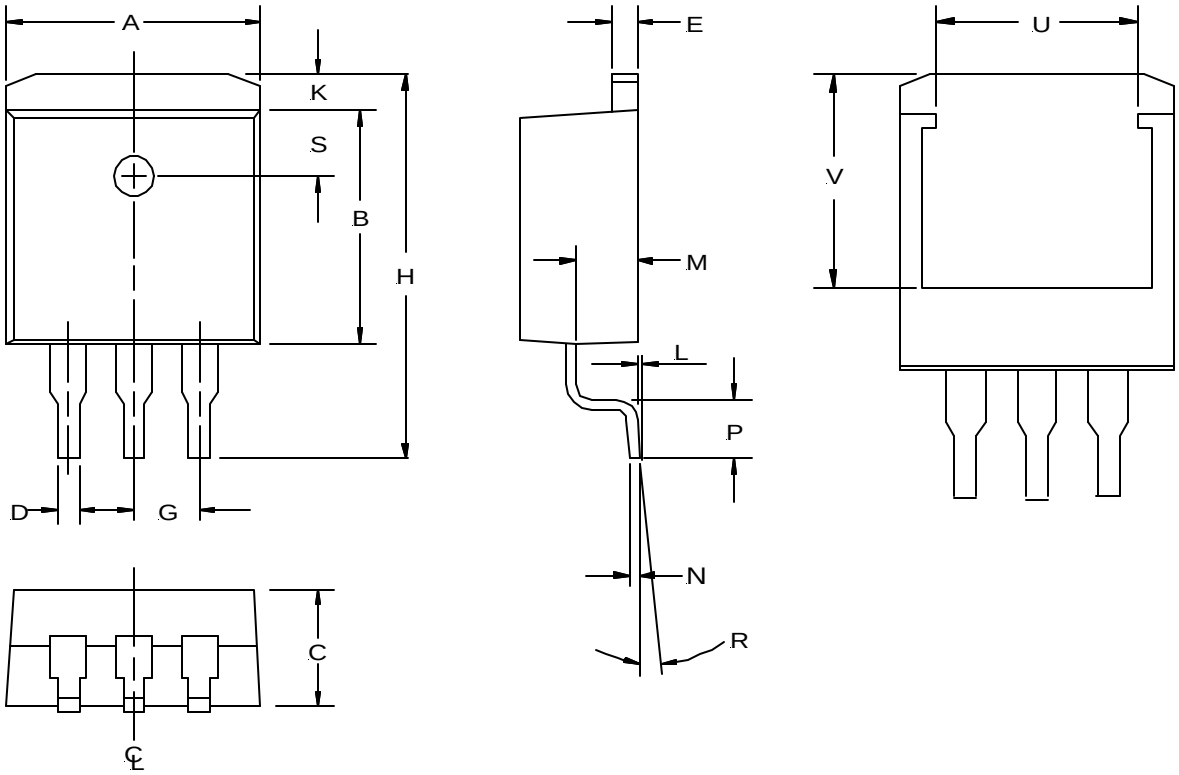




SYMBOL	MIN	MAX
A	6.477	6.731
B	5.004	5.207
C	0.686	0.838
D	7.417	8.179
E	9.703	10.084
F	0.635	0.889
G	2.286 BSC	
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

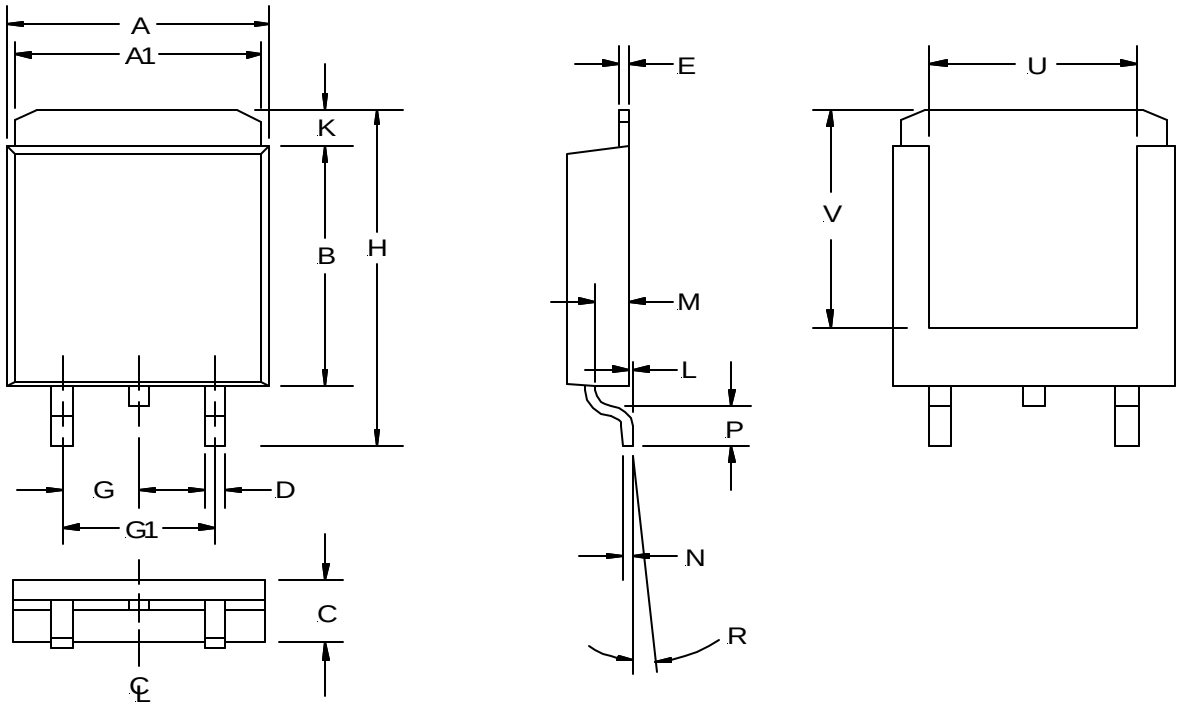
(M) TO-263 Package
3-Pin



SYMBOL	MIN	MAX
A	10.05	10.312
B	8.28	8.763
C	4.31	4.572
D	0.66	0.91
E	1.14	1.40
G	2.54 REF	
H	14.73	15.75
K	1.40	1.68
L	0.00	0.254
M	2.49	2.74
N	0.33	0.58
P	2.286	2.794
R	0°	8°
S	2.41	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

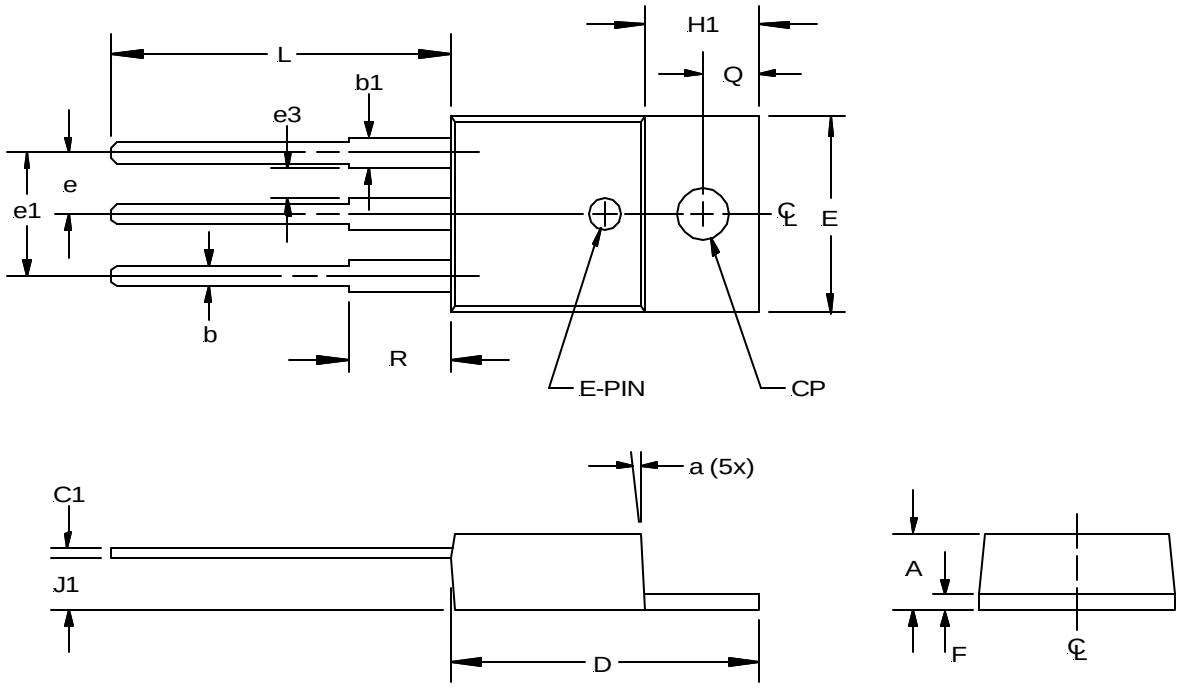
(P) Ultra Thin-Pak™
2-Pin



SYMBOL	MIN	MAX
A	5.91	6.17
A1	5.54	5.79
B	6.02	6.27
C	1.70	2.03
D	0.63	0.79
E	0.17	0.33
G	2.16	2.41
G1	4.45	4.70
H	9.42	9.68
K	0.76	1.27
L	0.02	0.13
M	0.89	1.14
N	0.25	0.25
P	0.94	1.19
R	2°	6°
U	2.92	3.30
V	5.08 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(T) TO-220 Package
3-Pin

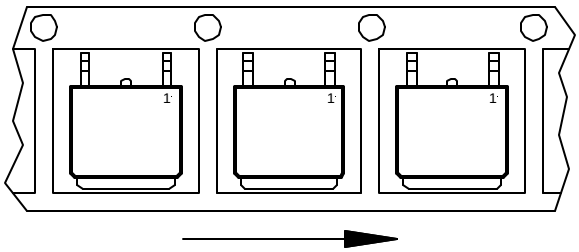


SYMBOL	MIN	MAX
A	4.06	4.83
a	3°	7.5°
b	0.63	1.02
b1	1.14	1.52
C1	0.38	0.56
CP	3.71D	3.96D
D	14.22	15.062
E	9.78	10.54
e	2.29	2.79
e1	4.83	5.33
e3	1.14	1.40
F	1.14	1.40
H1	5.94	6.55
J1	2.29	2.92
L	13.716	14.22
Q	2.62	2.87
R	5.588	6.17

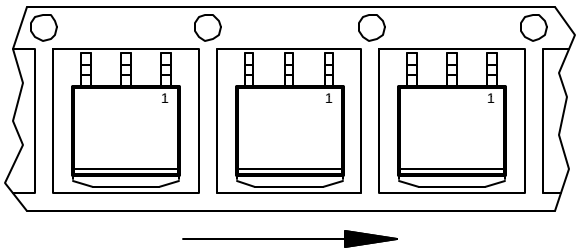
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

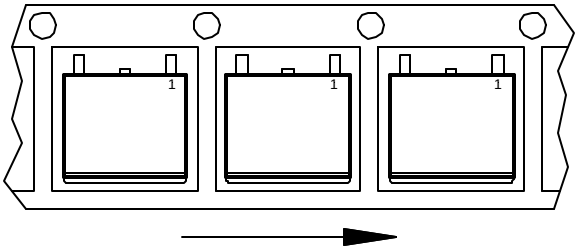
PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
M	TO-263	3	50	750	Fig B
P	Ultra Thin-Pak™	2	75	2500	Fig C
T	TO-220	3	50	---	---



Feed Direction
Figure A



Feed Direction
FigureB



Feed Direction
FigureC

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IRU1075

7.5A LOW DROPOUT POSITIVE ADJUSTABLE REGULATOR

FEATURES

- 1V Dropout at Full Load Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Output Current Limiting
- Built-In Thermal Shutdown

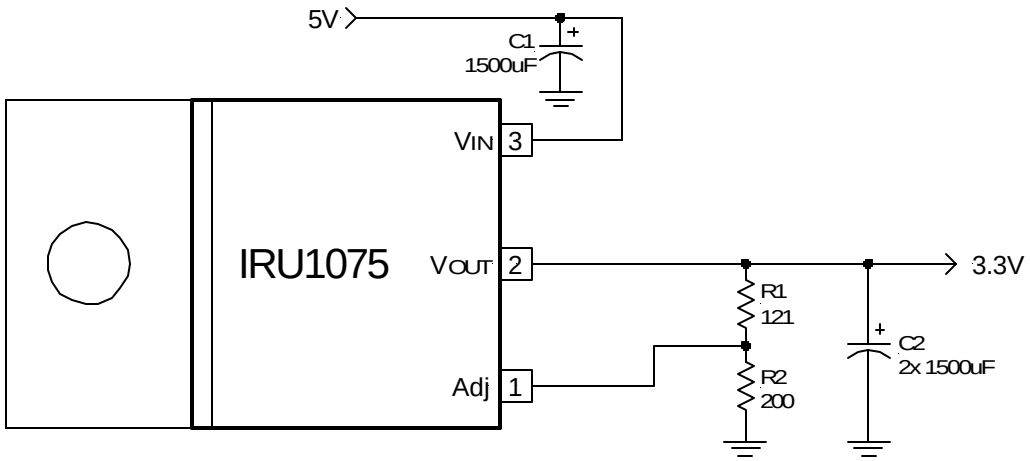
APPLICATIONS

- Low Voltage Processor Applications such as: P54C™ ,P55C™ , Cyrix M2™, POWER PC™ , AMD
- GTL+ Termination PENTIUM PRO™ , KLAMATH™
- Low Voltage Memory Termination Applications
- Standard 3.3V Chip Set and Logic Applications

DESCRIPTION

The IRU1075 is a low dropout three-terminal adjustable regulator with minimum of 7.5A output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications such as Pentium™ P54C™ , P55C™ as well as GTL+ termination for Pentium Pro™ and Klamath™ processor applications. The IRU1075 is also well suited for other processors such as Cyrix™ , AMD and Power PC™ applications. The IRU1075 is guaranteed to have <1.2V dropout at full load current making it ideal to provide well regulated outputs such as 3.3V with input supply voltage as low as 4.5V minimum.

TYPICAL APPLICATION



Typical application of IRU1075 in a 5V to 3.3V regulator.

Notes: Pentium P54C, P55C, Klamath, Pentium Pro, VRE are trademarks of Intel Corp. Cyrix M2 is trademark of Cyrix Corp. Power PC is trademark of IBM Corp.

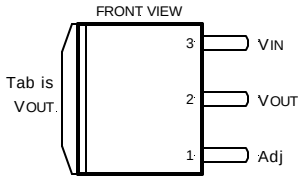
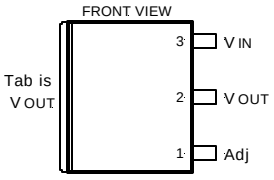
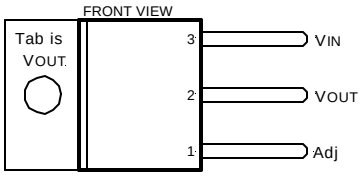
PACKAGE ORDER INFORMATION

T_J (°C)	3-PIN PLASTIC TO-263 (M)	3-PIN PLASTIC Ultra Thin-Pak™ (P)	3-PIN PLASTIC TO-220 (T)
0 To 150	IRU1075CM	IRU1075CP	IRU1075CT

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

3-PIN PLASTIC TO-263 (M)	3-PIN PLASTIC ULTRA THIN-PAK™ (P)	3-PIN PLASTIC TO-220 (T)
		
θ_{JA}=35°C/W for 1" Square pad	θ_{JA}=35°C/W for 1" Square pad	θ_{JT}=2.7°C/W θ_{JA}=60°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=10µF, and T_J=0 to 150°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	Io=10mA, T_J=25°C, (V_{IN}-Vo)=1.5V	1.238	1.250	1.262	V
		Io=10mA, (V_{IN}-Vo)=1.5V	1.225	1.250	1.275	
Line Regulation		Io=10mA, 1.3V<(V_{IN}-Vo)<7V			0.2	%
Load Regulation (Note 1)		V_{IN}=3.3V, V_{ADJ}=0, 10mA<Io<7.5A		0.4		%
Dropout Voltage (Note 2)	ΔV_O	Io=7.5A		1.0	1.2	V
		Io=4A		0.92	1.1	
Current Limit		V_{IN}=3.3V, ΔVo=100mV	7.6	9		A
Minimum Load Current (Note 3)		V_{IN}=3.3V, V_{ADJ}=0V		5	10	mA
Thermal Regulation		30ms Pulse, V_{IN}-Vo=3V, Io=7.5A		0.02		%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum,				
		Io=7.5A, V_{IN}-Vo=3V	60	70		dB
Adjust Pin Current	I_{ADJ}	Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C,				
		Io=10mA, V_{IN}-Vo=1.5V		55	120	µA
Adjust Pin Current Change		Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C		0.2	5	µA
Temperature Stability		V_{IN}=3.3V, V_{ADJ}=0V, Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3		%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%V_O

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor dividers are selected such that it automatically maintains this current.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	Adj	A resistor divider from this pin to the V_{OUT} pin and ground sets the output voltage.
2	V_{OUT}	The output of the regulator. A minimum of 10µF capacitor must be connected from this pin to ground to insure stability.
3	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be 1.3V higher than V_{OUT} in order for the device to regulate properly.

BLOCK DIAGRAM

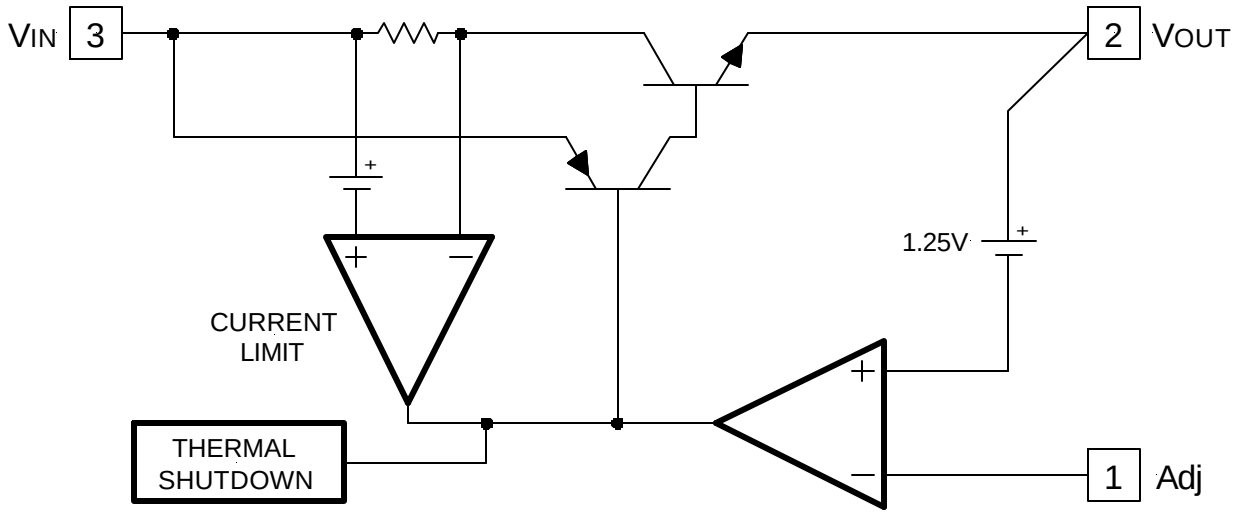


Figure 2 - Simplified block diagram of the IRU1075.

APPLICATION INFORMATION

Introduction

The IRU1075 adjustable Low Dropout (LDO) regulator is a three-terminal device which can easily be programmed with the addition of two external resistors to any voltages within the range of 1.25 to 5.5 V. This regulator unlike the first generation of the three-terminal regulators such as LM117 that required 3V differential between the input and the regulated output, only needs 1.3V differential to maintain output regulation. This is a key requirement for today's microprocessors that need typically 3.3V supply and are often generated from the 5V supply. Another major requirement of these microprocessors such as the Intel P54C™ is the need to switch the load current from zero to several amps in tens of nanoseconds at the processor pins, which translates to an approximately 300 to 500ns current step at the regulator. In addition, the output voltage tolerances are also extremely tight and they include the transient response as part of the specification. For example Intel VRE™ specification calls for a total of ±100mV including initial tolerance, load regulation and 0 to 4.6A load step.

The IRU1075 is specifically designed to meet the fast current transient needs as well as providing an accurate initial voltage, reducing the overall system cost with the need for fewer output capacitors.

Output Voltage Setting

The IRU1075 can be programmed to any voltages in the range of 1.25V to 5.5V with the addition of R1 and R2 external resistors according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) + I_{ADJ} \times R2$$

Where:

V_{REF} = 1.25V Typically

I_{ADJ} = 50µA Typically

R1 and R2 as shown in Figure 3:

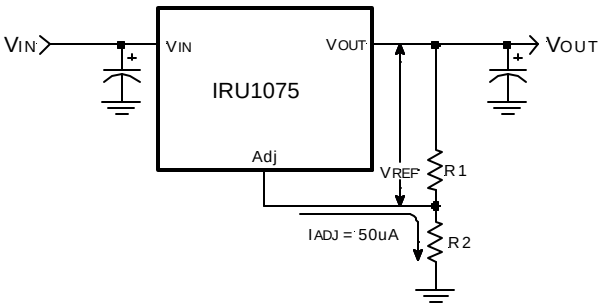


Figure 3 - Typical application of the IRU1075 for programming the output voltage.

The IRU1075 keeps a constant 1.25V between the output pin and the adjust pin. By placing a resistor R1 across these two pins a constant current flows through R1, adding to the I_{ADJ} current and into the R2 resistor producing a voltage equal to the $(1.25/R1) \times R2 + I_{ADJ} \times R2$ which will be added to the 1.25V to set the output voltage. This is summarized in the above equation. Since the minimum load current requirement of the IRU1075 is 10mA, R1 is typically selected to be 121Ω resistor so that it automatically satisfies the minimum current requirement. Notice that since I_{ADJ} is typically in the range of 50µA it only adds a small error to the output voltage and should only be considered when a very precise output voltage setting is required. For example, in a typical 3.3V application where R1=121Ω and R2=200Ω the error due to I_{ADJ} is only 0.3% of the nominal set point.

Load Regulation

Since the IRU1075 is only a three-terminal device, it is not possible to provide true remote sensing of the output voltage at the load. Figure 4 shows that the best load regulation is achieved when the bottom side of R2 is connected to the load and the top side of R1 resistor is connected directly to the case or the V_{OUT} pin of the regulator and not to the load. In fact, if R1 is connected to the load side, the effective resistance between the regulator and the load is gained up by the factor of (1+R2/R1), or the effective resistance will be, $R_{P(eff)} = R_P \times (1+R2/R1)$. It is important to note that for high current applications, this can represent a significant percentage of the overall load regulation and one must keep the path from the regulator to the load as short as possible to minimize this effect.

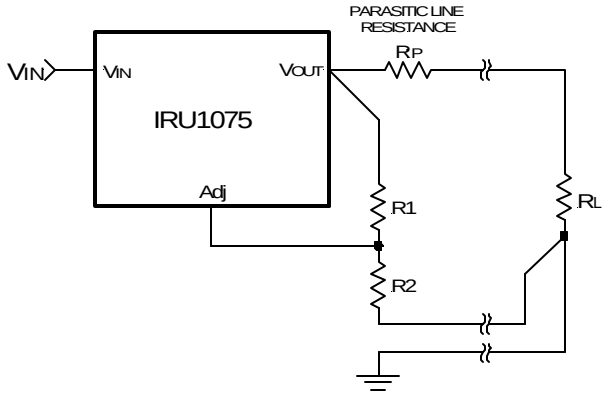


Figure 4 - Schematic showing connection for best load regulation.

Stability

The IRU1075 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for microprocessor applications use standard electrolytic capacitors with a typical ESR in the range of 50 to 100 mΩ and an output capacitance of 500 to 1000µF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1075 takes advantage of this phenomena in making the overall regulator loop stable. For most applications a minimum of 100µF aluminum electrolytic capacitor such as Sanyo MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response.

Thermal Design

The IRU1075 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the maximum allowable junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. The example below shows the steps in selecting the proper regulator heat sink for the worst case current consumption using Intel 200MHz microprocessor as the load.

Assuming the following specifications:

V_{IN} = 5V
V_{OUT} = 3.5V
$I_{OUT(MAX)}$ = 4.6A
T_A = 35°C

The steps for selecting a proper heat sink to keep the junction temperature below 135°C is given as:

1) Calculate the maximum power dissipation using:

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT})$$
$$P_D = 4.6 \times (5 - 3.5) = 6.9W$$

2) Select a package from the regulator data sheet and record its junction to case (or tab) thermal resistance.

Selecting TO-220 package gives us:

θ_{JC} = 2.7°C/W

3) Assuming that the heat sink is black anodized, calculate the maximum heat sink temperature allowed:

Assume, θcs = 0.05°C/W (heat-sink-to-case thermal resistance for black anodized)

$$T_S = T_J - P_D \times (\theta_{JC} + \theta_{CS})$$
$$T_S = 135 - 6.9 \times (2.7 + 0.05) = 116°C$$

4) With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance (θ_{SA}) is calculated by first calculating the temperature rise above the ambient as follows:

$$\Delta T = T_S - T_A = 116 - 35 = 81°C$$

ΔT = Temperature Rise Above Ambient

$$\theta_{SA} = \frac{\Delta T}{P_D} = \frac{81}{6.9} = 11.7°C/W$$

5) Next, a heat sink with lower θ_{SA} than the one calculated in Step 4 must be selected. One way to do this is to simply look at the graphs of the "Heat Sink Temp Rise Above the Ambient" vs. the "Power Dissipation" and select a heat sink that results in lower temperature rise than the one calculated in previous step. The following heat sinks from AAVID and Thermalloy meet this criteria.

	Air Flow (LFM)				
	0	**100**	**200**	**300**	**400**
Thermalloy	6021PB	6021PB	6073PB	6109PB	7141D
AAVID	534202B	534202B	507302	575002	576802B

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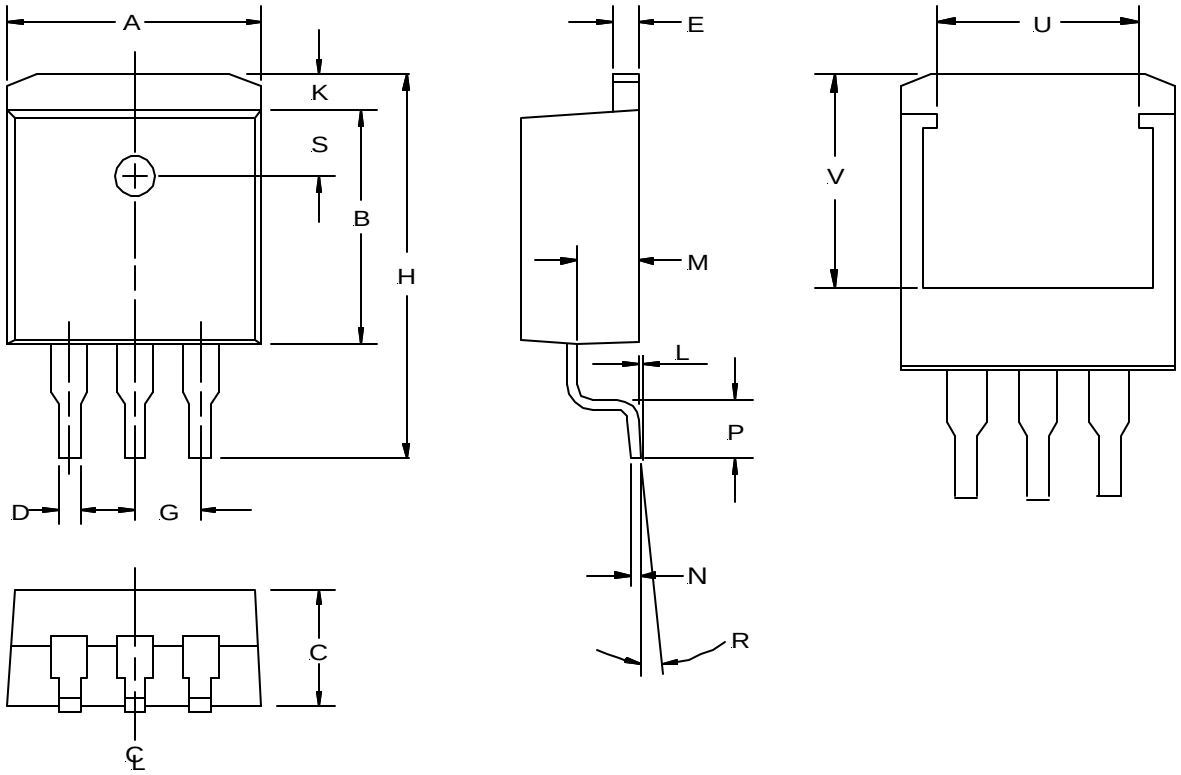
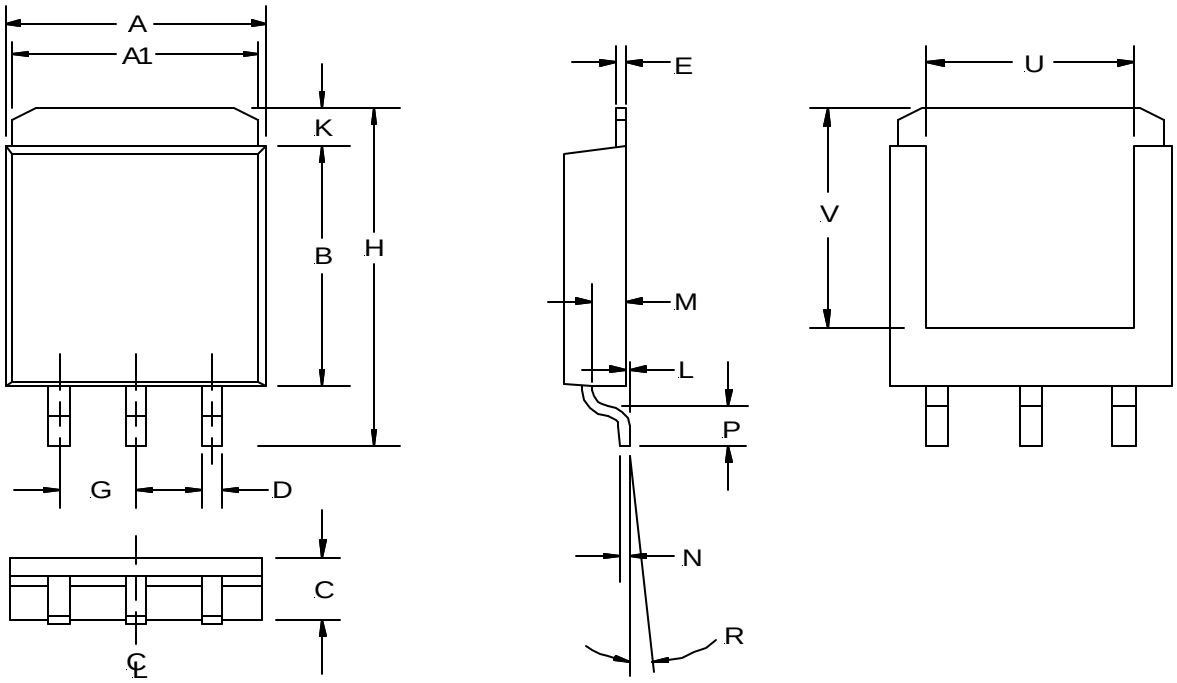
(M) TO-263 Package
3-Pin



SYMBOL	MIN	MAX
A	10.05	10.312
B	8.28	8.763
C	4.31	4.572
D	0.66	0.91
E	1.14	1.40
G	2.54 REF	
H	14.73	15.75
K	1.40	1.68
L	0.00	0.254
M	2.49	2.74
N	0.33	0.58
P	2.286	2.794
R	0°	8°
S	2.41	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

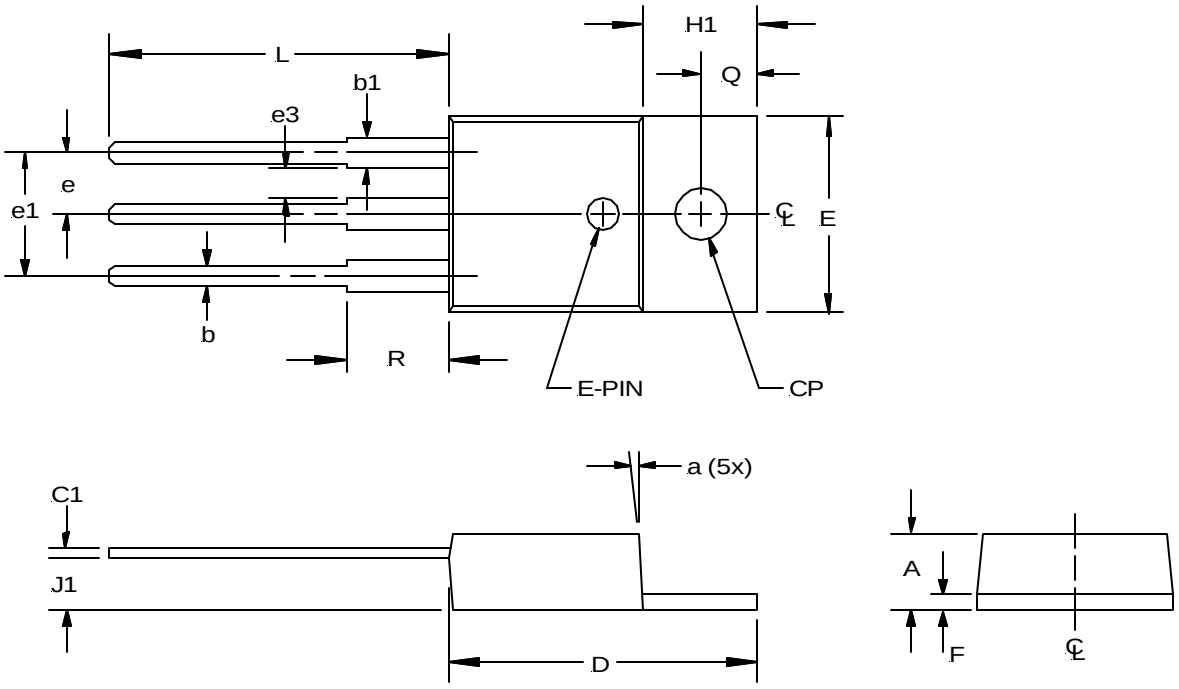
(P) Ultra Thin-Pak™
3-Pin



SYMBOL	MIN	MAX
A	9.27	9.52
A1	8.89	9.14
B	7.87	8.13
C	1.78	2.03
D	0.63	0.79
E	0.25 NOM	
G	2.54	
H	10.41	10.67
K	0.76	1.27
L	0.03	0.13
M	0.89	1.14
N	0.25	
P	0.79	1.04
R	3°	6°
U	5.59 NOM	
V	7.49 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(T) TO-220 Package
3-Pin

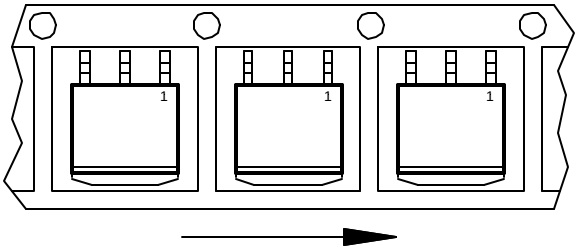


SYMBOL	MIN	MAX
A	4.06	4.83
a	3°	7.5°
b	0.63	1.02
b1	1.14	1.52
C1	0.38	0.56
CP	3.71D	3.96D
D	14.22	15.062
E	9.78	10.54
e	2.29	2.79
e1	4.83	5.33
e3	1.14	1.40
F	1.14	1.40
H1	5.94	6.55
J1	2.29	2.92
L	13.716	14.22
Q	2.62	2.87
R	5.588	6.17

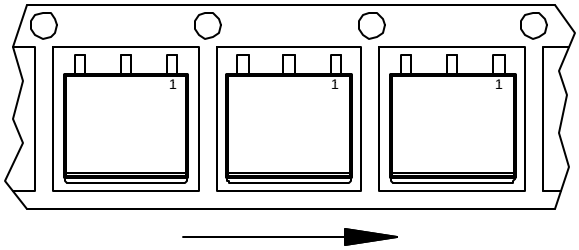
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
M	TO-263	3	50	750	Fig A
P	Ultra Thin-Pak™	3	75	2500	Fig B
T	TO-220	3	50	---	---



Feed Direction
Figure A



Feed Direction
FigureB

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IRU1117

800mA LOW DROPOUT POSITIVE ADJUSTABLE REGULATOR

FEATURES

- Guaranteed < 1.2V Dropout at 800mA Load Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown
- Available in SOT-223, D-Pak, Ultra Thin-Pak™ and 8-Pin SOIC Surface-Mount Packages

APPLICATIONS

- VGA & Sound Card Applications
- Low Voltage High Speed Termination Applications
- Standard 3.3V Chip Set and Logic Applications

DESCRIPTION

The IRU1117 is a low dropout, three-terminal adjustable regulator with minimum of 800mA output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications such as high speed bus termination and low current 3.3V logic supply. The IRU1117 is also well suited for other applications such as VGA and sound cards. The IRU1117 is guaranteed to have <1.2V dropout at full load current making it ideal to provide well regulated outputs of 2.5V to 3.6V with 4.75V to 7V input supply.

TYPICAL APPLICATION

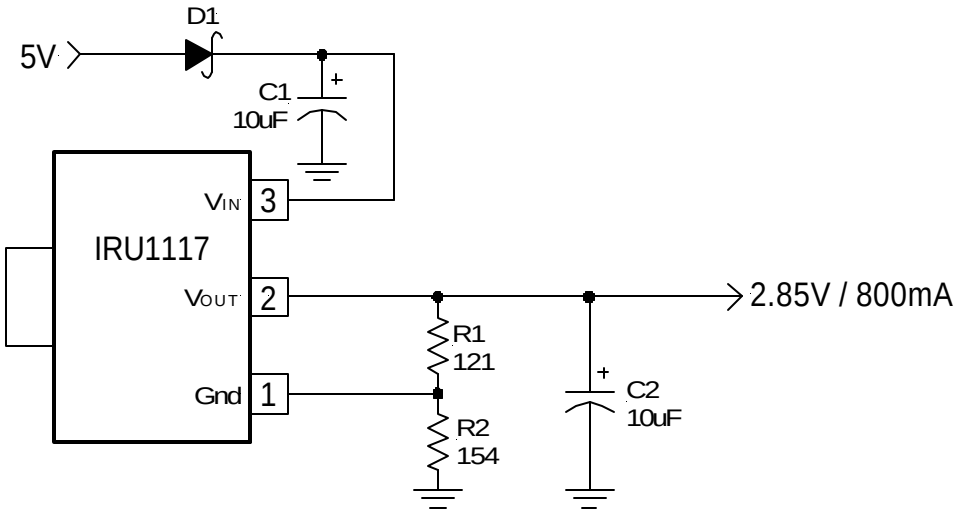


Figure 1 - Typical application of IRU1117 in a 5V to 2.85V SCSI termination regulator.

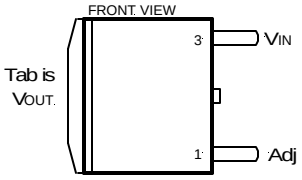
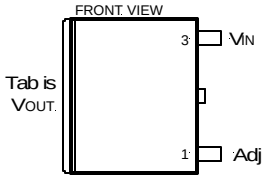
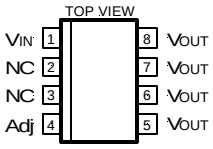
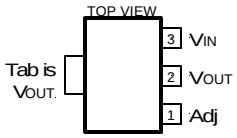
PACKAGE ORDER INFORMATION

T_J (°C)	2-PIN PLASTIC TO-252 (D-Pak)	2-PIN PLASTIC Ultra Thin-Pak™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SOT-223 (Y)
0 To 150	IRU1117CD	IRU1117CP	IRU1117CS	IRU1117CY

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN})	7V
Power Dissipation	Internally Limited
Storage Temperature Range	-65°C To 150°C
Operating Junction Temperature Range	0°C To 150°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)	2-PIN ULTRA THIN-PAK™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SO-223 (Y)
			
θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=55°C/W for 1" Sq pad	θ_{JA}=90°C/W for 0.4" Sq pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=10µF, and T_J=0 to 150°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	Io=10mA, T_J=25°C, (V_{IN}-Vo)=1.5V	1.238	1.250	1.262	V
		Io=10mA, (V_{IN}-Vo)=1.5V	1.225	1.250	1.275	
Line Regulation		Io=10mA, 1.3V<(V_{IN}-Vo)<7V			0.2	%
Load Regulation (Note 1)		V_{IN}=3.3V, V_{ADJ}=0, 10mA<Io<800mA			0.4	%
Dropout Voltage (Note 2)	ΔV_O	Io=1A		1.2	1.3	V
		Io=800mA, Note 2		1.1	1.2	
Current Limit		V_{IN}=3.3V, ΔVo=100mV	1.1			A
Minimum Load Current (Note 3)		V_{IN}=3.3V, V_{ADJ}=0V		5	10	mA
Thermal Regulation		30ms Pulse, V_{IN}-Vo=3V, Io=800mA		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum,				
		Io=0.5A, V_{IN}-Vo=3V	60	70		dB
Adjust Pin Current	I_{ADJ}	Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C,				
		Io=10mA, V_{IN}-Vo=1.5V		55	120	µA
Adjust Pin Current Change		Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C		0.2	5	µA
Temperature Stability		V_{IN}=3.3V, V_{ADJ}=0V, Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%V_O

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically, the resistor dividers are selected such that it automatically maintains this current. Typically, the values of the resistors used to build the voltage divider are selected to ensure that minimum load current is maintained.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	Adj	A resistor divider from this pin to the V_{OUT} pin and ground sets the output voltage.
2	V_{OUT}	The output of the regulator. A minimum of 10µF capacitor must be connected from this pin to ground to insure stability.
3	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum dropout voltage during the load transient response. This pin must always be 1.3V higher than V_{OUT} in order for the device to regulate properly.

BLOCK DIAGRAM

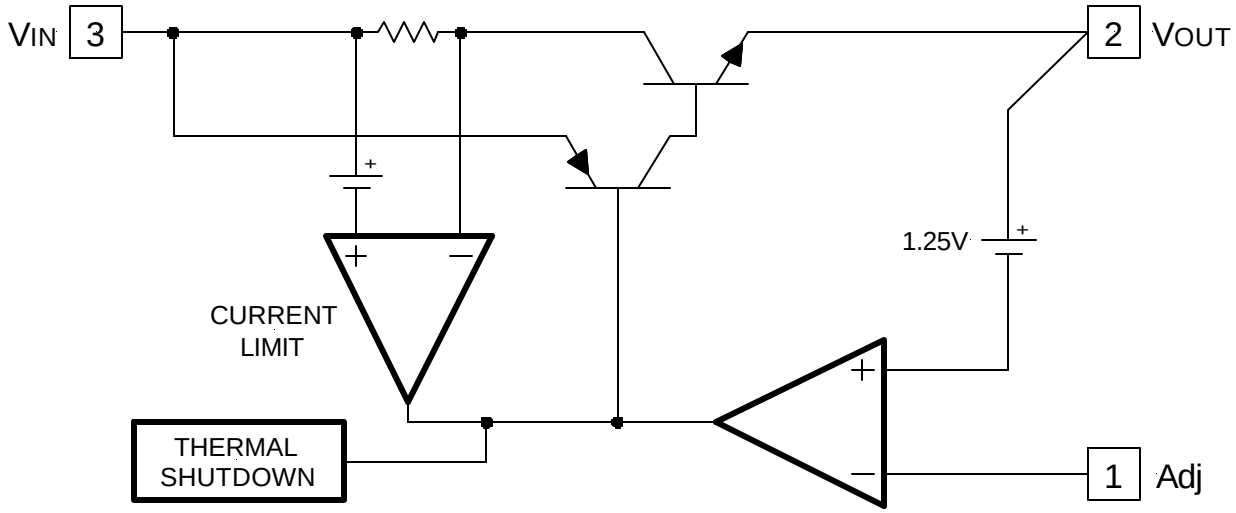


Figure 2 - Simplified block diagram of the IRU1117.

APPLICATION INFORMATION

Introduction

The IRU1117 adjustable Low Dropout (LDO) regulator is a three-terminal device which can easily be programmed with the addition of two external resistors to any voltages within the range of 1.25 to 5.5V. This regulator only needs 1.3V differential to maintain output regulation. Unlike the first generation of the three-terminal regulators such as LM117 that required 3V differential between the input and the regulated output.

The IRU1117 is specifically designed to meet the fast current transient needs as well as providing an accurate initial voltage, reducing the overall system cost with the need for fewer output capacitors. This is a key requirement for today's low voltage IC applications that typically need 3.3V supply and are often generated from the 5V supply. Other applications such as high speed memory termination need to switch the load current from zero to full load in tens of nanoseconds at their pins, which translates to an approximately 300 to 500ns current step at the regulator. In addition, the output voltage tolerances are sometimes tight and they include the transient response as part of the specification.

Output Voltage Setting

The IRU1117 can be programmed to any voltages in the range of 1.25V to 5.5V with the addition of R1 and R2 external resistors according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) + I_{ADJ} \times R2$$

Where:
VREF = 1.25V Typically
I_{ADJ} = 50µA Typically
R1 and R2 as shown in Figure 3:

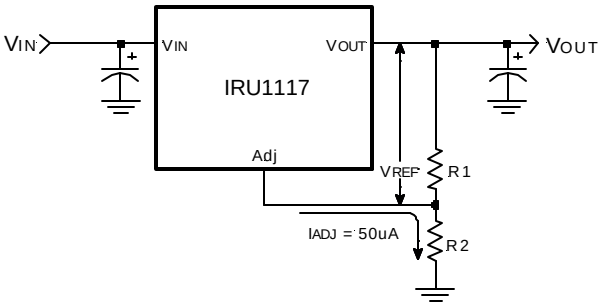


Figure 3 - Typical application of the IRU1117 for programming the output voltage.

The IRU1117 keeps a constant 1.25V between the output pin and the adjust pin. By placing a resistor R1 across these two pins a constant current flows through R1, adding to the I_{ADJ} current and into the R2 resistor producing a voltage equal to the $(1.25/R1) \times R2 + I_{ADJ} \times R2$ which will be added to the 1.25V to set the output voltage. This is summarized in the above equation. Since the minimum load current requirement of the IRU1117 is 10mA, R1 is typically selected to be 121Ω resistor so that it automatically satisfies the minimum current requirement. Notice that since I_{ADJ} is typically in the range of 50µA it only adds a small error to the output voltage and should only be considered when a very precise output voltage setting is required. For example, in a typical 3.3V application where R1=121Ω and R2=200Ω the error due to I_{ADJ} is only 0.3% of the nominal set point.

Load Regulation

Since the IRU1117 is only a three-terminal device, it is not possible to provide true remote sensing of the output voltage at the load. Figure 4 shows that the best load regulation is achieved when the bottom side of R2 is connected to the load and the top side of R1 resistor is connected directly to the case or the V_{OUT} pin of the regulator and not to the load. In fact, if R1 is connected to the load side, the effective resistance between the regulator and the load is multiplied by the factor of (1+R2/R1), or the effective resistance will be $R_{P(eff)} = R_P \times (1+R2/R1)$. It is important to note that for high current applications, this can represent a significant percentage of the overall load regulation and one must keep the path from the regulator to the load as short as possible to minimize this effect.

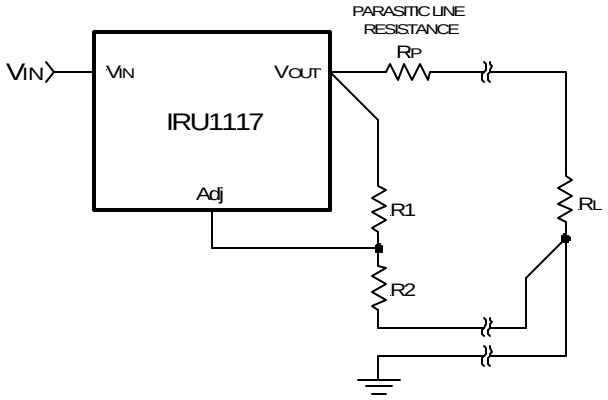


Figure 4 - Schematic showing connection for best load regulation.

Stability

The IRU1117 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for microprocessor applications use standard electrolytic capacitors with a typical ESR in the range of 50 to 100mΩ and an output capacitance of 500 to 1000µF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1117 takes advantage of this phenomenon in making the overall regulator loop stable. For most applications a minimum of 100µF aluminum electrolytic capacitor such as Sanyo MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response.

Thermal Design

The IRU1117 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the maximum allowable junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the heat sink be selected such that during maximum continuous load operation the junction temperature is kept below this number. The example below for a SCSI terminator application shows the steps in selecting the proper regulator in a surface-mount package. (See IRU1015 for non-surface-mount packages)

Assuming the following specifications:

V_{IN} = 5V
V_F = 0.5V
V_{OUT} = 2.85V
$I_{OUT(MAX)}$ = 0.8A
T_A = 35°C

Where:
V_F is the forward voltage drop of the D1 diode as shown in Figure 5.

+5V is significantly more than required to maintain drop-out voltage across the IRU1117 when regulating V_{OUT} to 2.85V. The "Extra" voltage means additional power is dissapated in the IRU1117. The diode dissapates some of this additional power, allowing the IRU1117 to run cooler.

The steps for selecting the right package with proper board area for heat sinking to keep the junction temperature below 135°C is given as:

1) Calculate the maximum power dissipation using:

$$P_D = I_{OUT} \times (V_{IN} - V_F - V_{OUT})$$
$$P_D = 0.8 \times (5 - 0.5 - 2.85) = 1.32W$$

2) Calculate the maximum θ_{JA} allowed for our example:

$$\theta_{JA(MAX)} = \frac{T_J - T_A}{P_D} = \frac{135 - 35}{1.32} = 75.6°C/W$$

3) Select a package from the data sheet with lower θ_{JA} than the one calculated in the previous step.

Selecting TO-252 (D-Pak) with at least 0.5" square of 0.062" FR4 board using 1oz. copper has 70°C/W which is lower than the calculated number.

To set the output DC voltage, we need to select R1 and R2:

4) Assuming R1 = 121Ω, 1%:

$$R2 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R1 = \left(\frac{2.85}{1.25} - 1\right) \times 121 = 154.8\Omega$$

Select R2 = 154Ω, 1%

5) Calculate the power dissapation for the schottky diode (D1):

$$P_D = V_F \times I_{OUT}$$
$$P_D = 0.5 \times 0.8 = 0.4W$$

and select a suitable component.

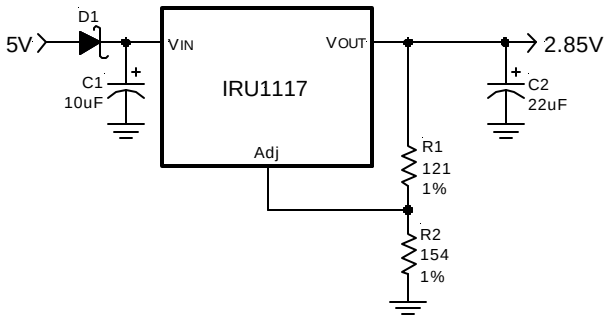


Figure 5 - Final Schematic for half of the GTL+ termination regulator.

Layout Consideration

The output capacitors must be located as close to the V_{OUT} terminal of the device as possible. It is recommended to use a section of a layer of the PC board as a plane to connect the V_{OUT} pin to the output capacitors to prevent any high frequency oscillation that may result due to excessive trace inductance.

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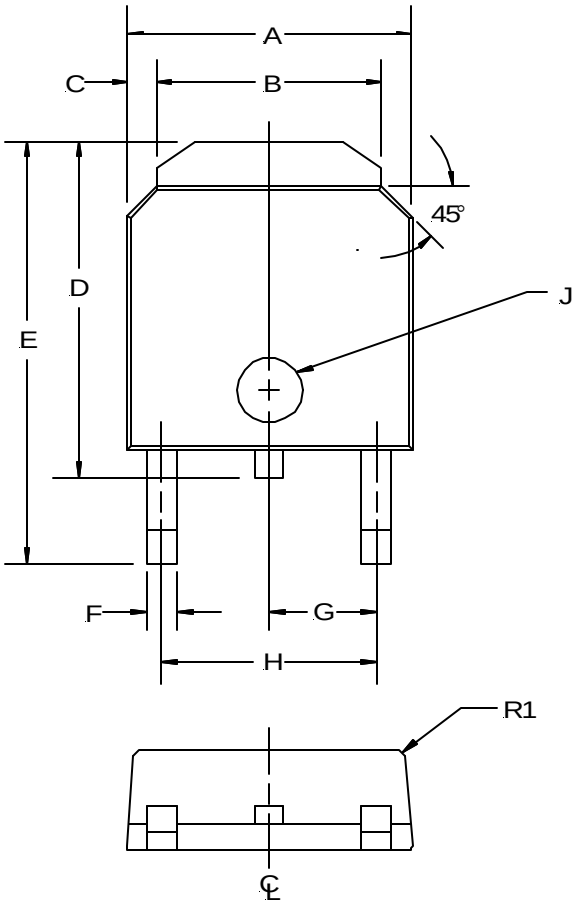
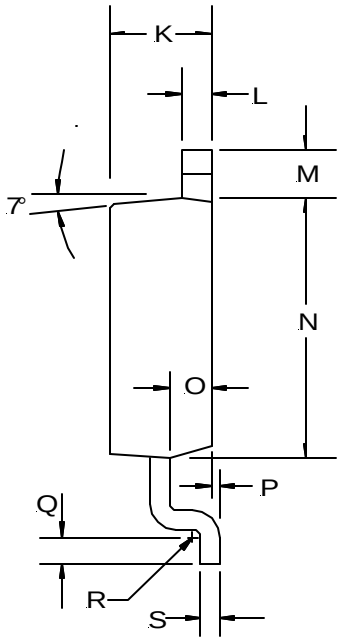
(D) TO-252 Package
2-Pin

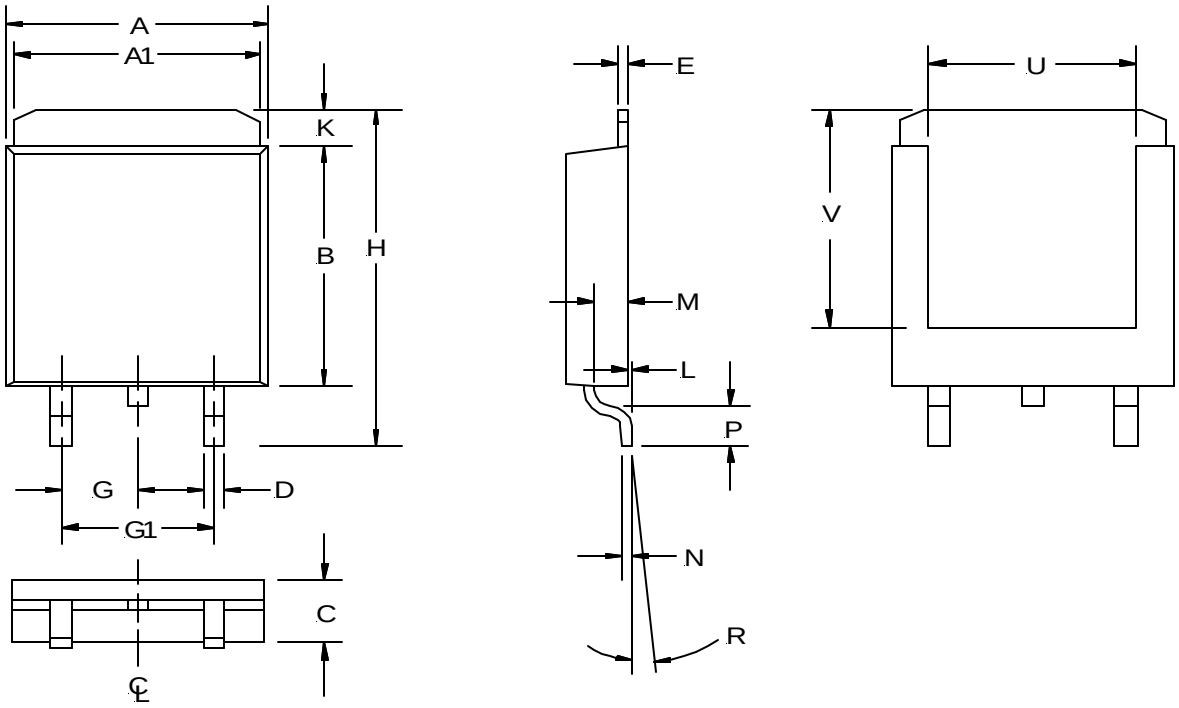




SYMBOL	MIN	MAX
A	6.477	6.731
B	5.004	5.207
C	0.686	0.838
D	7.417	8.179
E	9.703	10.084
F	0.635	0.889
G	2.286 BSC	
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

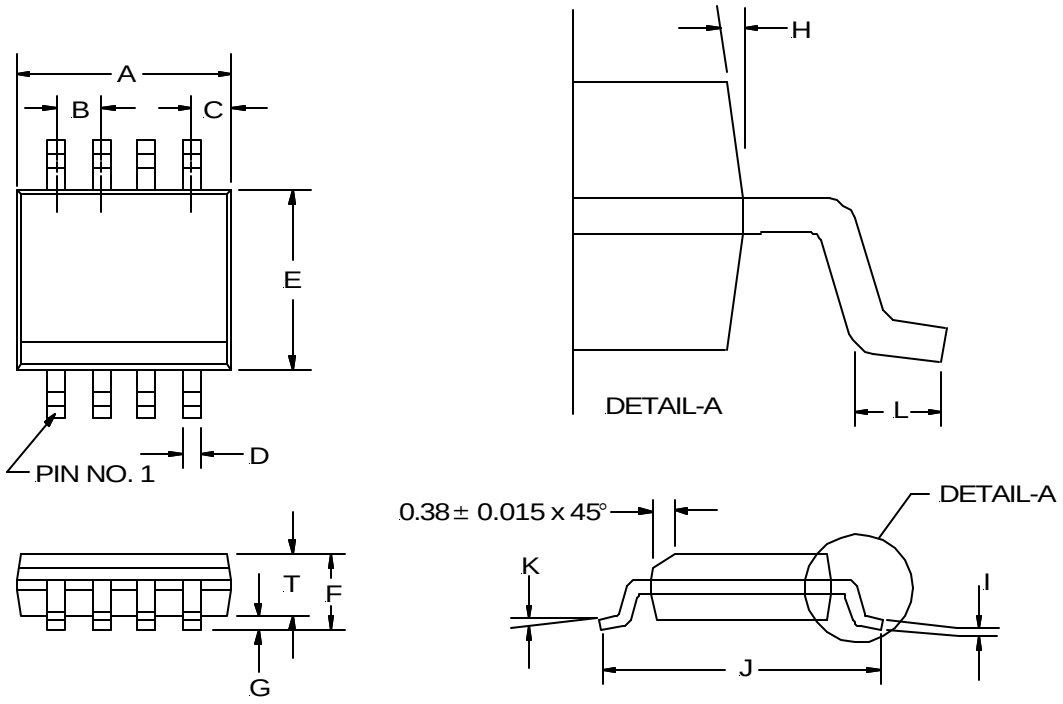
(P) Ultra Thin-Pak™
2-Pin



SYMBOL	MIN	MAX
A	5.91	6.17
A1	5.54	5.79
B	6.02	6.27
C	1.70	2.03
D	0.63	0.79
E	0.17	0.33
G	2.16	2.41
G1	4.45	4.70
H	9.42	9.68
K	0.76	1.27
L	0.02	0.13
M	0.89	1.14
N	0.25	0.25
P	0.94	1.19
R	2°	6°
U	2.92	3.30
V	5.08 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

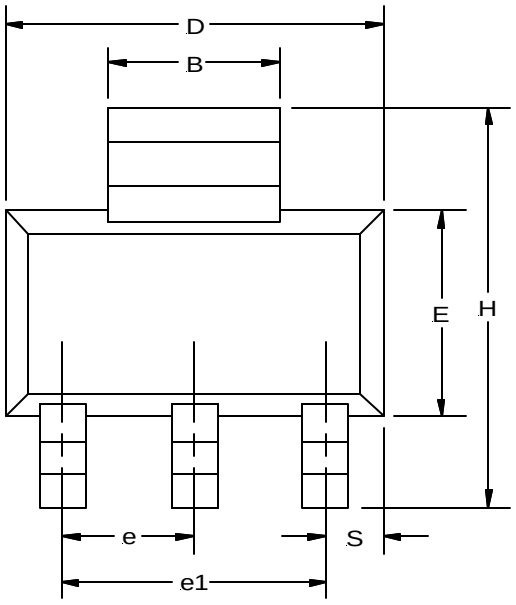
(S) SOIC Package
8-Pin Surface Mount, Narrow Body



8-PIN		
SYMBOL	**MIN**	**MAX**
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

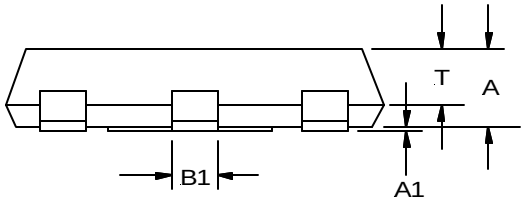
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

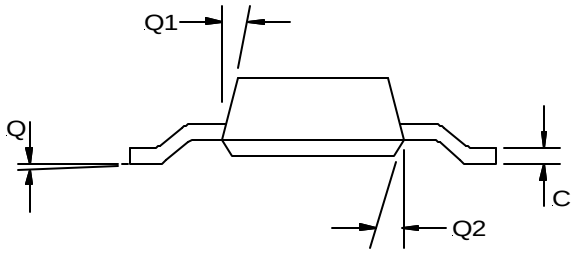
(Y) SOT-223 Package
3-Pin



SYMBOL	MIN	MAX
A	1.498	1.702
A1	0.02	0.11
B	2.895	3.15
B1	0.637	0.85
C	0.239	0.381
D	6.299	6.706
E	3.30	3.708
e	2.209	2.953
e1	4.496	4.699
H	6.70	7.30
Q	0°	10°
Q1	7°	16°
Q2	7°	16°
S	0.838	1.05
T	1.092	1.30

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.





PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
P	Ultra Thin-Pak™	2	75	2500	Fig B
S	SOIC, Narrow Body	8	95	2500	Fig C
Y	SOT-223	3	80	2500	Fig D

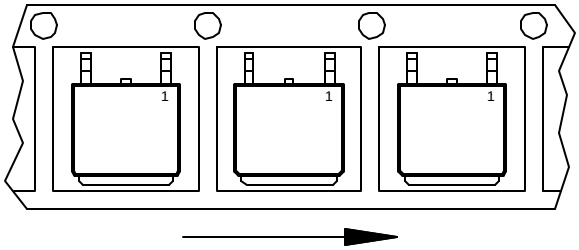


Figure A

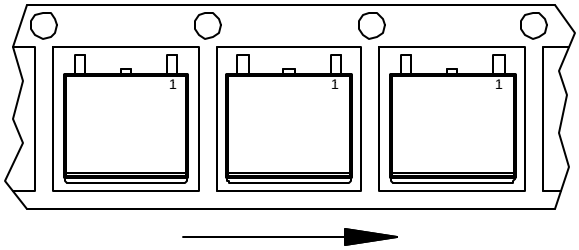


Figure B

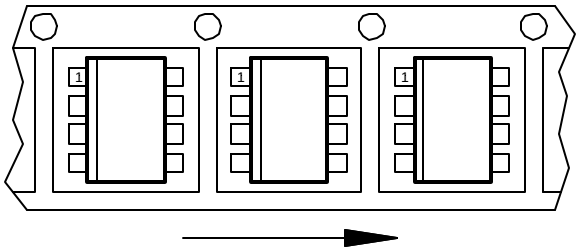


Figure C

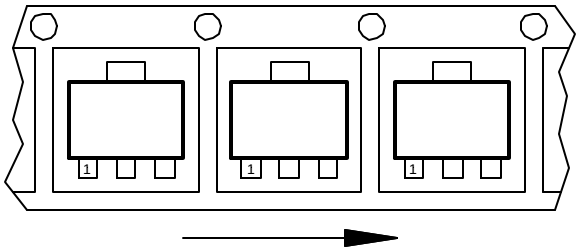


Figure D

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IRU1117-18

800mA LOW DROPOUT POSITIVE FIXED 1.8V REGULATOR

FEATURES

- Guaranteed < 1.2V Dropout at 800mA Load Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown
- Available in SOT-223, D-Pak, Ultra Thin-Pak™ and 8-Pin SOIC Surface-Mount Packages

APPLICATIONS

- Low Voltage IC Supply Applications
- PC Clock Supply Voltage

DESCRIPTION

The IRU1117-18 is a low dropout three-terminal fixed output regulator with minimum of 800mA output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications as well as generating clock supply for PC applications. The IRU1117-18 is guaranteed to have <1.2V dropout at full load current making it ideal to provide well regulated with 3.8V input supply. The IRU1117-18 is specifically designed to be stable with low cost aluminum capacitors while maintaining stability with low ESR tantalum caps.

TYPICAL APPLICATION

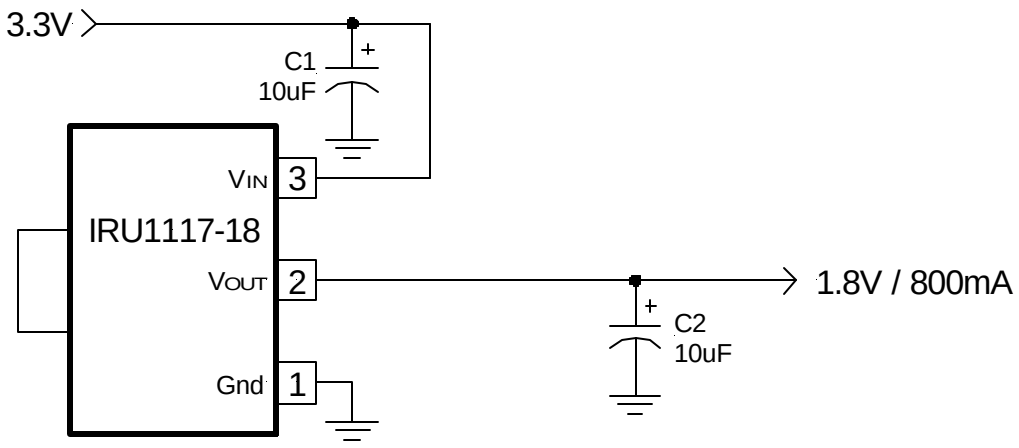


Figure 1 - Typical set-up of the IRU1117-18 in a 3.3V to 1.8V regulator application.

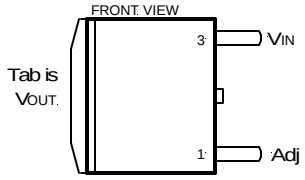
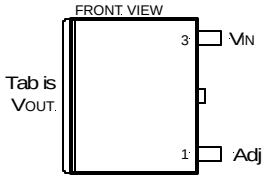
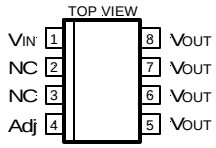
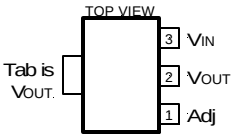
PACKAGE ORDER INFORMATION

T_J (°C)	2-PIN PLASTIC TO-252 (D-Pak)	2-PIN PLASTIC Ultra Thin-Pak™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SOT-223 (Y)
0 To 125	IRU1117-18CD	IRU1117-18CP	IRU1117-18CS	IRU1117-18CY

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)	2-PIN ULTRA THIN-PAK™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SOT-223 (Y)
			
θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=55°C/W for 1" Sq pad	θ_{JA}=90°C/W for 0.4" Sq pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, V_{IN}=5V, C_{OUT}=10µF, and T_J=0 to 125°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	V_O	Io=10mA, T_J=25°C	1.782	1.800	1.818	V
		Io=10mA	1.764	1.800	1.896	
Line Regulation		Io=10mA, 4.75V<V_{IN}<7V			7	mV
Load Regulation (Note 1)		10mA<Io<800mA			17	mV
Dropout Voltage (Note 2)		Io=1A		1.2	1.3	V
		Io=800mA		1.1	1.2	
Current Limit		ΔVo=100mV	1.1			A
Thermal Regulation		30ms Pulse, Io=800mA		0.01		%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum,				
		Io=0.5A		70		dB
Temperature Stability		Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3		%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%V_O

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Gnd	Ground pin. This pin must be connected to ground plane using a low inductance short connection.
2	V_{OUT}	The output of the regulator. This pin is also connected to the tab of the package. An output capacitor must be connected to this pin to insure stability of the regulator.
3	V_{IN}	Input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum dropout voltage during the load transient response. This pin must always be 1.3V higher than V_{OUT} in order for the device to regulate properly.

BLOCK DIAGRAM

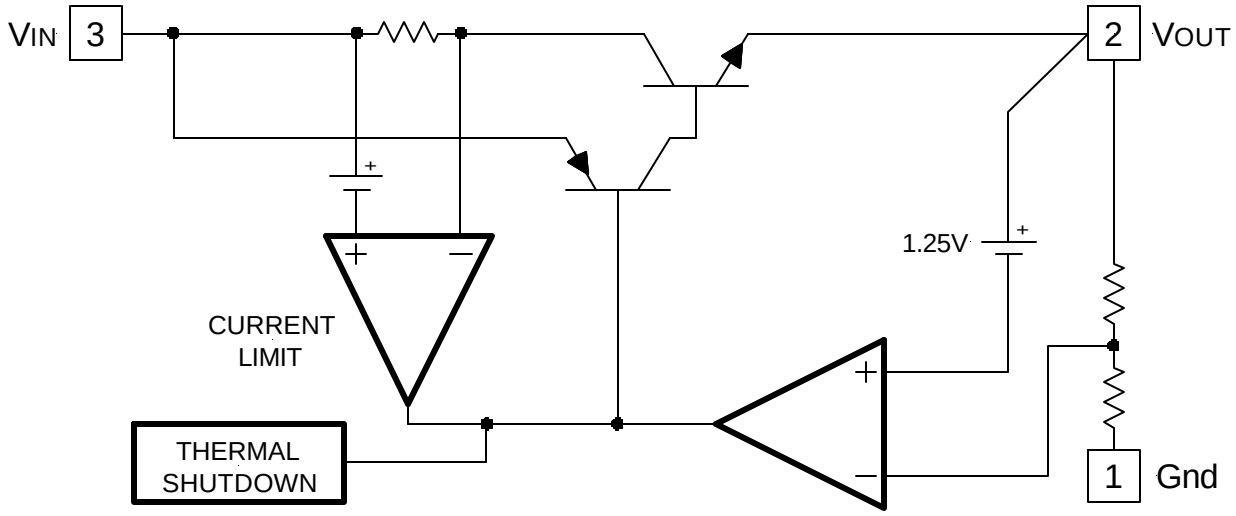


Figure 2 - Simplified block diagram of the IRU1117-18.

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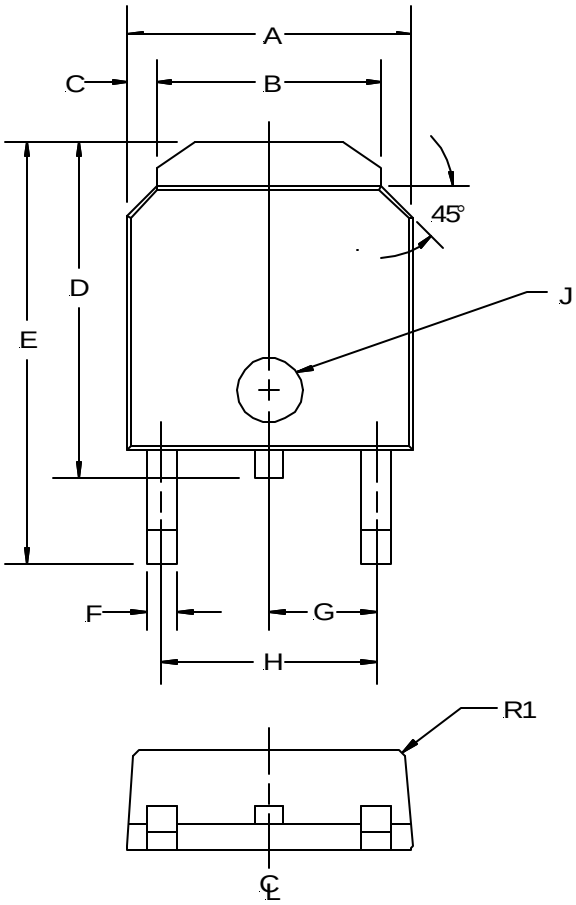
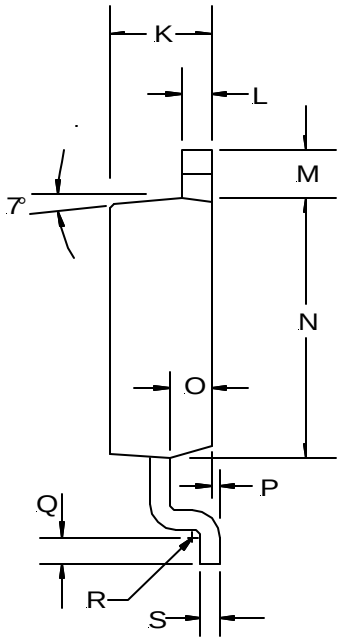
(D) TO-252 Package
2-Pin

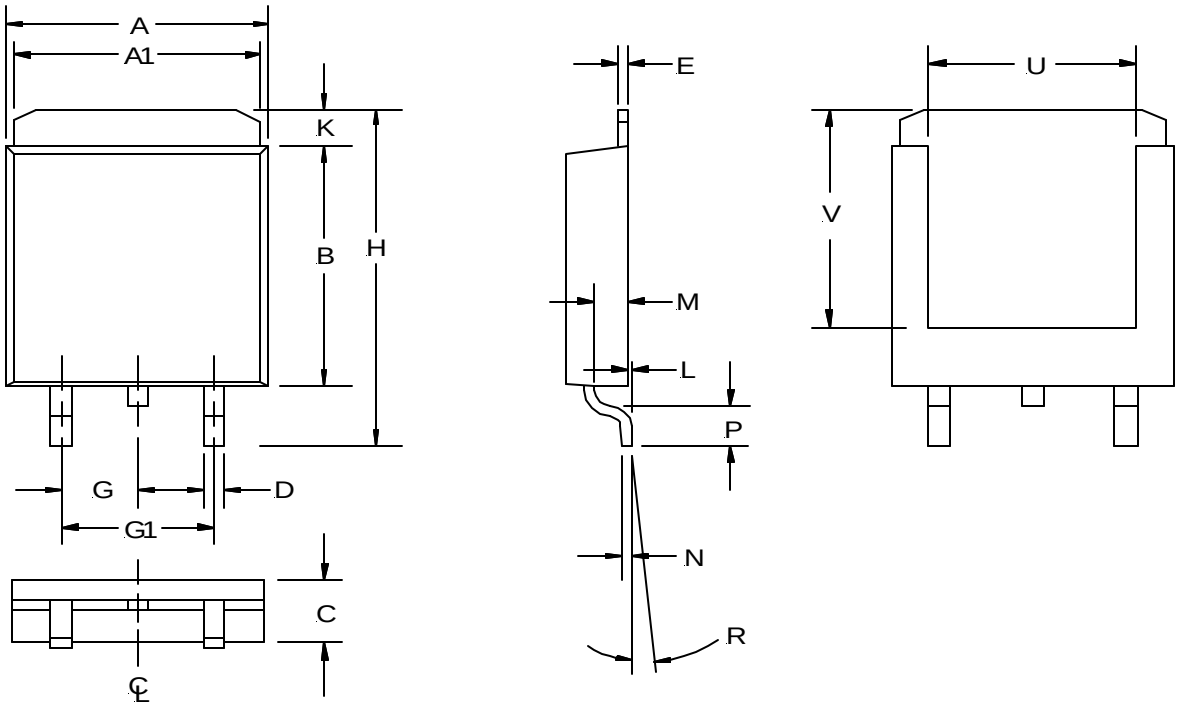




SYMBOL	MIN	MAX
A	6.477	6.731
B	5.004	5.207
C	0.686	0.838
D	7.417	8.179
E	9.703	10.084
F	0.635	0.889
G	2.286 BSC	
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

(P) Ultra Thin-Pak™
2-Pin



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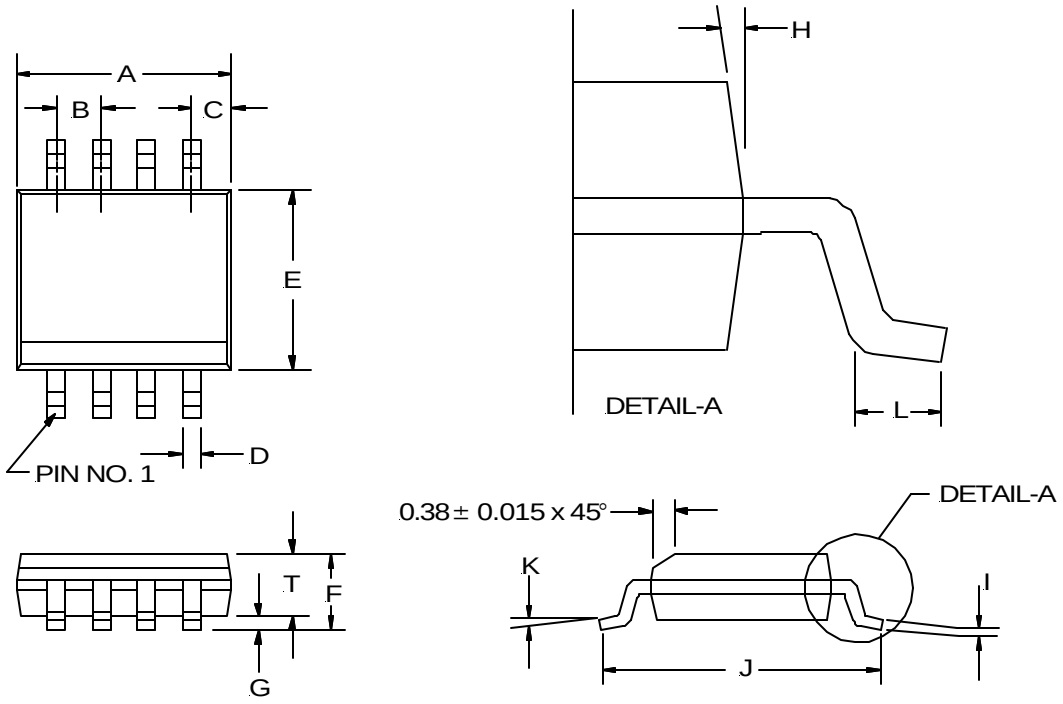
K	0.76	1.27
L	0.02	0.13
M	0.89	1.14
N	0.25	0.25
P	0.94	1.19
R	2°	6°
U	2.92	3.30
V	5.08 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(S) SOIC Package
8-Pin Surface Mount, Narrow Body



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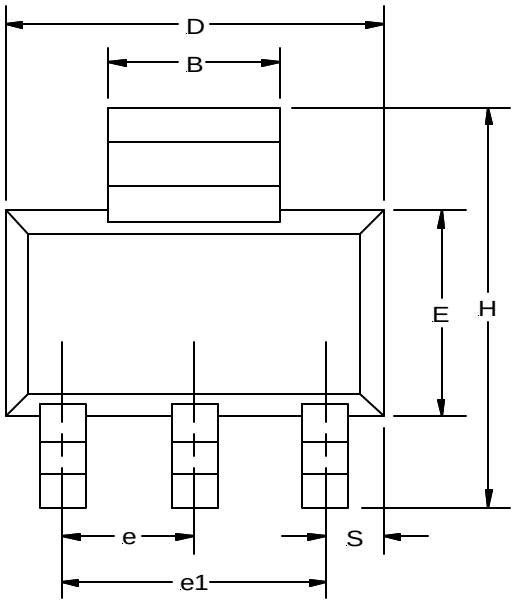
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(Y) SOT-223 Package
3-Pin



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A1	0.02	0.11
B	2.895	3.15
B1	0.637	0.85
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e1	4.496	4.699
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Q1	7°	16°
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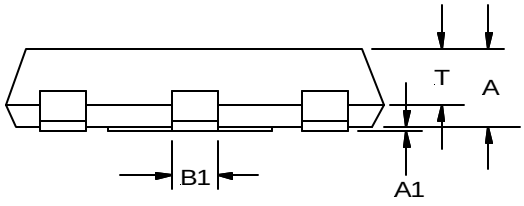
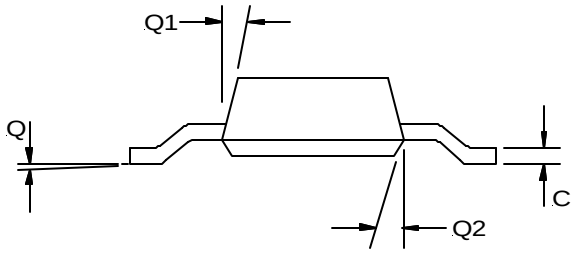
NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.





PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
P	Ultra Thin-Pak™	2	75	2500	Fig B
S	SOIC, Narrow Body	8	95	2500	Fig C
Y	SOT-223	3	80	2500	Fig D

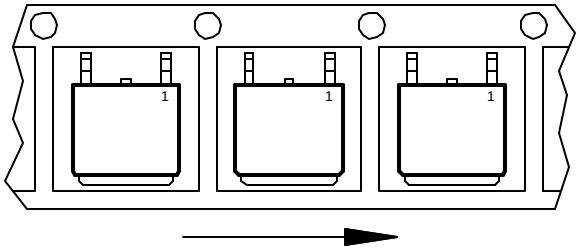


Figure A

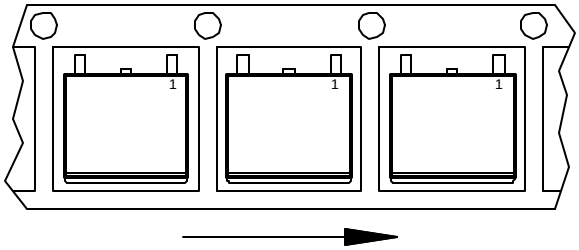


Figure B

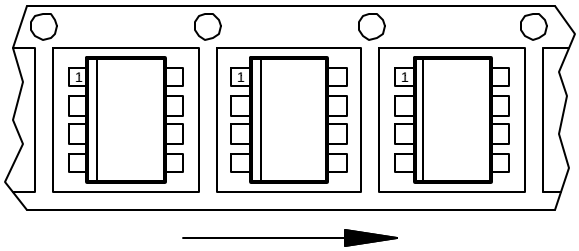


Figure C

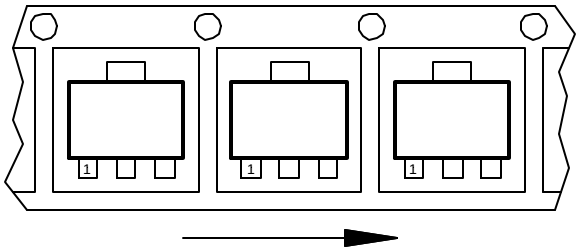


Figure D

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IRU1117-25

800mA LOW DROPOUT POSITIVE FIXED 2.5V REGULATOR

FEATURES

- Guaranteed < 1.2V Dropout at 800mALoad Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown
- Available in SOT-223, D-Pak, Ultra Thin-Pak™ and 8-Pin SOIC Surface-Mount Packages

APPLICATIONS

- Low Voltage IC Supply Applications
- PC Clock Supply Voltage

DESCRIPTION

The IRU1117-25 is a low dropout three-terminal fixed output regulator with minimum of 800mA output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications as well as generating clock supply for PC applications. The IRU1117-25 is guaranteed to have <1.2V dropout at full load current making it ideal to provide well regulated with 3.8V input supply. The IRU1117-25 is specifically designed to be stable with low cost aluminum capacitors while maintaining stability with low ESR tantalum caps.

TYPICAL APPLICATION

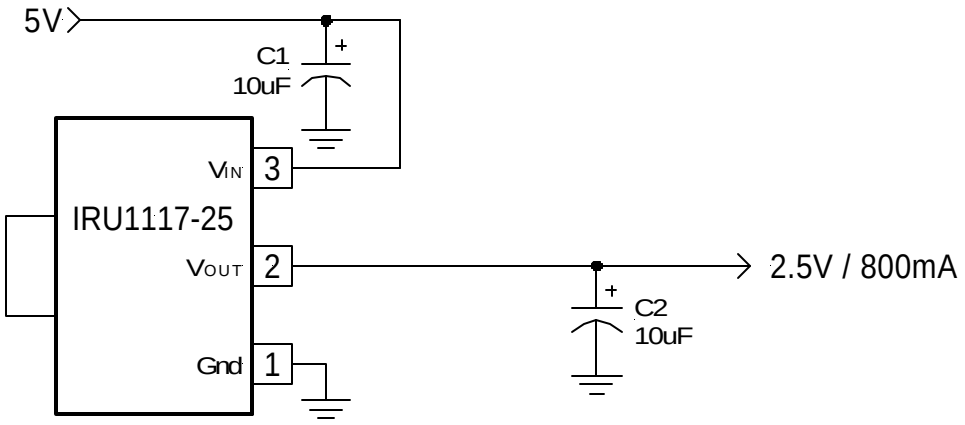


Figure 1 - Typical application of IRU1117-25 in a 5V to 2.5V regulator.

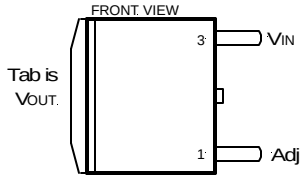
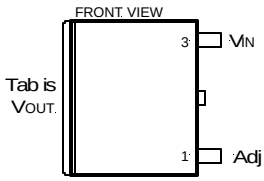
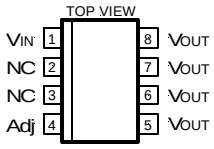
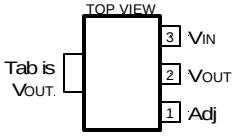
PACKAGE ORDER INFORMATION

TJ (°C)	2-PIN PLASTIC TO-252 (D-Pak)	2-PIN PLASTIC Ultra Thin-Pak™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SOT-223 (Y)
0 To 150	IRU1117-25CD	IRU1117-25CP	IRU1117-25CS	IRU1117-25CY

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)	2-PIN ULTRA THIN-PAK™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SOT-223 (Y)
			
θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=55°C/W for 1" Sq pad	θ_{JA}=90°C/W for 0.4" Sq pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, V_{IN}=5V, C_{OUT}=10µF, and T_J=0 to 125°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	V_O	Io=10mA, T_J=25°C	2.475	2.500	2.525	V
		Io=10mA	2.450	2.500	2.550	
Line Regulation		Io=10mA, 4.75V<V_{IN}<7V			7	mV
Load Regulation (Note 1)		10mA<Io<800mA			17	mV
Dropout Voltage (Note 2)		Io=1A		1.2	1.3	V
		Io=800mA		1.1	1.2	
Current Limit		ΔVo=100mV	1.1			A
Thermal Regulation		30ms Pulse, Io=800mA		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum,				
		Io=0.5A		70		dB
Temperature Stability		Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%V_O

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Gnd	Ground pin. This pin must be connected to ground plane using a low inductance short connection.
2	V_{OUT}	The output of the regulator. This pin is also connected to the tab of the package. An output capacitor must be connected to this pin to insure stability of the regulator.
3	V_{IN}	Input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum dropout voltage during the load transient response. This pin must always be 1.3V higher than V_{OUT} in order for the device to regulate properly.

BLOCK DIAGRAM

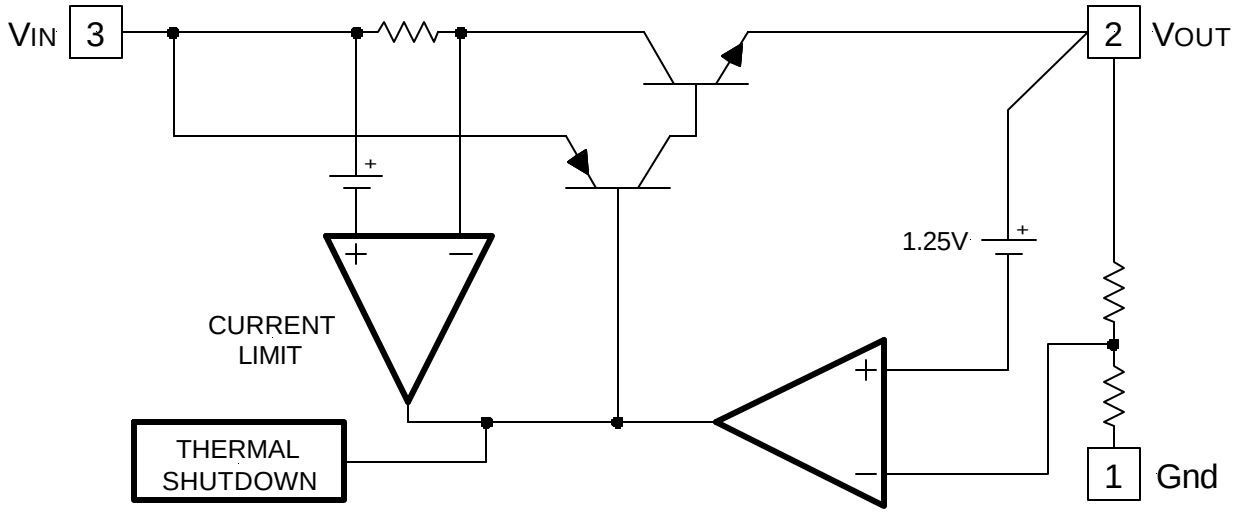


Figure 2 - Simplified block diagram of the IRU1117-25.

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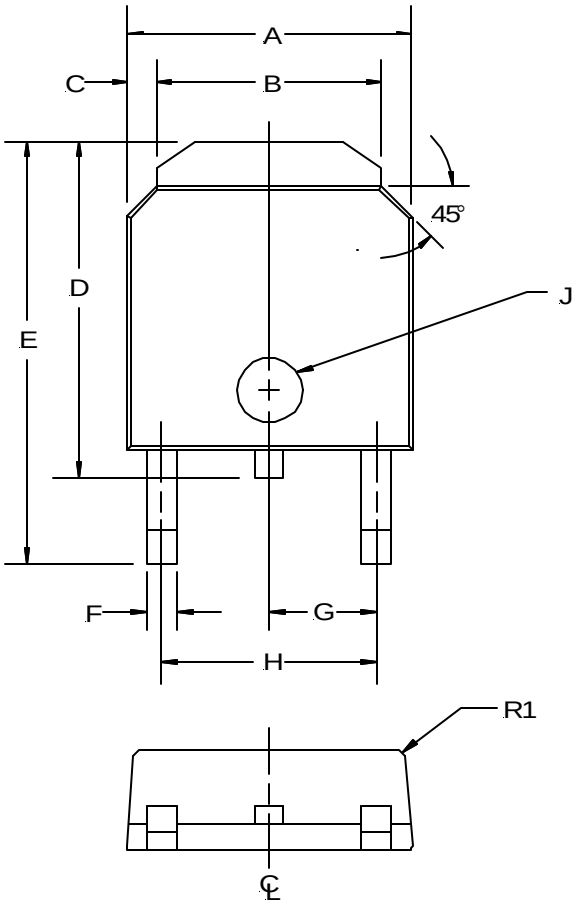
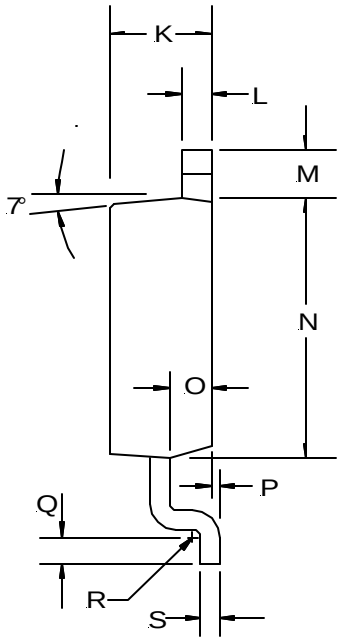
(D) TO-252 Package
2-Pin

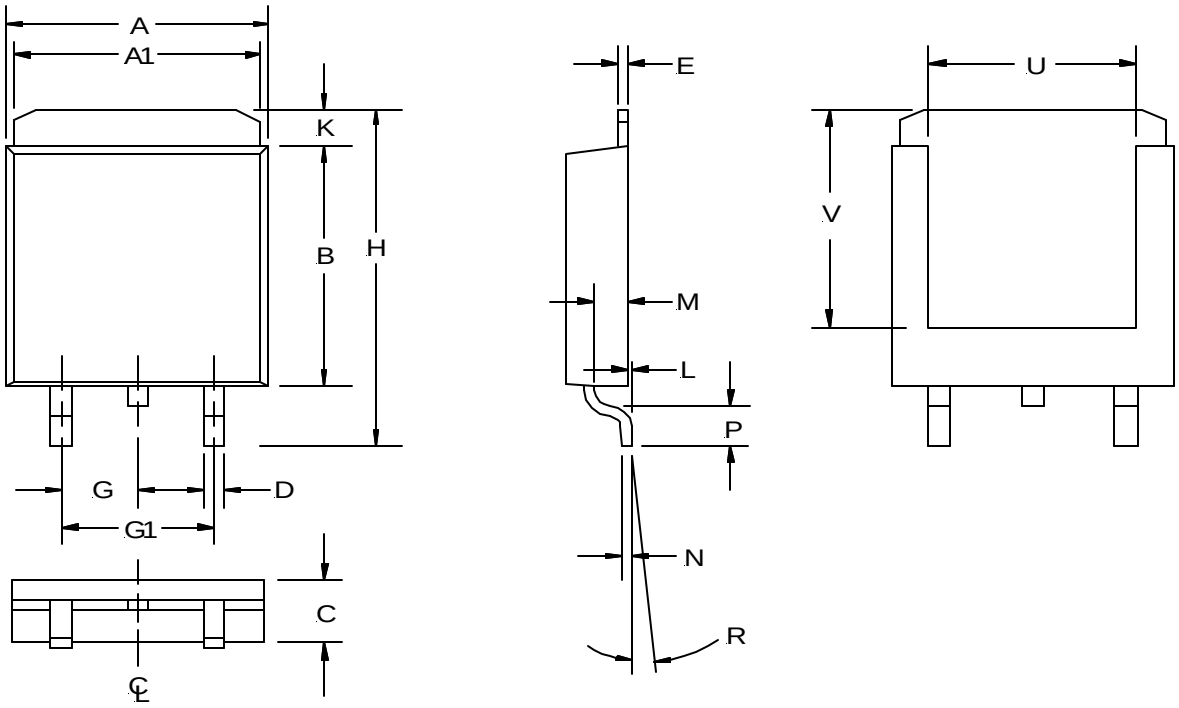




SYMBOL	MIN	MAX
A	6.477	6.731
B	5.004	5.207
C	0.686	0.838
D	7.417	8.179
E	9.703	10.084
F	0.635	0.889
G	2.286 BSC	
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

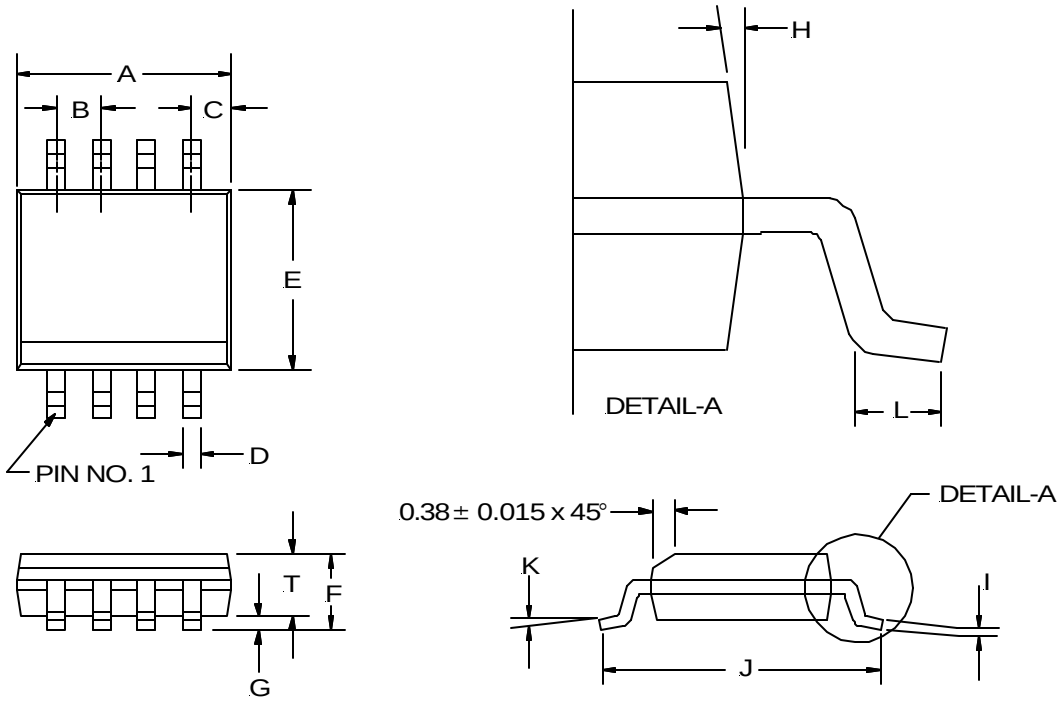
(P) Ultra Thin-Pak™
2-Pin



SYMBOL	MIN	MAX
A	5.91	6.17
A1	5.54	5.79
B	6.02	6.27
C	1.70	2.03
D	0.63	0.79
E	0.17	0.33
G	2.16	2.41
G1	4.45	4.70
H	9.42	9.68
K	0.76	1.27
L	0.02	0.13
M	0.89	1.14
N	0.25	0.25
P	0.94	1.19
R	2°	6°
U	2.92	3.30
V	5.08 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

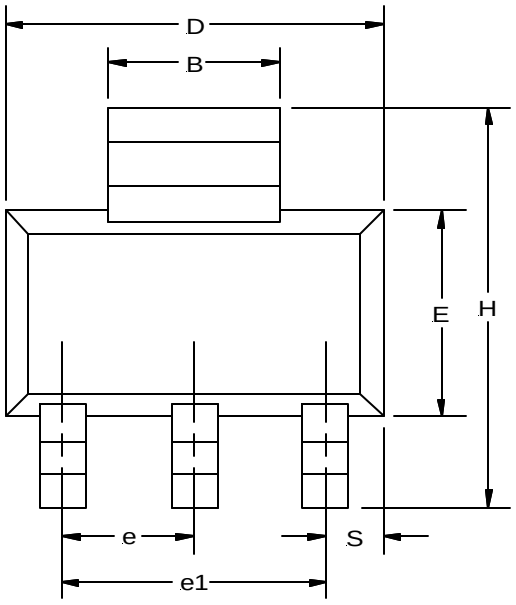
(S) SOIC Package
8-Pin Surface Mount, Narrow Body



8-PIN		
SYMBOL	**MIN**	**MAX**
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

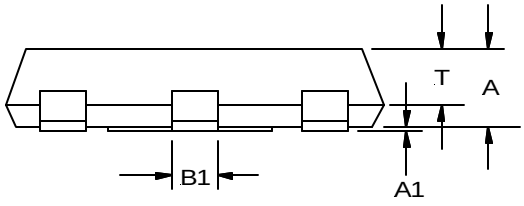
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

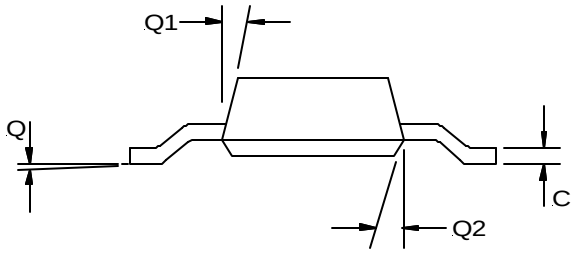
(Y) SOT-223 Package
3-Pin



SYMBOL	MIN	MAX
A	1.498	1.702
A1	0.02	0.11
B	2.895	3.15
B1	0.637	0.85
C	0.239	0.381
D	6.299	6.706
E	3.30	3.708
e	2.209	2.953
e1	4.496	4.699
H	6.70	7.30
Q	0°	10°
Q1	7°	16°
Q2	7°	16°
S	0.838	1.05
T	1.092	1.30

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.





PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
P	Ultra Thin-Pak™	2	75	2500	Fig B
S	SOIC, Narrow Body	8	95	2500	Fig C
Y	SOT-223	3	80	2500	Fig D

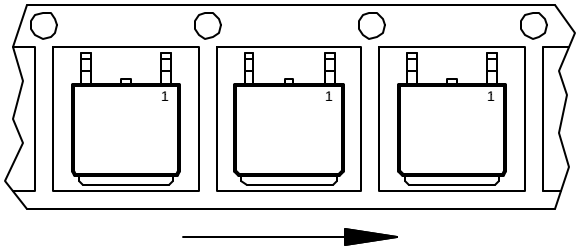


Figure A

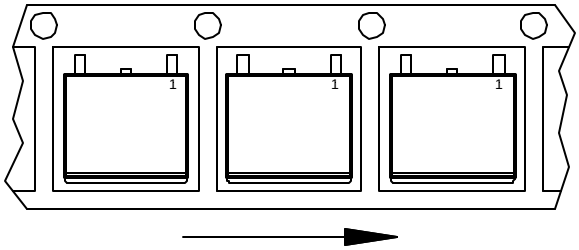


Figure B

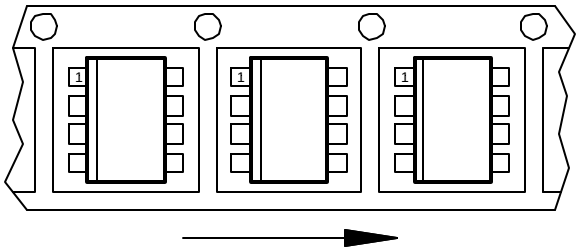


Figure C

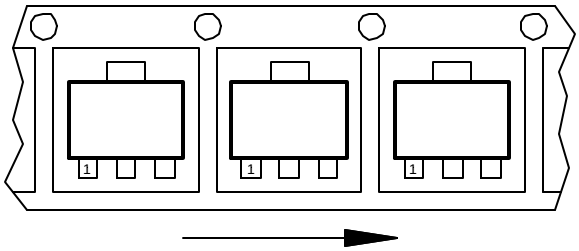


Figure D

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IRU1117-33

800mA LOW DROPOUT POSITIVE FIXED 3.3V REGULATOR

FEATURES

- Guaranteed < 1.2V Dropout at 800mA Load Current
- Fast Transient Response
- 1% Output Voltage Initial Accuracy
- Built-In Thermal Shutdown
- Available in SOT-223, D-Pak, Ultra Thin-Pak™ and 8-Pin SOIC Surface-Mount Packages

APPLICATIONS

- VGA & Sound Card Applications
- Standard 3.3V Chip Set and Logic Applications

DESCRIPTION

The IRU1117-33 is a low dropout three-terminal fixed output regulator with minimum of 800mA output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications such as VGA, sound & DVD cards. The IRU1117-33 is guaranteed to have <1.2V dropout at full load current making it ideal to provide well regulated with 4.75V to 7V input supply. The IRU1117-33 is specifically designed to be stable with low cost aluminum capacitors while maintaining stability with low ESR tantalum caps.

TYPICAL APPLICATION

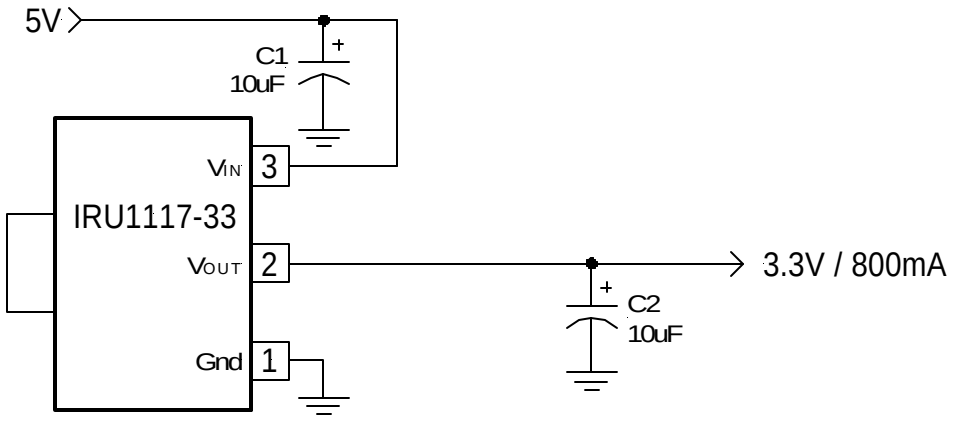


Figure 1 - Typical application of IRU1117-33 in a 5V to 3.3V regulator.

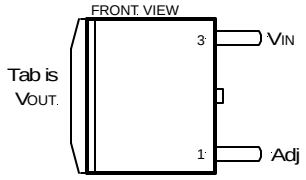
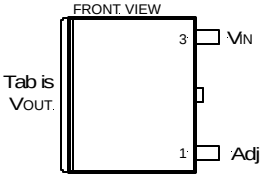
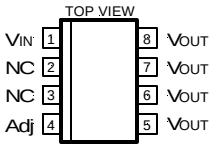
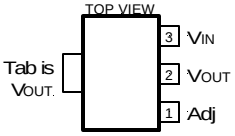
PACKAGE ORDER INFORMATION

T_J (°C)	2-PIN PLASTIC TO-252 (D-Pak)	2-PIN PLASTIC Ultra Thin-Pak™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SOT-223 (Y)
0 To 150	IRU1117-33CD	IRU1117-33CP	IRU1117-33CS	IRU1117-33CY

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)	2-PIN ULTRA THIN-PAK™ (P)	8-PIN PLASTIC SOIC (S)	3-PIN PLASTIC SOT-223 (Y)
			
θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=70°C/W for 0.5" Sq pad	θ_{JA}=55°C/W for 1" Sq pad	θ_{JA}=90°C/W for 0.4" Sq pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, V_{IN}=5V, C_{OUT}=10µF, and T_J=0 to 125°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	V_O	Io=10mA, T_J=25°C	3.267	3.300	3.333	V
		Io=10mA	3.235	3.300	3.365	
Line Regulation		Io=10mA, 4.75V<V_{IN}<7V			7	mV
Load Regulation (Note 1)		10mA<Io<800mA			17	mV
Dropout Voltage (Note 2)		Io=1A			1.3	V
		Io=800mA			1.2	
Current Limit		ΔVo=100mV	1.1			A
Thermal Regulation		30ms Pulse, Io=800mA		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum,				
		Io=0.5A	60	70		dB
Temperature Stability		Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%V_O

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

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BLOCK DIAGRAM

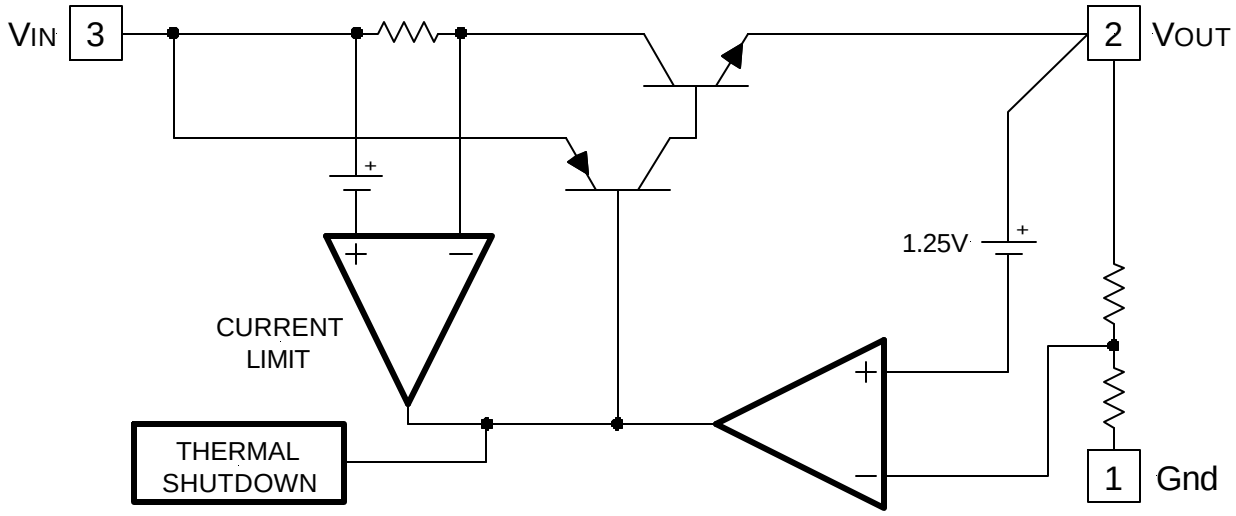

Figure 2 - Simplified block diagram of the IRU1117-33.

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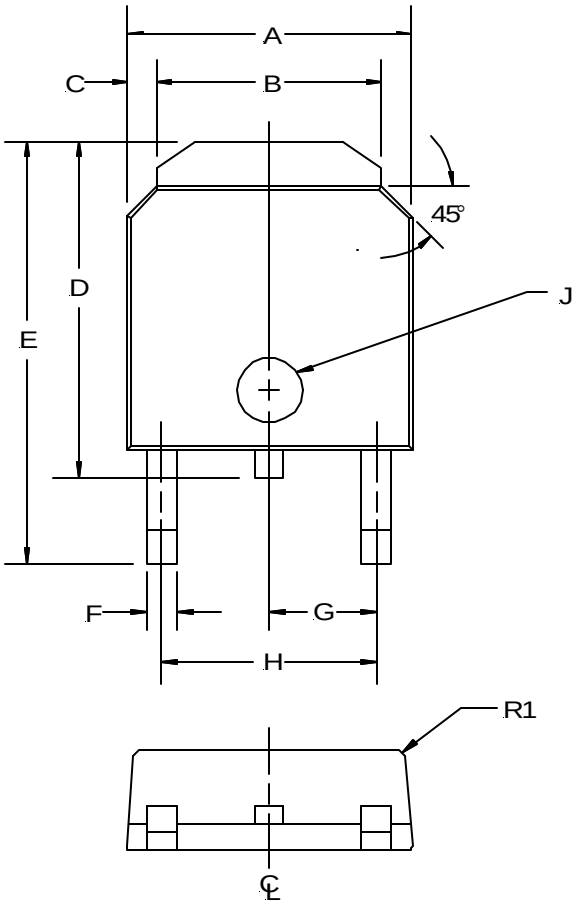
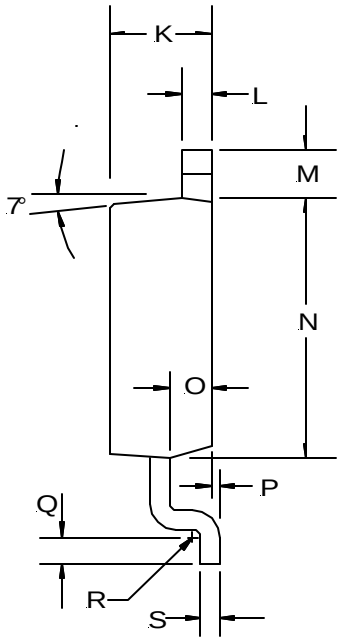
(D) TO-252 Package
2-Pin





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E	9.703	10.084
F	0.635	0.889
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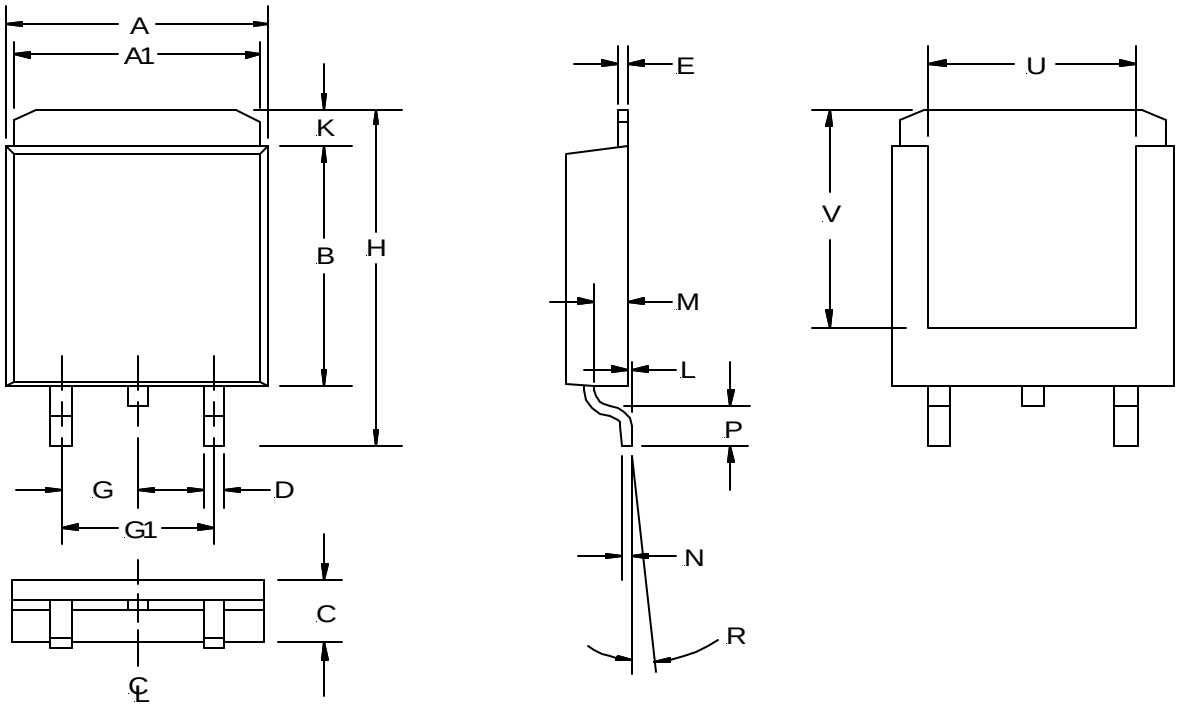
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

(P) Ultra Thin-Pak™
2-Pin



SYMBOL	MIN	MAX
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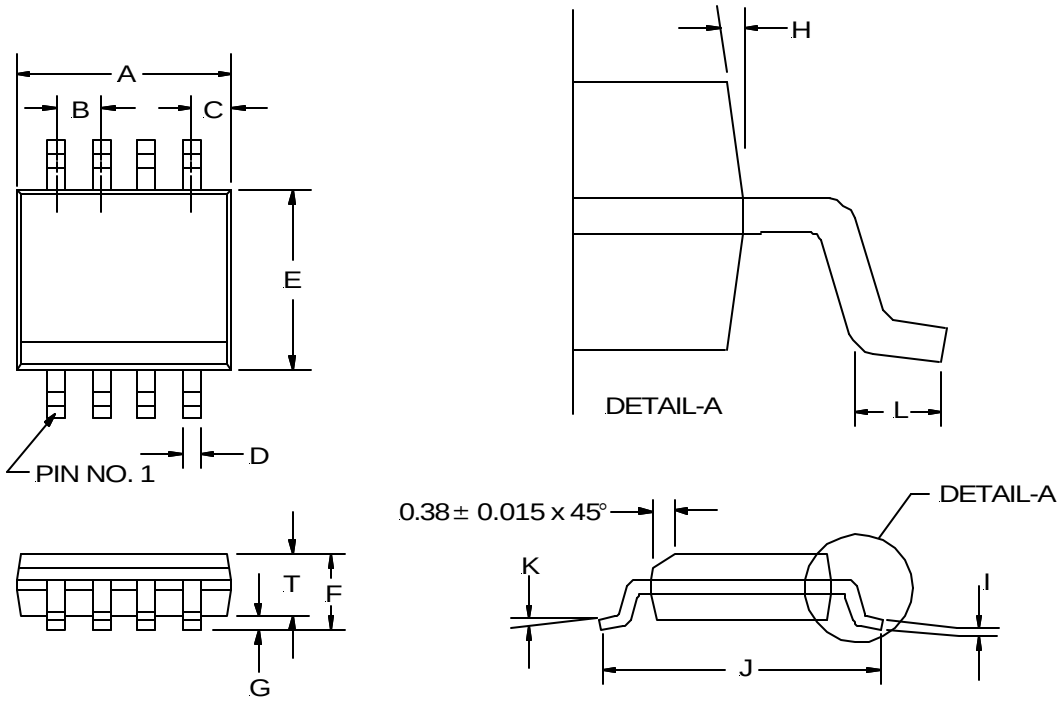
B	6.02	6.27
C	1.70	2.03
D	0.63	0.79
E	0.17	0.33
G	2.16	2.41
G1	4.45	4.70
H	9.42	9.68
K	0.76	1.27
L	0.02	0.13
M	0.89	1.14
N	0.25	0.25
P	0.94	1.19
R	2°	6°
U	2.92	3.30
V	5.08 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

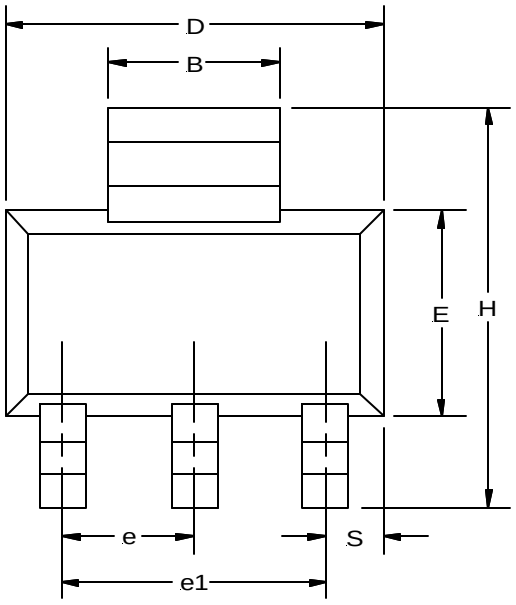
(S) SOIC Package
8-Pin Surface Mount, Narrow Body



8-PIN		
SYMBOL	**MIN**	**MAX**
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

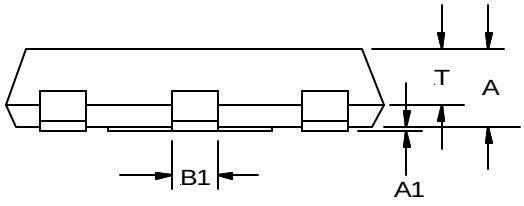
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

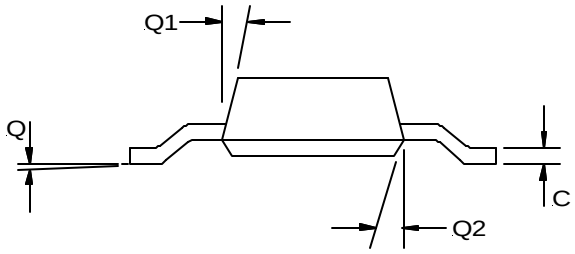
(Y) SOT-223 Package
3-Pin



SYMBOL	MIN	MAX
A	1.498	1.702
A1	0.02	0.11
B	2.895	3.15
B1	0.637	0.85
C	0.239	0.381
D	6.299	6.706
E	3.30	3.708
e	2.209	2.953
e1	4.496	4.699
H	6.70	7.30
Q	0°	10°
Q1	7°	16°
Q2	7°	16°
S	0.838	1.05
T	1.092	1.30

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.





PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
P	Ultra Thin-Pak™	2	75	2500	Fig B
S	SOIC, Narrow Body	8	95	2500	Fig C
Y	SOT-223	3	80	2500	Fig D

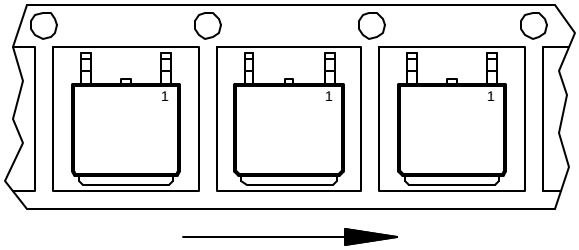


Figure A

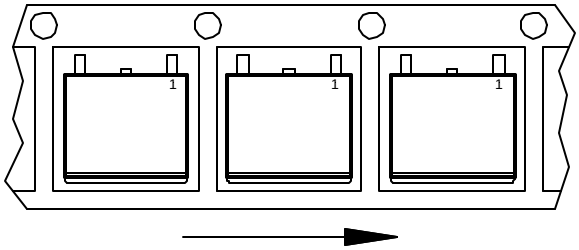


Figure B

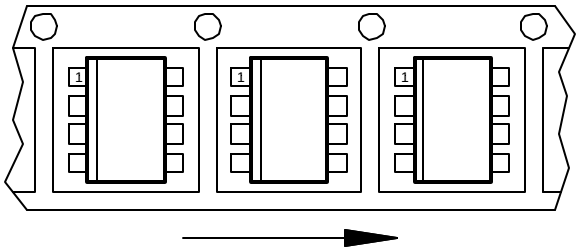


Figure C

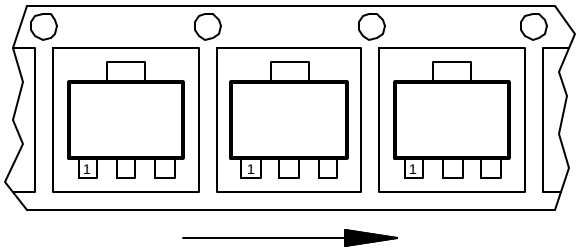


Figure D

International
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IRU1120

2A LOW DROPOUT POSITIVE ADJUSTABLE REGULATOR

PRELIMINARY DATA SHEET

FEATURES

- **Stable with ceramic capacitor**
- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- 2% Voltage Reference Initial Accuracy
- Output Current Limiting
- Built-In Thermal Shutdown

APPLICATIONS

- High Efficiency Linear Regulator
- Hard Disk Drivers, CD-ROMs, DVDs
- ADSL and Cable Modems

DESCRIPTION

The IRU1120 is an adjustable linear voltage regulator. It is packaged in a 5-pin ultra thin-pak surface mount package. The adjustable output voltage can be set from 1.25V and up using a simple resistor divider. The input power can be supplied by a single 5V supply. The regulator is capable of supplying 2 Amps of continuous current with an input voltage of 5V. The output is protected by both current limit and thermal shutdown circuits.

TYPICAL APPLICATION

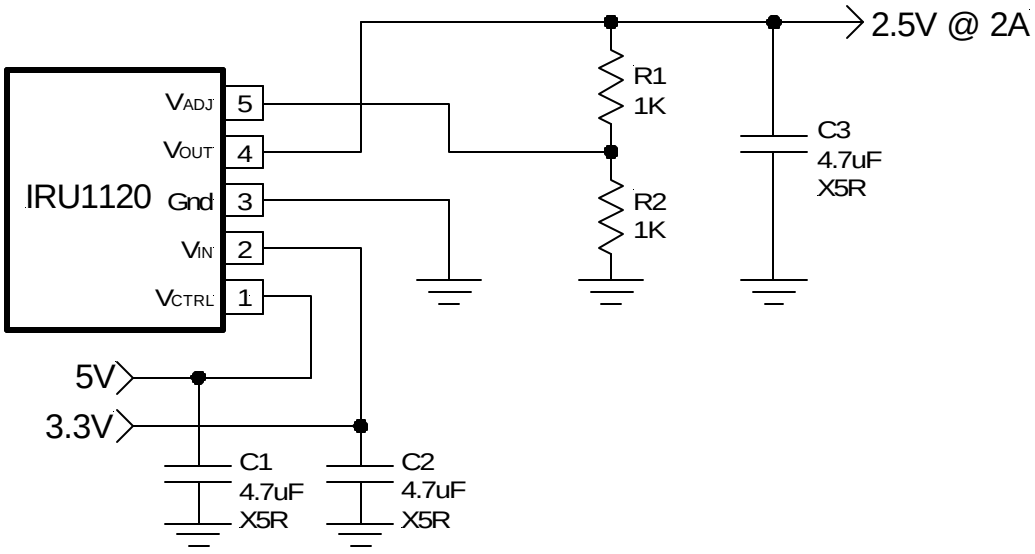


Figure 1 - Typical application of IRU1120.

PACKAGE ORDER INFORMATION

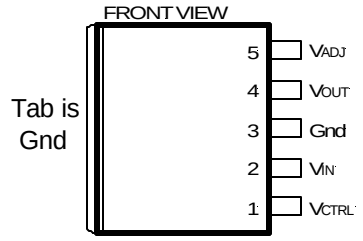
T_A (°C)	DEVICE	PACKAGE	OUTPUT
0 To 125	IRU1120CP	5-Pin Ultra Thin-Pak™ (P)	Adjustable

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 10V
Input Voltage (V_{CTRL}) 10V
Operating Junction Temperature Range ..... -40°C To 150°C
Operating Ambient Temperature Range ..... -40°C To 125°C
Storage Temperature Range ..... -65°C To 150°C

PACKAGE INFORMATION

5-Pin Ultra Thin-Pak™ (P)



θ_{JA}=30°C/W for 1" Square Pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=C_{CTRL}=C_{OUT}=4.7µF. Typical values refer to T_J=25°C unless otherwise noted. I_{FL}=2A. V_{ADJ} is connected to V_{OUT} and V_{IN}=V_{CTRL}=5V unless otherwise noted.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}	Io=10mA, T_J=25°C	1.225	1.25	1.275	V
		Io=10mA, 0°C< T_J<125°C	1.213	1.25	1.287	
Line Regulation	Reg_{LINE}	Io=10mA, Vo+1.3V<V_{IN}=V_{CTRL}<10V		0.5	0.7	%Vo
		Io=10mA, V_{IN}=V_{CTRL}=2.6 to 10V for				
		the following: 0°C< T_J<125°C		1.13	1.25	%Vo
		-40°C< T_J<125°C		1.4		
Load Regulation	Reg_{LOAD}	Note 1, 10mA<Io<2A for the				
		following: 0°C< T_J<125°C		0.2	0.4	%Vo
		-40°C< T_J<125°C		0.3		
Dropout Voltage	V_{DO1}	Note 2, Io=1A, V_{CTRL}=5V,				
		V_O+V_{DO1}<V_{IN}<3.3V for the following:				
		0°C< T_J<125°C		0.48	0.63	V
		-40°C< T_J<125°C		0.6		
Dropout Voltage	V_{DO2}	Note 2, Io=1.5A, V_{CTRL}=5V,				
		V_O+V_{DO2}<V_{IN}<3.3V for the following:				
		0°C< T_J<125°C		0.75	0.9	V
		-40°C< T_J<125°C		0.94		
Dropout Voltage	V_{DO3}	Note 2, Io=2A, V_{CTRL}=5V,				
		V_O+V_{DO3}<V_{IN}<3.3V for the following:				
		0°C< T_J<125°C		1.1	1.25	V
		-40°C< T_J<125°C		1.27		
Dropout Voltage	V_{DO4}	Note 2, Io=1A, V_{CTRL}=V_{IN} for the				
		following: 0°C< T_J<125°C		1.05	1.2	V
		-40°C< T_J<125°C		1.2		

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Dropout Voltage	V_{DO5}	Note 2, Io=1.5A, V_{CTRL}=V_{IN} for the following: 0°C< T_J<125°C		1.2	1.35	V
		-40°C< T_J<125°C		1.3		
Dropout Voltage	V_{DO6}	Note 2, Io=2A, V_{CTRL}=V_{IN} for the following: 0°C< T_J<125°C		1.35	1.5	V
		-40°C< T_J<125°C		1.44		
Current Limit	I_{OL}	ΔV_{O1}=10% Below Regulation	2.3	3	4	A
Minimum Load Current	$I_{O(min)}$	Note 3, 5		1	5	mA
Thermal Regulation	Reg_{THERM}	Note 5, 30ms pulse, Io=I_{FL}		0.1		%/W
Ripple Rejection (Vcc to Output)	PSRR	Note 5, 100Hz<f<100KHz, Io=20mA		32		dB
Temperature Stability	$Stab_{TEMP}$	Note 4, 5, Io=10mA		0.5		%Vo
Long Term Stability	$Stab_{LONG}$	Note 5		0.3		%Vo
RMS Output Noise	V_N	Note 5, 10Hz<f<10KHz		0.003		%Vo
Vcc Quiescent Current	I_{Q1}	Io=0mA		1	3	mA

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation.

Note 4: Temperature stability is the change in output from nominal over the operating temperature range.

Note 5: Guaranteed by design, but not tested in production.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	V_{CTRL}	The control input pin of the regulator. This pin is connected to the 5V supply to provide base current for the pass transistor of the regulator. This allows the regulator to have very low dropout voltage, enabling use with low values of V_{IN}. A 1µF high frequency capacitor is connected from this pin to V_{IN} to ensure stability.
2	V_{IN}	The power input pin of the regulator. A minimum of input capacitance must be connected from this pin to ground to insure that the input voltage does not sag below the minimum dropout voltage during the load transient response. This pin must always be higher than the V_{OUT} pin by the amount of dropout voltage (see data sheet) in order for the device to regulate properly.
3	Gnd	This pin is connected with ground. It is also the tab of the package.
4	V_{OUT}	The output of the regulator. A minimum of output capacitance must be connected from this pin to ground to insure stability.
5	V_{ADJ}	A resistor divider from this pin to the V_{OUT} pin and to ground sets the output voltage. See application section for divider setting recommendations and a circuit example.

BLOCK DIAGRAM

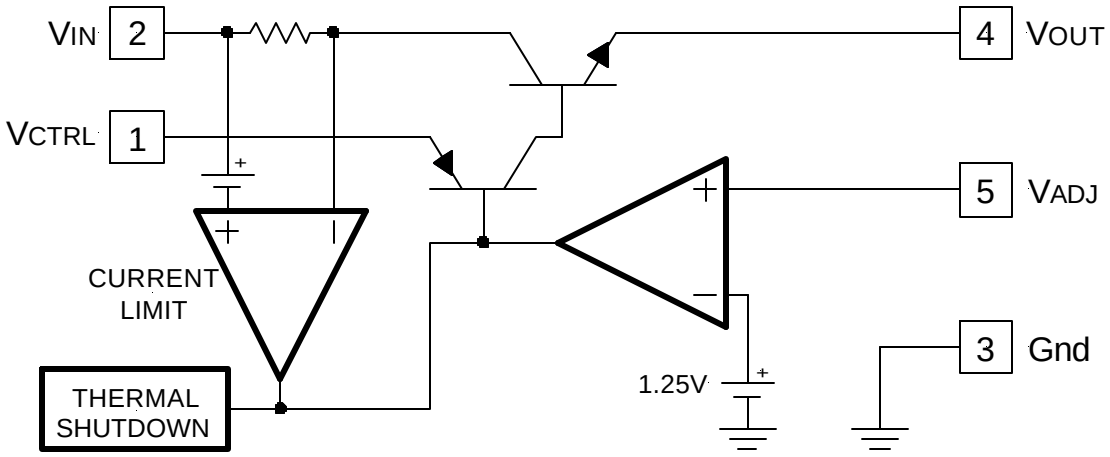


Figure 2 - Simplified block diagram of the IRU1120.

APPLICATION INFORMATION

Introduction

The IRU1120 adjustable regulator is a five-terminal device designed specifically to provide extremely low dropout voltages comparable to the PNP type without the disadvantage of the extra power dissipation due to the base current associated with PNP regulators. This is done by bringing out the control pin of the regulator that provides the base current to the power NPN and connecting it to a voltage that is grater than the voltage present at the V_{IN} pin. This flexibility makes the IRU1120 ideal for applications where dual inputs are available such as a computer mother board with an ATX style power supply that provides 5V and 3.3V to the board.

The IRU1120 is specifically designed to meet the fast current transient needs as well as providing an accurate initial voltage, reducing the overall system cost with the need for fewer number of output capacitors.

Output Voltage Setting

The IRU1120 can be programmed to any voltage in the range of 1.25V to 5.5V by using two external resistors. The output voltage is defined as:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) + I_{ADJ} \times R1$$

Where:

V_{REF} = 1.25V Typically

I_{ADJ} < 1µA Typically

R_1 and R_2 as shown in Figure 3:

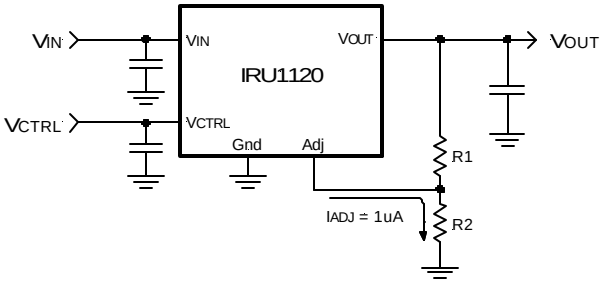


Figure 3 - Typical application of the IRU1120 for programming the output voltage.

The IRU1120 keeps a constant 1.25V between the adjust pin and the ground pin. By replacing a resistor (R2), between these two pins, a constant current flows through R1, subtracting the I_{ADJ} current out of the R1 to set the overall output voltage. Notice that since the I_{ADJ} is typically in the range of 1µA, it only adds a small error to the output voltage which is negligible.

Thermal Protection
When the junction temperature exceeds 150°C, the internal thermal protection shuts the IRU1120 down.

Current Limit Protection
The IRU1120 provides Over Current Protection when the output current exceeds typically 3A. The output decreases to limit the power dissipation.

Stability
The IRU1120 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. A minimum input capacitance of 4.7μF and a minimum output capacitance 4.7μF Ceramic capacitor is needed for regulator stage as well as the specified minimum loads to guarantee stability.

Transient Response and PSRR
The input and output capacitors are critical in order to ensure good transient response and PSRR. The most important aspects of this are capacitor selection, placement and trace routing. Place each capacitor as close as physically possible to its corresponding regulator pin. Use wide traces for a low inductance path. Couple directly to the ground and power planes as possible. The use of low ESR capacitors is crucial to achieving good results. Larger capacitance and lower ESR will improve both PSRR and transient response.

Thermal Design
The IRU1120 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the allowable maximum junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. The example below shows the steps in selecting the proper surface mount package.

Assuming, the following conditions:

V_{OUT} = 2.7V
V_{IN} = 3.3V
V_{CTRL} = 5V
I_{OUT} = 1A (DC Avg)

Calculate the maximum power dissipation using the following equation:

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + \left(\frac{I_{OUT}}{60}\right) \times (V_{CTRL} - V_{OUT})$$

$$P_D = 1 \times (3.3 - 2.7) + \left(\frac{1}{60}\right) \times (5 - 2.7) = 0.63W$$

For Ultra Thin-Pak™ we have:

R_{THJA} = 25°C/W
T_A = 45°C

$$\Delta T = P_D \times R_{THJA} = 0.63 \times 25 = 15.75°C$$

$$T_J = T_A + \Delta T = 60.75°C$$

Layout Consideration
The IRU1120, like many other high-speed regulators, requires that the output capacitors be close to the device for stability. For power consideration, a ground plane pad of approximately one-inch square on the component side must be dedicated to the device where all Gnd pins are connected to dissipate the power. If a multilayer board is used, it is recommended that the inner layers of the board are also dedicated to the size of the pad for better thermal characteristics.

TYPICAL CHARACTERISTICS

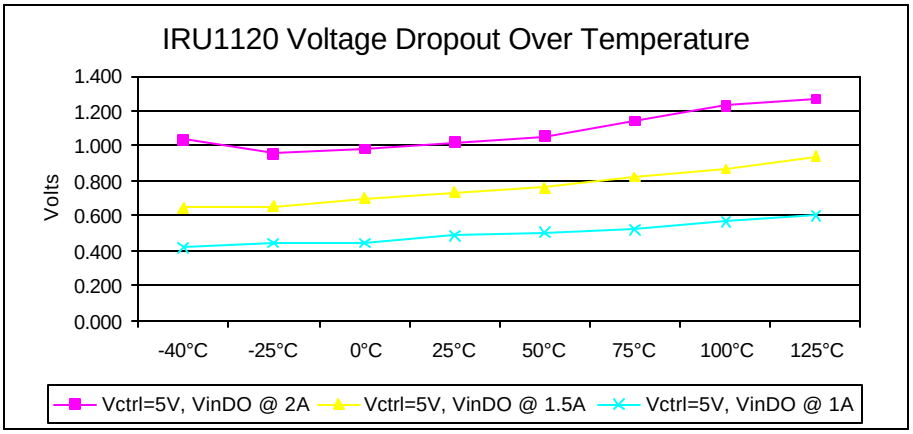


Figure 4 - Voltage dropout over temperature @ V_{CTRL}=5V.

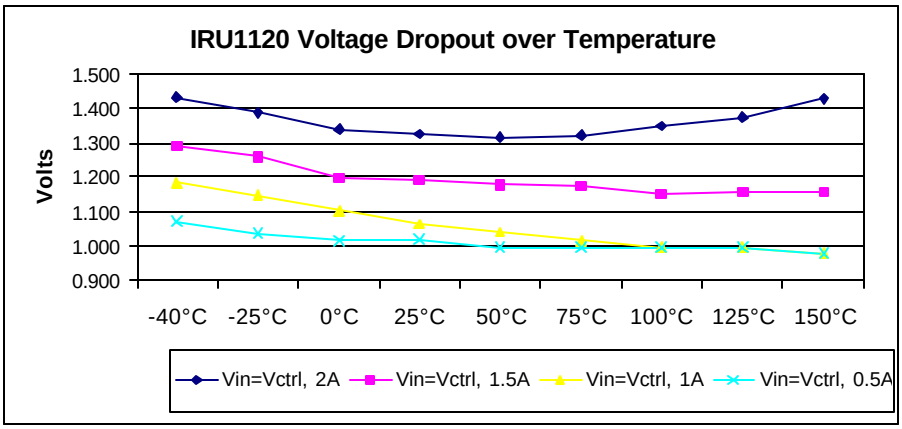


Figure 5 - Voltage dropout over temperature @ V_{IN}=V_{CTRL}.

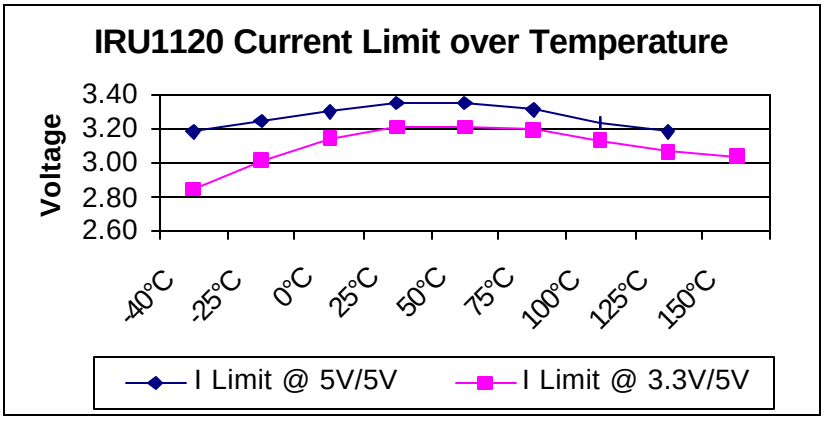


Figure 6 - Current limit over temperature @ V_{CTRL}=V_{IN}=5V and V_{CTRL}=5V and V_{IN}=3.3V

TEST DATA FOR IRU1120

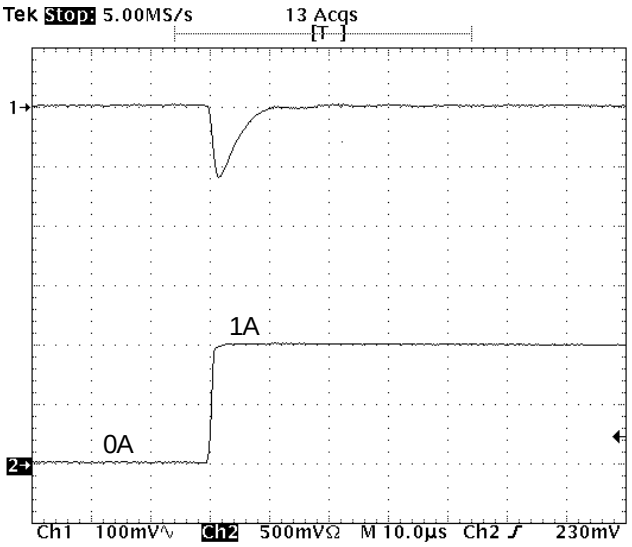


Figure 7- Load transient response @ I_{OUT} 0 to 1A,
V_{IN}=V_{CTRL}=5V, V_{OUT}=2.5V,
C_{IN}=C_{CTRL}=C_{OUT}=4.7µF, Ceramic.
Ch1: V_{OUT} (100mV/Div).
Ch2: I_{OUT} (0.5A/Div).

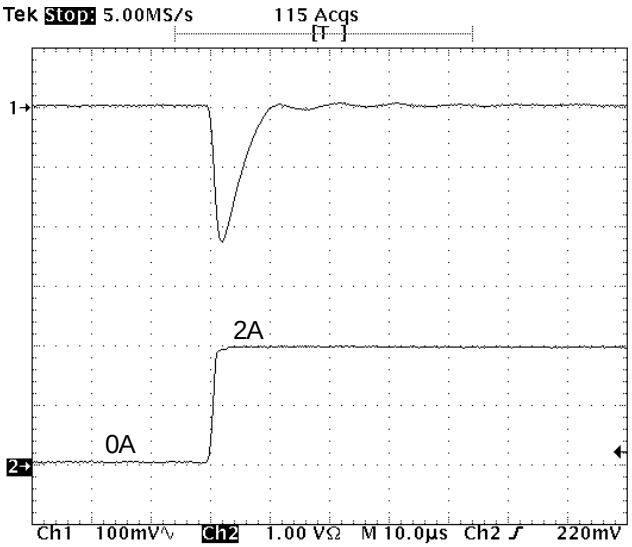


Figure 8- Load Transient response @ I_{OUT} 0 to 2A,
V_{IN}=VCTRL=5V, V_{OUT}=2.5V,
C_{IN}=C_{CTRL}=C_{OUT}=4.7µF, Ceramic.
Ch1: V_{OUT} (100mV/Div).
Ch2: I_{OUT} (1A/Div).

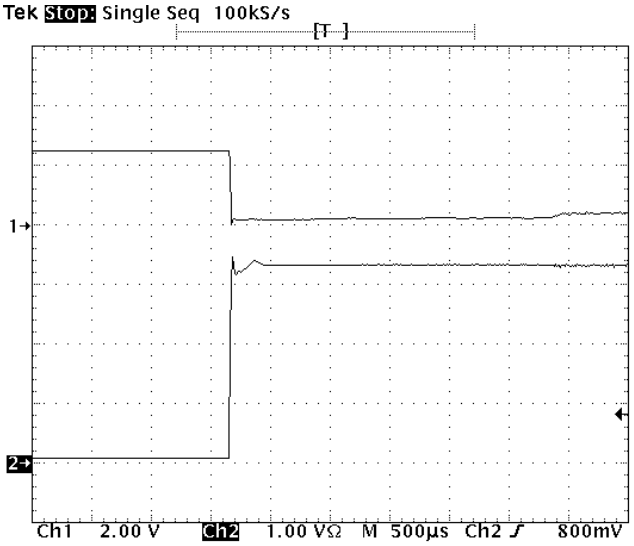


Figure 9- Current Limit Characteristic, V_{IN}=V_{CTRL}=5V,
V_{OUT}=2.5V, C_{IN}=C_{CTRL}=C_{OUT}=4.7uF, Ceramic.
Ch1: V_{OUT} (2V/Div).
Ch2: Shorted Current (I_{OUT}) (1A/Div).

International
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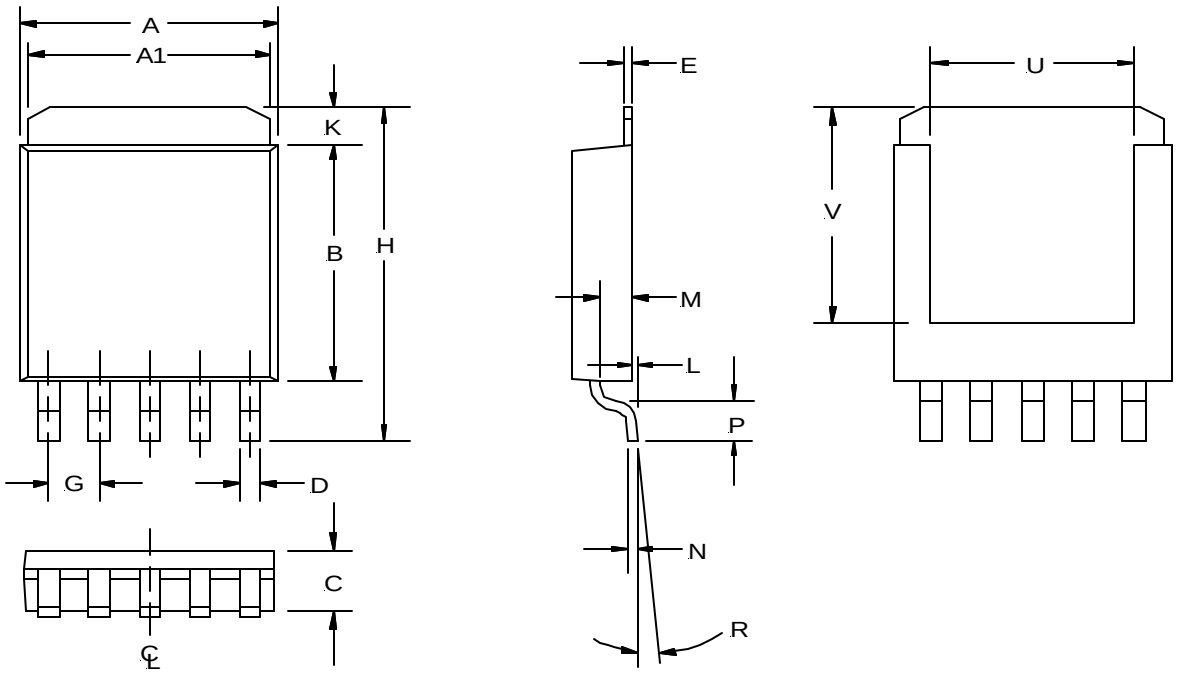
Data and specifications subject to change without notice. 02/01

(P) Ultra Thin-Pak™
5-Pin

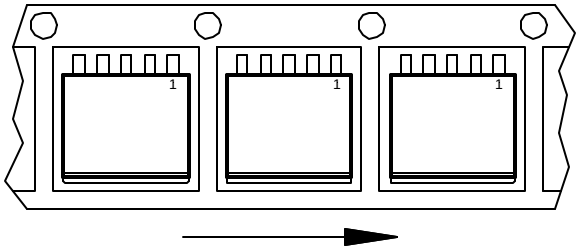


SYMBOL	MIN	MAX
A	9.27	9.52
A1	8.89	9.14
B	7.87	8.13
C	1.78	2.03
D	0.63	0.79
E	0.25 NOM	
G	1.72	
H	10.41	10.67
K	0.76	1.27
L	0.03	0.13
M	0.89	1.14
N	0.25	
P	0.79	1.04
R	3°	6°
U	5.59 NOM	
V	7.49 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
P	Ultra Thin-Pak™	5	75	2500	Fig A



Feed Direction
Figure A

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IRU1150

4A ULTRA LOW DROPOUT POSITIVE ADJUSTABLE REGULATOR

FEATURES

- 0.7V Dropout at 4A
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown

APPLICATIONS

- 3.3V to 2.7V Intel I740 Chip Set

DESCRIPTION

The IRU1150 is a 4A regulator with extremely low dropout voltage using a proprietary bipolar process that achieves comparable equivalent on-resistance to that of discrete MOSFETs. This product is specifically designed to provide well regulated supply for applications requiring 2.8V or lower voltages from 3.3V ATX power supplies where high efficiency of a switcher can be achieved without the cost and complexity associated with switching regulators. One such application is the new graphic chip sets that require anywhere from 2.4V to 2.7V supply such as the Intel I740 chip set.

TYPICAL APPLICATION

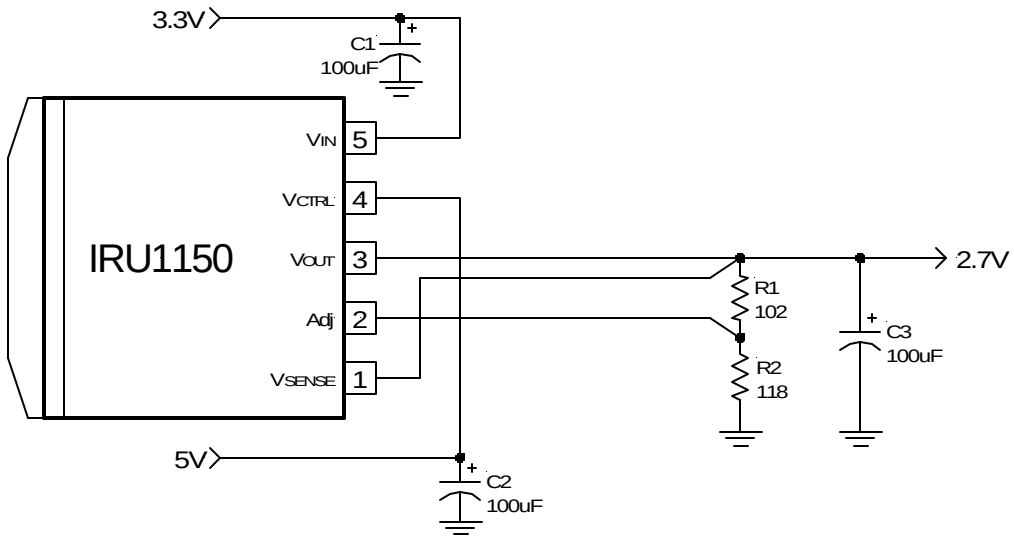


Figure 1 - Typical application of IRU1150 in a 3.3V to 2.7V for I740 chip.

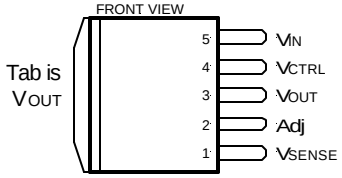
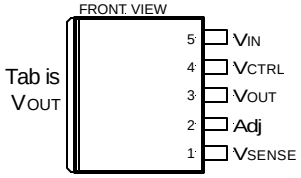
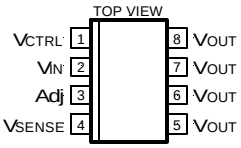
PACKAGE ORDER INFORMATION

T_J (°C)	5-PIN PLASTIC TO-263 (M)	5-PIN PLASTIC Ultra Thin-Pak™ (P)	8-PIN PLASTIC SOIC (S)
0 To 125	IRU1150CM	IRU1150CP	IRU1150CS

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Control Input Voltage (V_{CTRL}) 14V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

5-PIN PLASTIC TO-263 (M)	5-PIN PLASTIC ULTRA THIN-PAK™ (P)	8-PIN PLASTIC SOIC (S)
		
θ_{JA}=35°C/W for 0.5" square pad	θ_{JA}=35°C/W for 0.5" square pad	θ_{JA}=55°C/W for 1" Sq pad area

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=10µF, and T_J=0 to 125°C. Typical values refer to T_J=25°C. V_{OUT}=V_{SENSE}.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	V_{CTRL}=2.7 to 12V, V_{IN}=2.05V to 5.5, Io=10mA to 4A, V_{ADJ}=0V	1.225	1.250	1.275	V
Line Regulation		V_{CTRL}=2.5V to 7V, V_{IN}=1.75V to 5.5V, Io=10mA, V_{ADJ}=0V	-5	-0.2	+5	mV
Load Regulation (Note 1)		V_{CTRL}=2.75V, V_{IN}=2.1V, Io=10mA to 4A, V_{ADJ}=0V	-5	3	+5	mV
Dropout Voltage (Note 2) (V_{CTRL} - V_{OUT})		V_{ADJ}=0V for all conditions below:				
		V_{IN}=2.05V, Io=1.5A		1.00	1.15	V
		V_{IN}=2.05V, Io=3A		1.05	1.15	
		V_{IN}=2.05V, Io=4A		1.13	1.20	
Dropout Voltage (Note 2) (V_{IN} - V_{OUT})		V_{ADJ}=0V for all conditions below:				
		V_{CTRL}=2.75V, Io=1.5A		0.26	0.38	V
		V_{CTRL}=2.75V, Io=3A		0.50	0.60	
		V_{CTRL}=2.75V, Io=4A		0.70	1.15	
Current Limit		V_{CTRL}=2.75V, V_{IN}=2.05V, ΔVo=100mV, V_{ADJ}=0V	4.2	4.65	6	A
Minimum Load Current (Note 3)		V_{CTRL}=5V, V_{IN}=3.3V, V_{ADJ}=0V		1	10	mA
Thermal Regulation		30ms Pulse		0.01		%/W
Ripple Rejection		V_{CTRL}=5V, V_{IN}=5V, Io=4A, V_{ADJ}=0V, T_J=25°C, V_{RIPPLE}=1V_{PP} at 120Hz		70		dB
Control Pin Current		V_{ADJ}=0V for all below conditions:				
		V_{CTRL}=2.75V, V_{IN}=2.05V, Io=1.5A		16	25	mA
		V_{CTRL}=2.75V, V_{IN}=2.05V, Io=3A		36	50	
		V_{CTRL}=2.75V, V_{IN}=2.05V, Io=4A		67	85	
Adjust Pin Current	I_{ADJ}	V_{CTRL}=2.75V, V_{IN}=2.05V, V_{ADJ}=0V		50		µA

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor dividers are selected such that it automatically maintains this current.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	V_{SENSE}	This pin is the positive side of the reference which allows remote load sensing to achieve excellent load regulation.
2	Adj	A resistor divider from this pin to the V_{OUT} pin and ground sets the output voltage.
3	V_{OUT}	The output of the regulator. A minimum of 10µF capacitor must be connected from this pin to ground to insure stability.
4	V_{CTRL}	This pin is the supply pin for the internal control circuitry as well as the base drive for the pass transistor. This pin must always be higher than the V_{OUT} pin in order for the device to regulate. (See specifications)
5	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be higher than V_{OUT} in order for the device to regulate. (See specifications)

BLOCK DIAGRAM

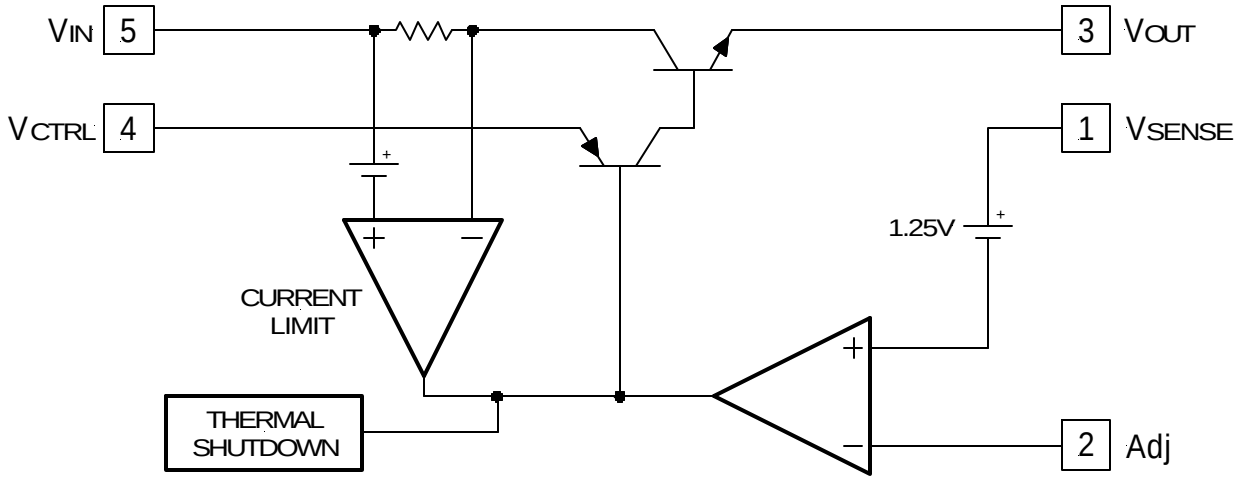


Figure 2 - Simplified block diagram of the IRU1150.

APPLICATION INFORMATION

Introduction

The IRU1150 adjustable regulator is a five-terminal device designed specifically to provide extremely low dropout voltages comparable to the PNP type without the disadvantage of the extra power dissipation due to the base current associated with PNP regulators. This is done by bringing out the control pin of the regulator that provides the base current to the power NPN and connecting it to a voltage that is grater than the voltage present at the V_{IN} pin. This flexibility makes the IRU1150 ideal for applications where dual inputs are available such as a computer mother board with an ATX style power supply that provides 5V and 3.3V to the board. One such application is the new graphic chip sets that require anywhere from 2.4V to 2.7V supply such as the Intel I740 chip set. The IRU1150 can easily be programmed with the addition of two external resistors to any voltages within the range of 1.25 to 5.5 V. Another major requirement of these graphic chips such as the Intel I740 is the need to switch the load current from zero to several amps in tens of nanoseconds at the processor pins, which translates to an approximately 300 to 500ns of current step at the regulator. In addition, the output voltage tolerances are also extremely tight and they include the transient response as part of the specification.

The IRU1150 is specifically designed to meet the fast current transient needs as well as providing an accurate initial voltage, reducing the overall system cost with the need for fewer number of output capacitors. Another feature of the device is its true remote sensing capability which allows accurate voltage setting at the load rather than at the device.

Output Voltage Setting

The IRU1150 can be programmed to any voltages in the range of 1.25V to 5.5V with the addition of R1 and R2 external resistors according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) + I_{ADJ} \times R2$$

Where:
V_{REF} = 1.25V Typically
I_{ADJ} = 50µA Typically
R_1 and R_2 as shown in Figure 3:

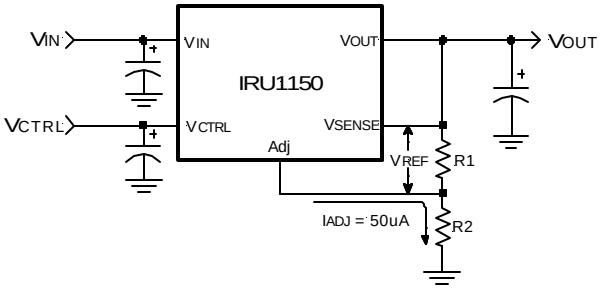


Figure 3 - Typical application of the IRU1150 for programming the output voltage.

The IRU1150 keeps a constant 1.25V between the V_{SENSE} pin and the V_{ADJ} pin. By placing a resistor R1 across these two pins and connecting the V_{SENSE} and V_{OUT} pin together, a constant current flows through R1, adding to the Iadj current and into the R2 resistor producing a voltage equal to the $(1.25/R1) \times R2 + I_{ADJ} \times R2$. This voltage is then added to the 1.25V to set the output voltage. This is summarized in the above equation. Since the minimum load current requirement of the IRU1150 is 10mA, R1 is typically selected to be a 121Ω resistor so that it automatically satisfies this condition. Notice that since the I_{ADJ} is typically in the range of 50µA it only adds a small error to the output voltage and should be considered when very precise output voltage setting is required.

Load Regulation

Since the IRU1150 has separate pins for the output (V_{OUT}) and the sense (V_{SENSE}), it is ideal for providing true remote sensing of the output voltage at the load. This means that the voltage drops due to parasitic resistance such as PCB traces between the regulator and the load are compensated for using remote sensing. Figure 4 shows a typical application of the IRU1150 with remote sensing.

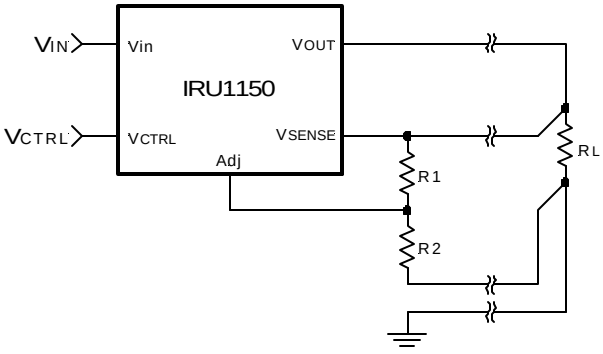


Figure 4 - Schematic showing connection for best load regulation.

Stability

The IRU1150 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for the microprocessor applications use standard electrolytic capacitors with typical ESR in the range of 50 to 100mΩ and an output capacitance of 500 to 1000μF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1150 takes advantage of this phenomena in making the overall regulator loop stable.

For most applications a minimum of 100μF aluminum electrolytic capacitor such as Sanyo, MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response.

Thermal Design

The IRU1150 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the allowable maximum junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. The example below shows the steps in selecting the proper surface mount package.

Assuming, the following conditions:

V_{OUT} = 2.7V
V_{IN} = 3.3V
V_{CTRL} = 5V
I_{OUT} = 2A (DC Avg)

Calculate the maximum power dissipation using the following equation:

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + \left(\frac{I_{OUT}}{60}\right) \times (V_{CTRL} - V_{OUT})$$

$$P_D = 2 \times (3.3 - 2.7) + \left(\frac{2}{60}\right) \times (5 - 2.7) = 1.28W$$

Using table below select the proper package and the amount of copper board needed.

Pkg	Copper Area	θ_{JA}(°C/W)	Max Pd (T_A=25°C)	Max Pd (T_A=45°C)
TO-263	1.4"X1.4"	25	4.4W	3.6W
TO-263	1.0"X1.0"	30	3.7W	3.0W
TO-263	0.7"X0.7"	35	3.1W	2.6W
TO-263	Pad Size	45	2.4W	2.0W
SO-8	1.0"X1.0"	55	2.0W	1.63W

Note: Above table is based on the maximum junction temperature of 135°C.

As shown in the above table, any of the two packages will do the job. For low cost applications the SOIC 8-pin package is recommended.

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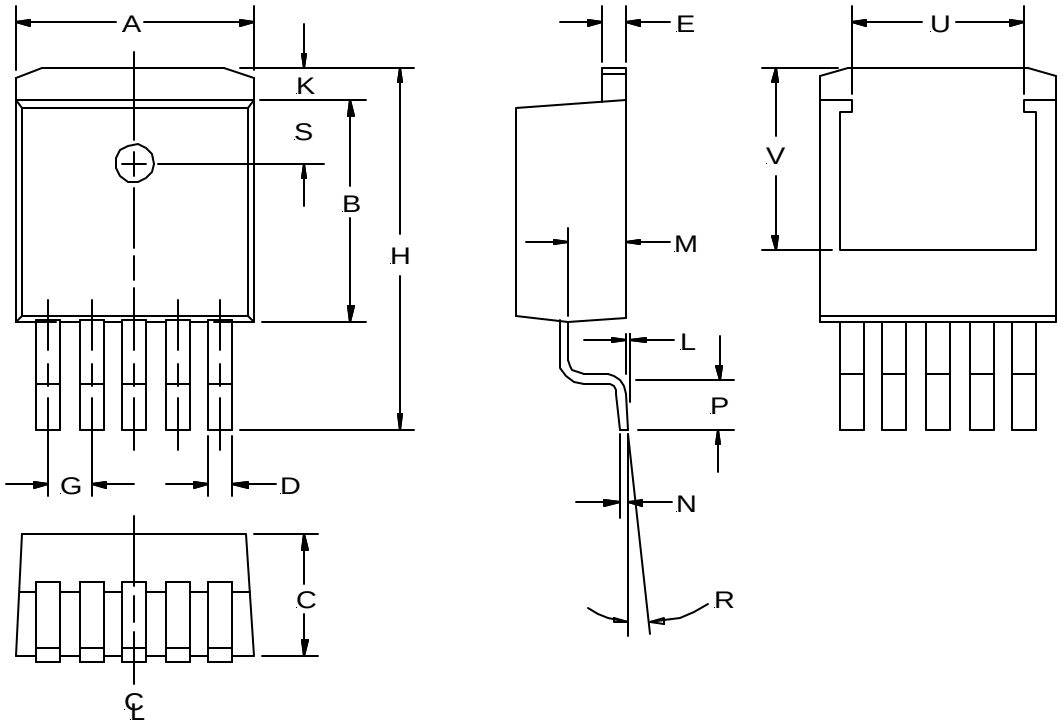
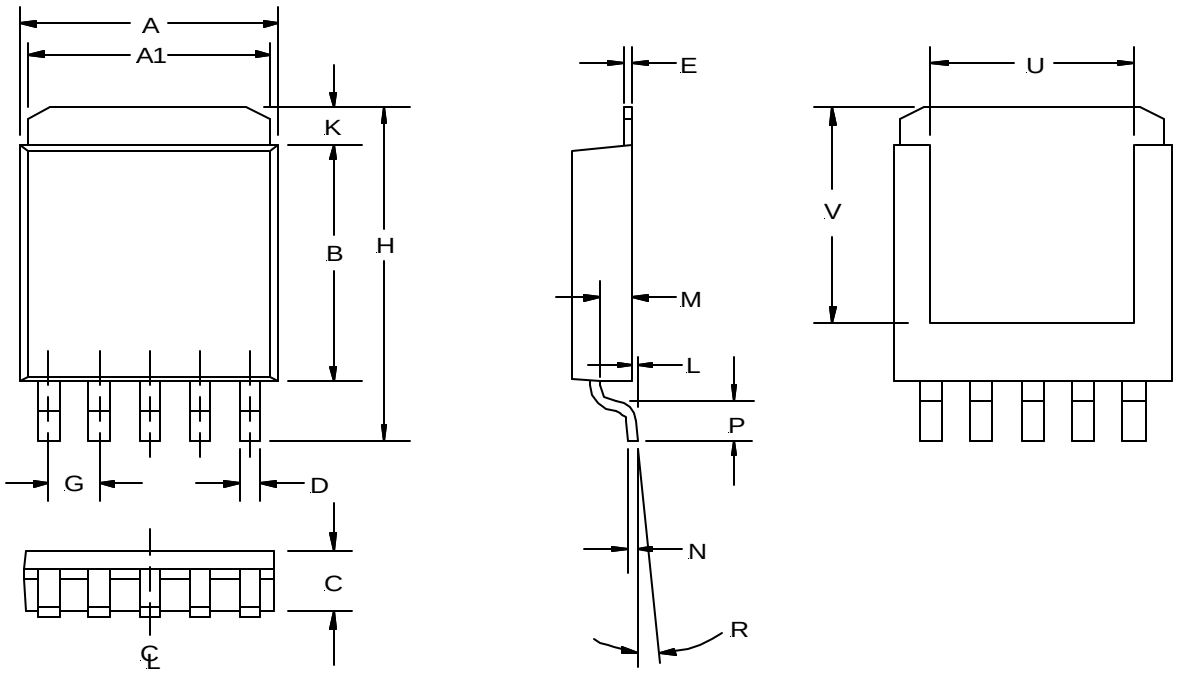
(M) TO-263 Package
5-Pin



SYMBOL	MIN	MAX
A	10.05	10.668
B	8.28	9.169
C	4.31	4.597
D	0.66	0.91
E	1.14	1.40
G	1.575	1.829
H	14.605	15.875
K	1.143	1.68
L	0.00	0.305
M	2.49	2.74
N	0.33	0.58
P	2.286	2.794
R	0°	8°
S	1.143	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

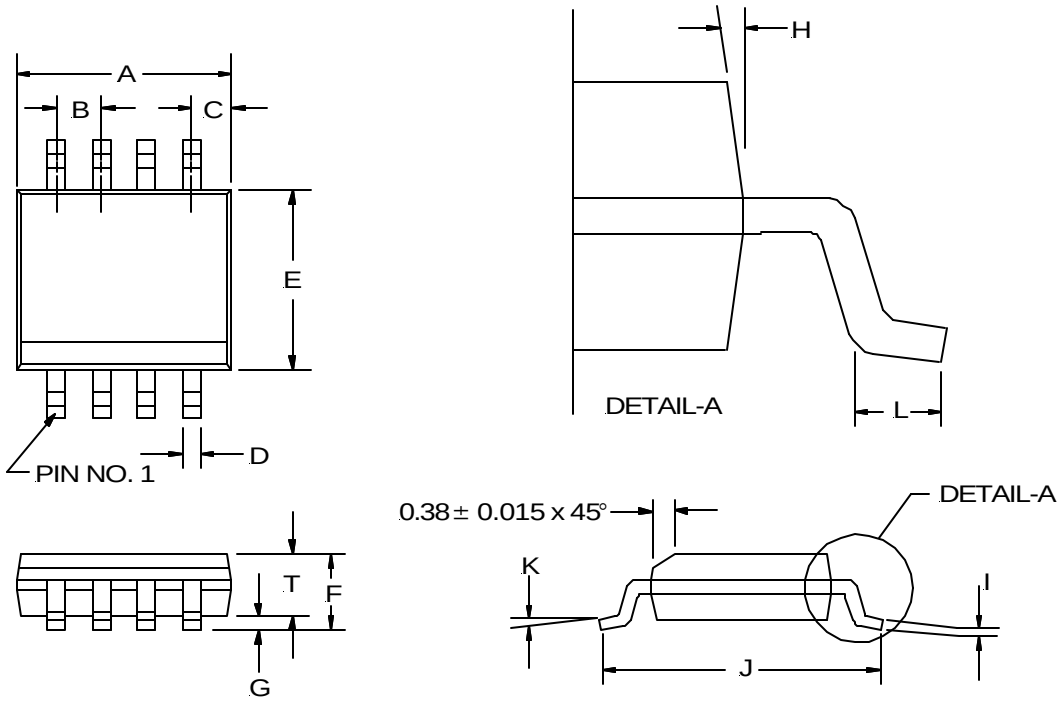
(P) Ultra Thin-Pak™
5-Pin



SYMBOL	MIN	MAX
A	9.27	9.52
A1	8.89	9.14
B	7.87	8.13
C	1.78	2.03
D	0.63	0.79
E	0.25 NOM	
G	1.72	
H	10.41	10.67
K	0.76	1.27
L	0.03	0.13
M	0.89	1.14
N	0.25	
P	0.79	1.04
R	3°	6°
U	5.59 NOM	
V	7.49 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(S) SOIC Package
8-Pin Surface Mount, Narrow Body

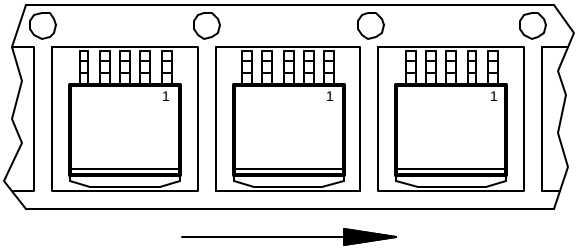


8-PIN		
SYMBOL	**MIN**	**MAX**
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

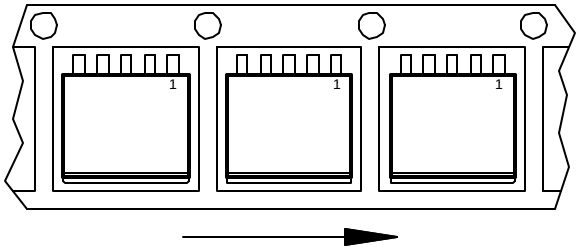
NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

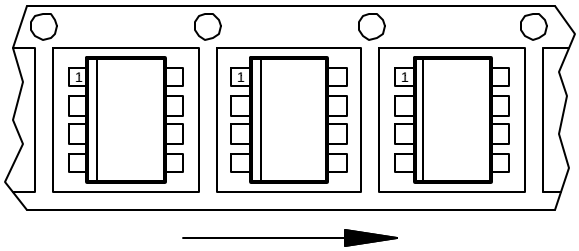
PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
M	TO-263	5	50	750	Fig A
P	Ultra Thin-Pak™	5	75	2500	Fig B
S	SOIC, Narrow Body	8	95	2500	Fig C



Feed Direction
Figure A



Feed Direction
Figure B



Feed Direction
Figure C

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IRU1160

6A ULTRA LOW DROPOUT POSITIVE ADJUSTABLE REGULATOR

FEATURES

- 0.62V Dropout at 6A
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown

APPLICATIONS

- VGA Card Applications
- On-Board Low Voltage Regulator Supply such as 3.3V to 2.8V

DESCRIPTION

The IRU1160 is a 6A regulator with extremely low dropout voltage using a proprietary bipolar process that achieves comparable equivalent on resistance to that of discrete MOSFETs. This product is specifically designed to provide well regulated supply for applications requiring 2.8V or lower voltages from 3.3V ATX power supplies where high efficiency of a switcher can be achieved without the cost and complexity associated with switching regulators.

TYPICAL APPLICATION

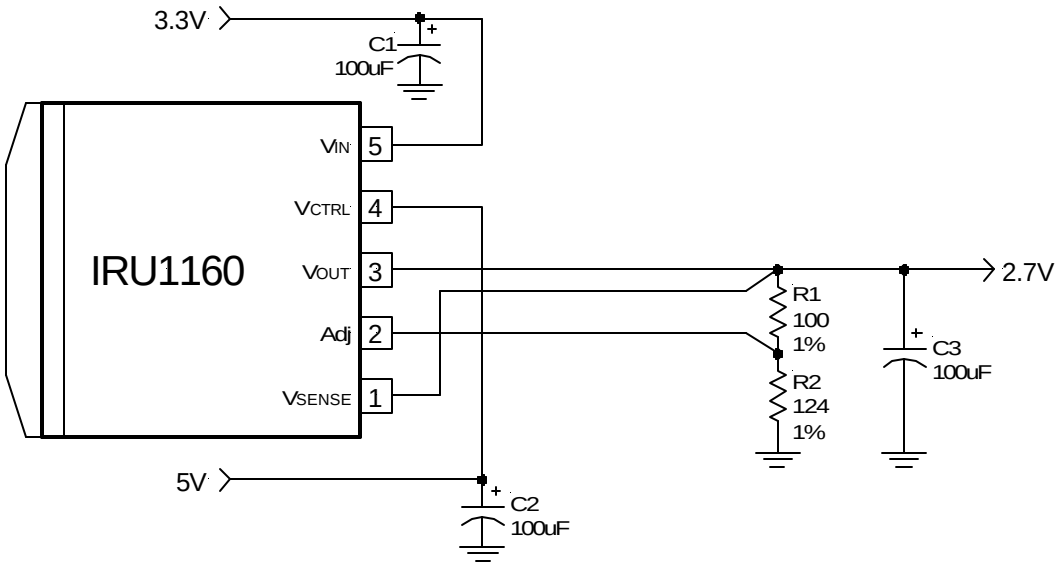


Figure 1 - Typical application of IRU1160 in a 3.3V to 2.8V.

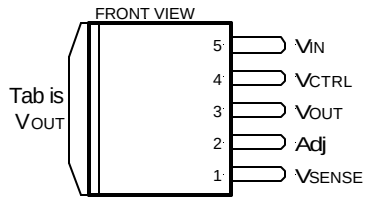
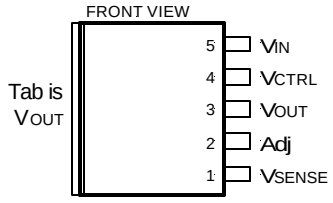
PACKAGE ORDER INFORMATION

T_J (°C)	5-PIN PLASTIC TO-263 (M)	5-PIN PLASTIC Ultra Thin-Pak™ (P)
0 To 125	IRU1160CM	IRU1160CP

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Control Input Voltage (V_{CTRL}) 14V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

5-PIN PLASTIC TO-263 (M)	5-PIN PLASTIC ULTRA THIN-PAK™ (P)
	
θ_{JA}=35°C/W for 0.5" square pad	θ_{JA}=35°C/W for 0.5" square pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=µF, C_{OUT}=10µF, and T_J=0 to 125°C. Typical values refer to T_J=25°C. V_{OUT}=V_{SENSE}.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	V_{CTRL}=2.75, V_{IN}=2V, Io=10mA,				
		T_J=25°C, V_{ADJ}=0V	1.225	1.250	1.275	V
		V_{CTRL}=2.7 to 12V, V_{IN}=2.05V to 5.5V,				
		Io=10mA to 6A, V_{ADJ}=0V	1.225	1.250	1.275	
Line Regulation		V_{CTRL}=2.5V to 7V, V_{IN}=1.75V to 5.5V,				
		Io=10mA, V_{ADJ}=0V			3	mV
Load Regulation (Note 1)		V_{CTRL}=2.75V, V_{IN}=2.1V,				
		Io=10mA to 6A, V_{ADJ}=0V			6	mV
Dropout Voltage (Note 2)		V_{ADJ}=0V for all conditions below:				
(V_{CTRL} - V_{OUT})		V_{IN}=2.05V, Io=1.5A		1.00		V
		V_{IN}=2.05V, Io=5A		1.10		
		V_{IN}=2.05V, Io=6A		1.20	1.30	
Dropout Voltage (Note 2)		V_{ADJ}=0V for all conditions below:				
(V_{IN} - V_{OUT})		V_{CTRL}=2.75V, Io=1.5A		0.15	0.20	V
		V_{CTRL}=2.75V, Io=5A		0.40	0.52	
		V_{CTRL}=2.75V, Io=6A		0.55	0.62	
Current Limit		V_{CTRL}=2.75V, V_{IN}=2.05V,				
		ΔVo=100mV, V_{ADJ}=0V	6.2			A
Minimum Load Current (Note 3)		V_{CTRL}=5V, V_{IN}=3.3V, V_{ADJ}=0V		5	10	mA
Thermal Regulation		30ms Pulse		0.01	0.02	%/W
Ripple Rejection		V_{CTRL}=5V, V_{IN}=5V, Io=5A, V_{ADJ}=0V,				
		T_J=25°C, V_{RIPPLE}=1V_{PP} at 120Hz	60	70		dB

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Control Pin Current		V_{ADJ}=0V for all below conditions:				
		V_{CTRL}=2.75V, V_{IN}=2.05V, Io=1.5A		15		mA
		V_{CTRL}=2.75V, V_{IN}=2.05V, Io=5A		50		
		V_{CTRL}=2.75V, V_{IN}=2.05V, Io=6A		60		
Adjust Pin Current	I_{ADJ}	V_{CTRL}=2.75V, V_{IN}=2.05V, V_{ADJ}=0V		50	120	µA

Note 1: Low duty cycle pulse testing with Kelvin connections are required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

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PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
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5	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum dropout voltage during the load transient response. This pin must always be higher than V_{OUT} in order for the device to regulate. (See specifications)

BLOCK DIAGRAM

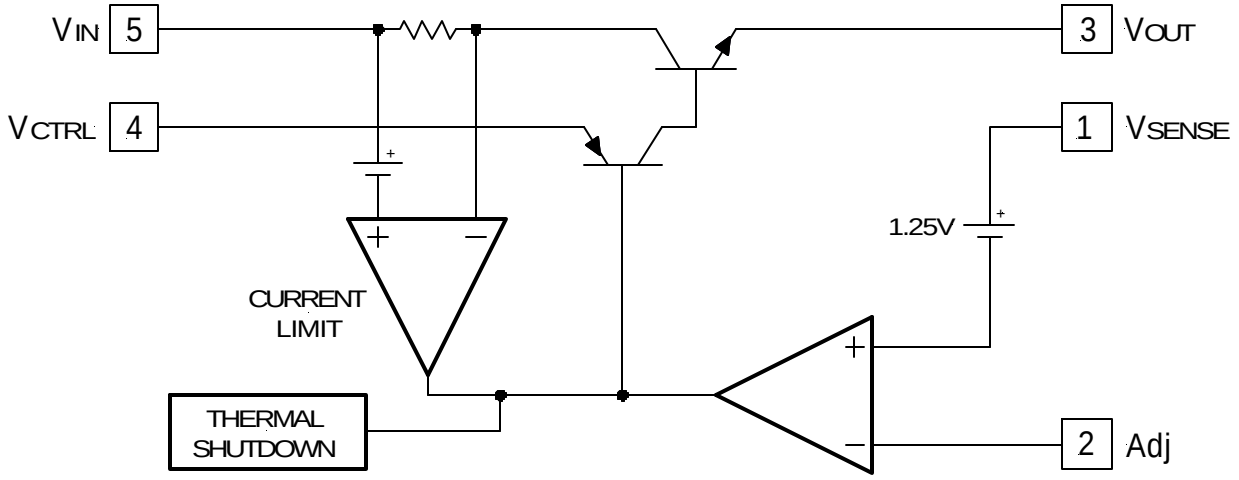

Figure 2 - Simplified block diagram of the IRU1160.

APPLICATION INFORMATION

Introduction

The IRU1160 adjustable regulator is a five-terminal device designed specifically to provide extremely low dropout voltages comparable to the PNP type without the disadvantage of the extra power dissipation due to the base current associated with PNP regulators. This is done by bringing out the control pin of the regulator that provides the base current to the power NPN and connecting it to a voltage that is grater than the voltage present at the V_{IN} pin. This flexibility makes the IRU1160 ideal for applications where dual inputs are available such as a computer mother board with an ATX style power supply that provides 5V and 3.3V to the board. One such application is the new graphic chip sets that require anywhere from 2.4V to 2.7V supply such as the Intel I740 chip set. The IRU1160 can easily be programmed with the addition of two external resistors to any voltages within the range of 1.25 to 5.5 V. Another major requirement of these graphic chips such as the Intel I740 is the need to switch the load current from zero to several amps in tens of nanoseconds at the processor pins, which translates to an approximately 300 to 500ns of current step at the regulator. In addition, the output voltage tolerances are also extremely tight and they include the transient response as part of the specification.

The IRU1160 is specifically designed to meet the fast current transient needs as well as providing an accurate initial voltage, reducing the overall system cost with the need for fewer number of output capacitors. Another feature of the device is its true remote sensing capability which allows accurate voltage setting at the load rather than at the device.

Output Voltage Setting

The IRU1160 can be programmed to any voltages in the range of 1.25V to 5.5V with the addition of R1 and R2 external resistors according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) + I_{ADJ} \times R2$$

Where:
V_{REF} = 1.25V Typically
I_{ADJ} = 50µA Typically
R_1 & R_2 as shown in Figure 3:

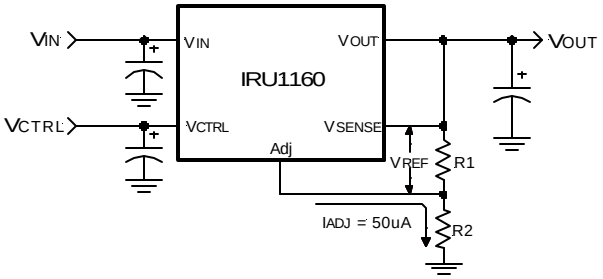

Figure 3 - Typical application of the IRU1160 for programming the output voltage.

The IRU1160 keeps a constant 1.25V between the V_{SENSE} pin and the V_{ADJ} pin. By placing a resistor R1 across these two pins and connecting the V_{SENSE} and V_{OUT} pin together, a constant current flows through R1, adding to the I_{ADJ} current and into the R2 resistor producing a voltage equal to the $(1.25/R1) \times R2 + I_{ADJ} \times R2$. This voltage is then added to the 1.25V to set the output voltage. This is summarized in the above equation. Since the minimum load current requirement of the IRU1160 is 10mA, R1 is typically selected to be a 121Ω resistor so that it automatically satisfies this condition. Notice that since the I_{ADJ} is typically in the range of 50µA, it adds a small error to the output voltage and should be considered when very precise output voltage setting is required.

Load Regulation

Since the IRU1160 has separate pins for the output (V_{OUT}) and the sense (V_{SENSE}), it is ideal for providing true remote sensing of the output voltage at the load. This means that the voltage drops due to parasitic resistance such as PCB traces between the regulator and the load are compensated for using remote sensing. Figure 4 shows a typical application of the IRU1160 with remote sensing.

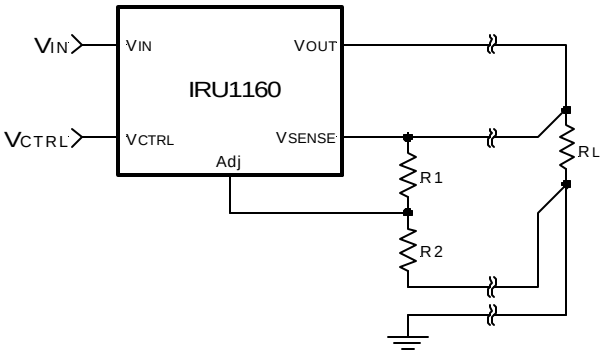

Figure 4 - Schematic showing connection for best load regulation.

Stability

The IRU1160 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for the microprocessor applications use standard electrolytic capacitors with typical ESR in the range of 50 to 100mΩ and an output capacitance of 500 to 1000μF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1160 takes advantage of this phenomena in making the overall regulator loop stable.

For most applications a minimum of 100μF aluminum electrolytic capacitor such as Sanyo, MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response.

Thermal Design

The IRU1160 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the allowable maximum junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. The example below shows the steps in selecting the proper surface mount package.

Assuming, the following conditions:

V_{OUT} = 2.8V
V_{IN} = 3.3V
V_{CTRL} = 5V
I_{OUT} = 3A (DC Avg)

Calculate the maximum power dissipation using the following equation:

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + \left(\frac{I_{OUT}}{60}\right) \times (V_{CTRL} - V_{OUT})$$

$$P_D = 1 \times (3.3 - 2.8) + \left(\frac{3}{60}\right) \times (5 - 2.8) = 1.61W$$

Using table below select the proper package and the amount of copper board needed.

Pkg	Copper Area	θ_{JA}(°C/W)	Max Pd (T_A=25°C)	Max Pd (T_A=45°C)
TO-263	1.4"X1.4"	25	4.4W	3.6W
TO-263	1.0"X1.0"	30	3.7W	3.0W
TO-263	0.7"X0.7"	35	3.1W	2.6W
TO-263	Pad Size	45	2.4W	2.0W

Note: Above table is based on the maximum junction temperature of 135°C.

International
IOR Rectifier

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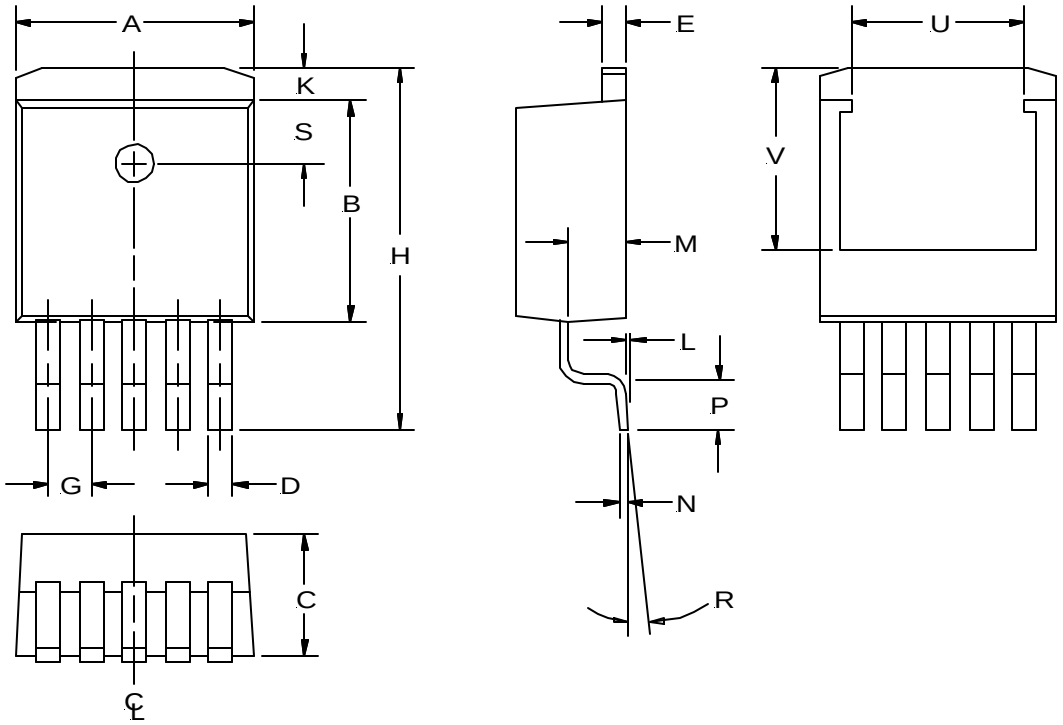
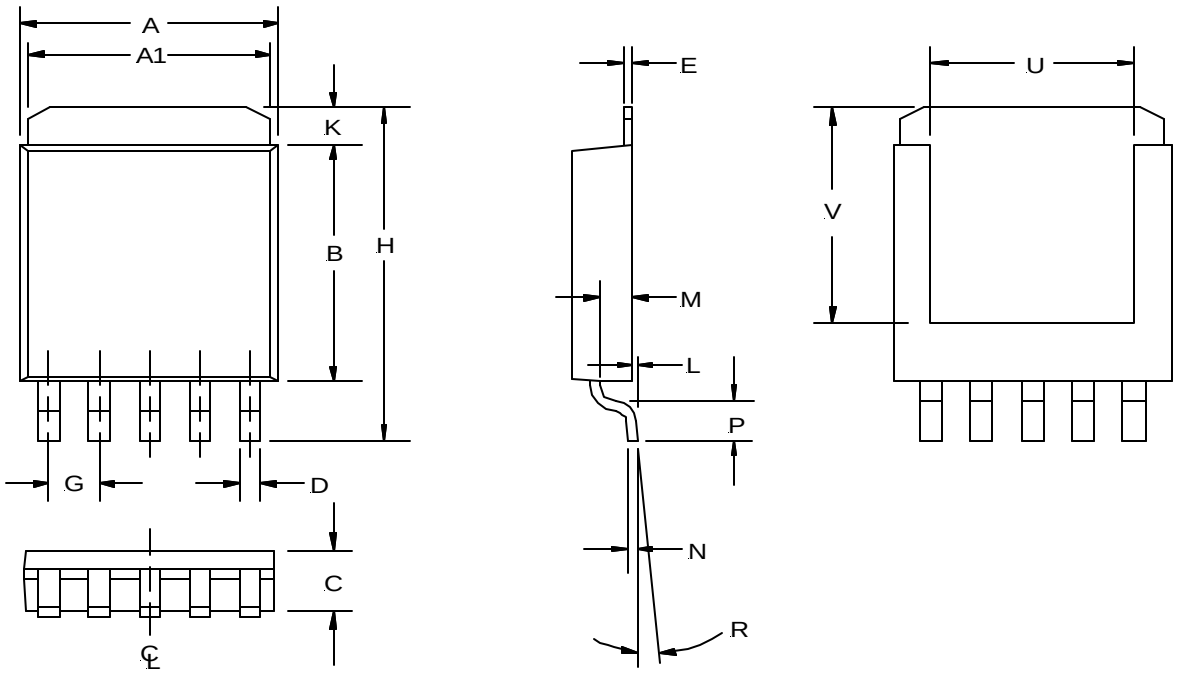
(M) TO-263 Package
5-Pin



SYMBOL	MIN	MAX
A	10.05	10.668
B	8.28	9.169
C	4.31	4.597
D	0.66	0.91
E	1.14	1.40
G	1.575	1.829
H	14.605	15.875
K	1.143	1.68
L	0.00	0.305
M	2.49	2.74
N	0.33	0.58
P	2.286	2.794
R	0°	8°
S	1.143	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(P) Ultra Thin-Pak™
5-Pin

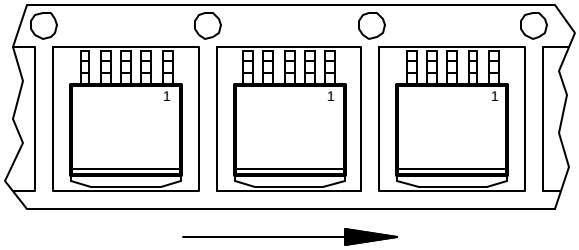


SYMBOL	MIN	MAX
A	9.27	9.52
A1	8.89	9.14
B	7.87	8.13
C	1.78	2.03
D	0.63	0.79
E	0.25 NOM	
G	1.72	
H	10.41	10.67
K	0.76	1.27
L	0.03	0.13
M	0.89	1.14
N	0.25	
P	0.79	1.04
R	3°	6°
U	5.59 NOM	
V	7.49 NOM	

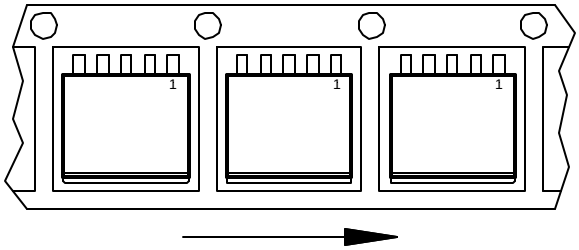
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
M	TO-263	5	50	750	Fig A
P	Ultra Thin-Pak™	5	75	2500	Fig B



Feed Direction
Figure A



Feed Direction
Figure B

International
IOR Rectifier

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IRU1175

7.5A ULTRA LOW DROPOUT POSITIVE ADJUSTABLE REGULATOR

FEATURES

- 0.5V Dropout at 7.5A (Equivalent of 67mΩ)
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown

APPLICATIONS

- 3.3V to 2.7V Intel I740 Chip Set

DESCRIPTION

The IRU1175 is a 7.5A regulator with extremely low dropout voltage using a proprietary bipolar process that achieves comparable equivalent on resistance to that of discrete MOSFETs. This product is specifically designed to provide well regulated supply for applications requiring very low dropout such as 2.8V from 3.3V ATX power supplies where the same efficiency as the switcher can be achieved without the cost and complexity associated with switching regulators. One such application is the new graphic chip sets that requires 2.7V supply such as the Intel I740 chip set.

TYPICAL APPLICATION

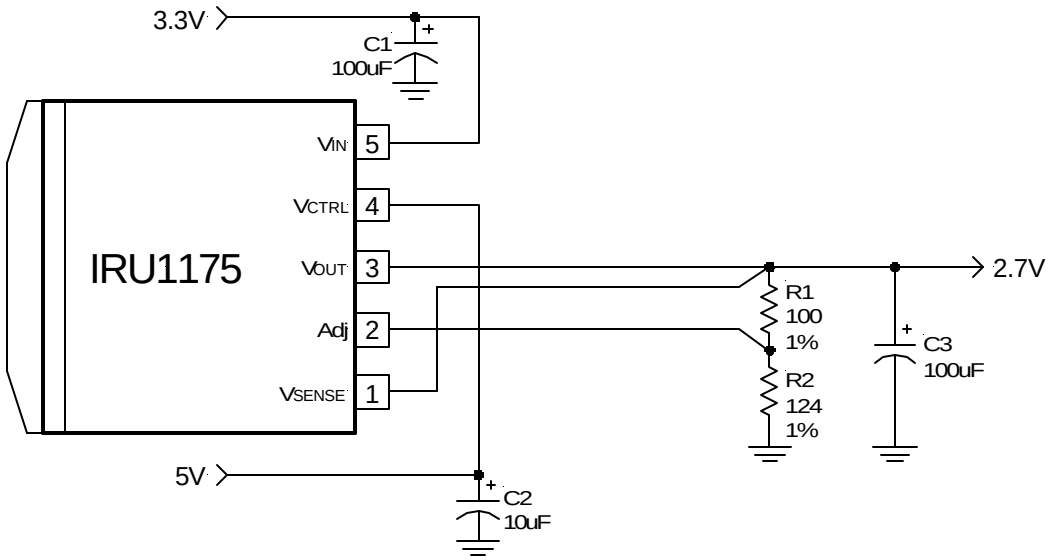


Figure 1 - Typical application of IRU1175.

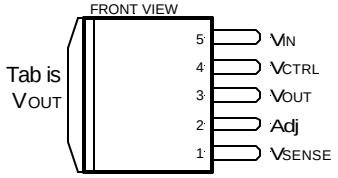
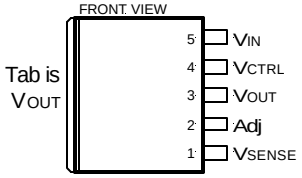
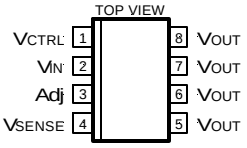
PACKAGE ORDER INFORMATION

T_J (°C)	5-PIN PLASTIC TO-263 (M)	5-PIN PLASTIC Ultra Thin-Pak™ (P)	8-PIN PLASTIC SOIC (S)
0 To 125	IRU1175CM	IRU1175CP	IRU1175CS

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 6V
Control Input Voltage (V_{CTRL}) 14V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

5-PIN PLASTIC TO-263 (M)	5-PIN PLASTIC ULTRA THIN-PAK™ (P)	8-PIN PLASTIC SOIC (S)
		
θ_{JA}=35°C/W for 0.5" square pad	θ_{JA}=35°C/W for 0.5" square pad	θ_{JA}=55°C/W for 1" Sq pad area

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=10µF, and T_J=0 to 125°C. Typical values refer to T_J=25°C. V_{OUT}=V_{SENSE}.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	V_{CTRL}=2.75, V_{IN}=2V, Io=10mA,				
		T_J=25°C, V_{ADJ}=0V	1.225	1.250	1.275	V
		V_{CTRL}=2.7 to 12V, V_{IN}=2.05V to 5.5,				
		Io=10mA to 7.5A, V_{ADJ}=0V	1.225	1.250	1.275	
Line Regulation		V_{CTRL}=2.5V to 7V, V_{IN}=1.75V to 5.5V,				
		Io=10mA, V_{ADJ}=0V		0.5	3	mV
Load Regulation (Note 1)		V_{CTRL}=2.75V, V_{IN}=2.1V,				
		Io=10mA to 7.5A, V_{ADJ}=0V		2	6	mV
Dropout Voltage (Note 2)		V_{ADJ}=0V for all conditions below:				
(V_{CTRL} - V_{OUT})		V_{IN}=2.05V, Io=1.5A		0.95		V
		V_{IN}=2.05V, Io=3A		1.00		
		V_{IN}=2.05V, Io=5A		1.05		
		V_{IN}=2.05V, Io=7.5A		1.15	1.30	
Dropout Voltage (Note 2)		V_{ADJ}=0V for all conditions below:				
(V_{IN} - V_{OUT})		V_{CTRL}=2.75V, Io=1.5A		0.100	0.130	V
		V_{CTRL}=2.75V, Io=3A		0.200	0.260	
		V_{CTRL}=2.75V, Io=3A		0.330	0.430	
		V_{CTRL}=2.75V, Io=7.5A		0.500	0.650	
Current Limit		V_{CTRL}=2.75V, V_{IN}=2.05V,				
		ΔVo=100mV, V_{ADJ}=0V	7.7	9		A
Minimum Load Current (Note 3)		V_{CTRL}=5V, V_{IN}=3.3V, V_{ADJ}=0V		5	10	mA
Thermal Regulation		30ms Pulse		0.01	0.02	%/W
Ripple Rejection		V_{CTRL}=5V, V_{IN}=5V, Io=3A, V_{ADJ}=0V,				
		T_J=25°C, V_{RIPPLE}=1V_{PP} at 120Hz	60	70		dB

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Control Pin Current		V_{ADJ}=0V for all below conditions:				
		V_{CTRL}=2.75V, V_{IN}=2.05V, Io=1.5A		15		mA
		V_{CTRL}=2.75V, V_{IN}=2.05V, Io=3A		30		
		V_{CTRL}=2.75V, V_{IN}=2.05V, Io=5A		50		
		V_{CTRL}=2.75V, V_{IN}=2.05V, Io=7.5A		70		
Adjust Pin Current	I_{ADJ}	V_{CTRL}=2.75V, V_{IN}=2.05V, V_{ADJ}=0V		50	120	µA

Note 1: Low duty cycle pulse testing with Kelvin connections are required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor dividers are selected such that it automatically maintains this current.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	V_{SENSE}	This pin is the positive side of the reference which allows remote load sensing to achieve excellent load regulation.
2	Adj	A resistor divider from this pin to the V_{OUT} pin and ground sets the output voltage.
3	V_{OUT}	The output of the regulator. A minimum of 10µF capacitor must be connected from this pin to ground to insure stability.
4	V_{CTRL}	This pin is the supply pin for the internal control circuitry as well as the base drive for the pass transistor. This pin must always be higher than the V_{OUT} pin in order for the device to regulate. (See specifications)
5	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be higher than V_{OUT} in order for the device to regulate. (See specifications)

BLOCK DIAGRAM

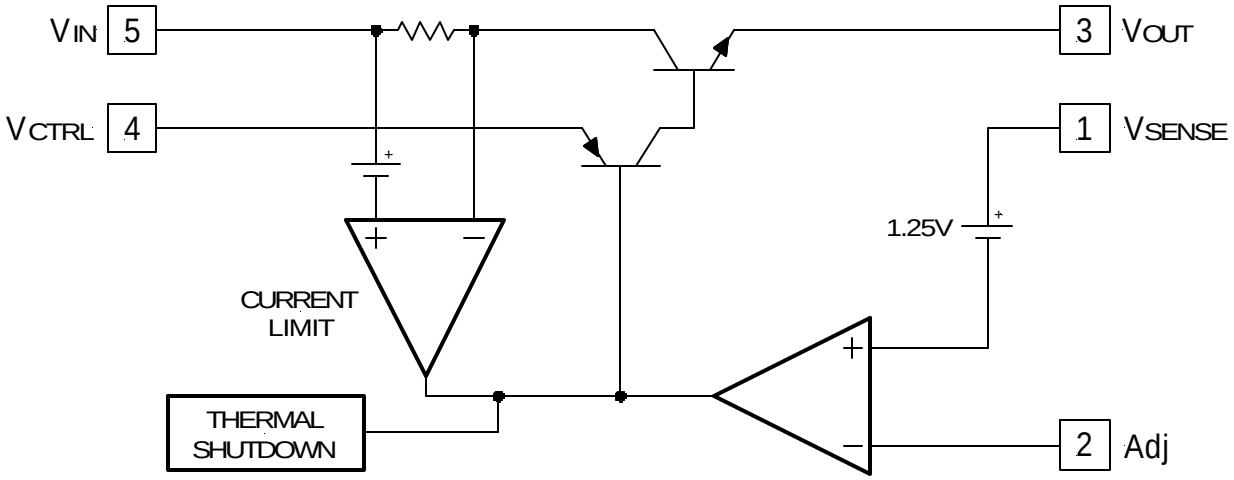


Figure 2 - Simplified block diagram of the IRU1175.

APPLICATION INFORMATION

Introduction

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Output Voltage Setting

The IRU1175 can be programmed to any voltages in the range of 1.25V to 5.5V with the addition of R1 and R2 external resistors according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) + I_{ADJ} \times R2$$

Where:

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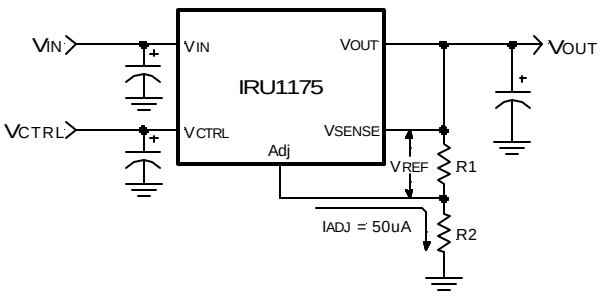
I_{ADJ} = 50µA Typically

R_1 & R_2 as shown in Figure 3:



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Load Regulation

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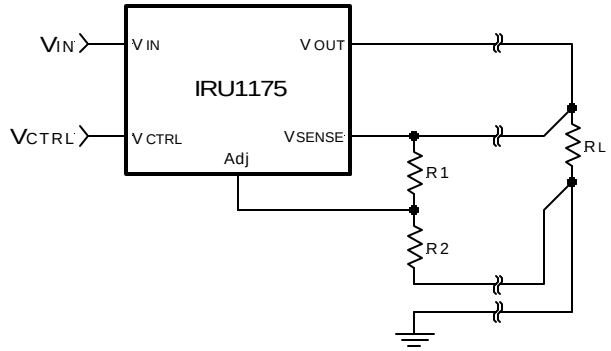

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Assuming, the following conditions:

V_{OUT} = 2.7V
V_{IN} = 3.3V
V_{CTRL} = 5V
I_{OUT} = 2A (DC Avg)

Calculate the maximum power dissipation using the following equation:

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + \left(\frac{I_{OUT}}{60}\right) \times (V_{CTRL} - V_{OUT})$$

$$P_D = 2 \times (3.3 - 2.7) + \left(\frac{2}{60}\right) \times (5 - 2.7) = 1.28W$$

Using table below select the proper package and the amount of copper board needed.

Pkg	Copper Area	θ_{JA}(°C/W)	Max Pd (T_A=25°C)	Max Pd (T_A=45°C)
TO-263	1.4"x1.4"	25	4.4W	3.6W
TO-263	1.0"x1.0"	30	3.7W	3.0W
TO-263	0.7"x0.7"	35	3.1W	2.6W
TO-263	Pad Size	45	2.4W	2.0W
SOIC	1.0"x1.0"	55	2.0W	1.63W

Note: Above table is based on the maximum junction temperature of 135°C.

As shown in the above table, any of the two packages will do the job. For low cost applications the SOIC 8-pin package is recommended.

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TAC Fax: (310) 252-7903
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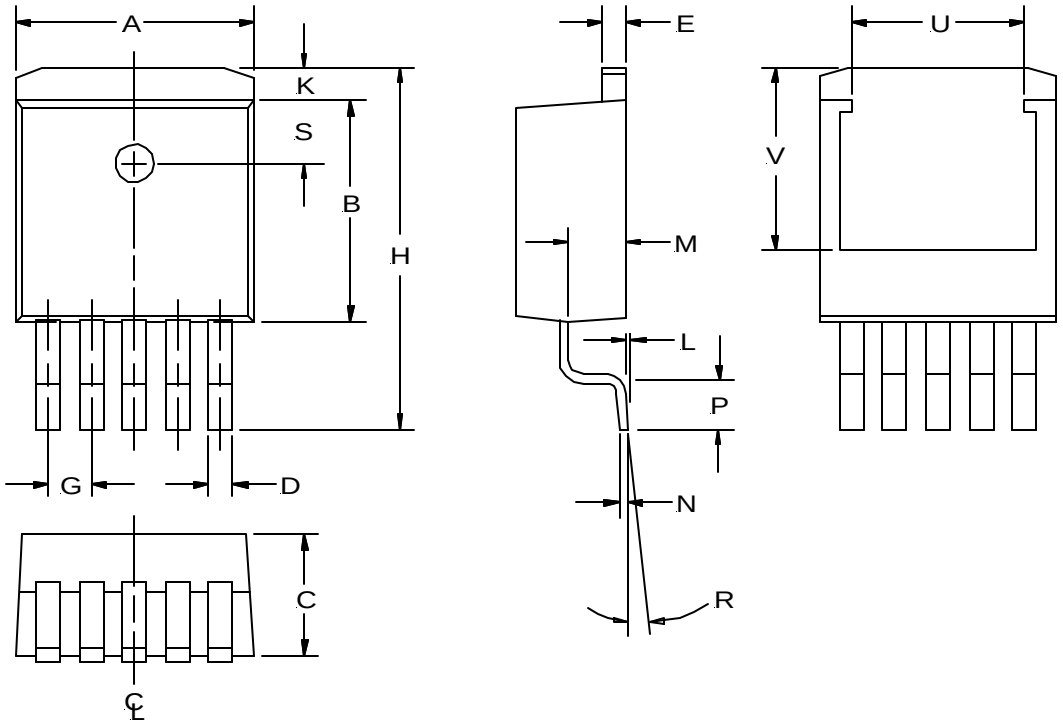
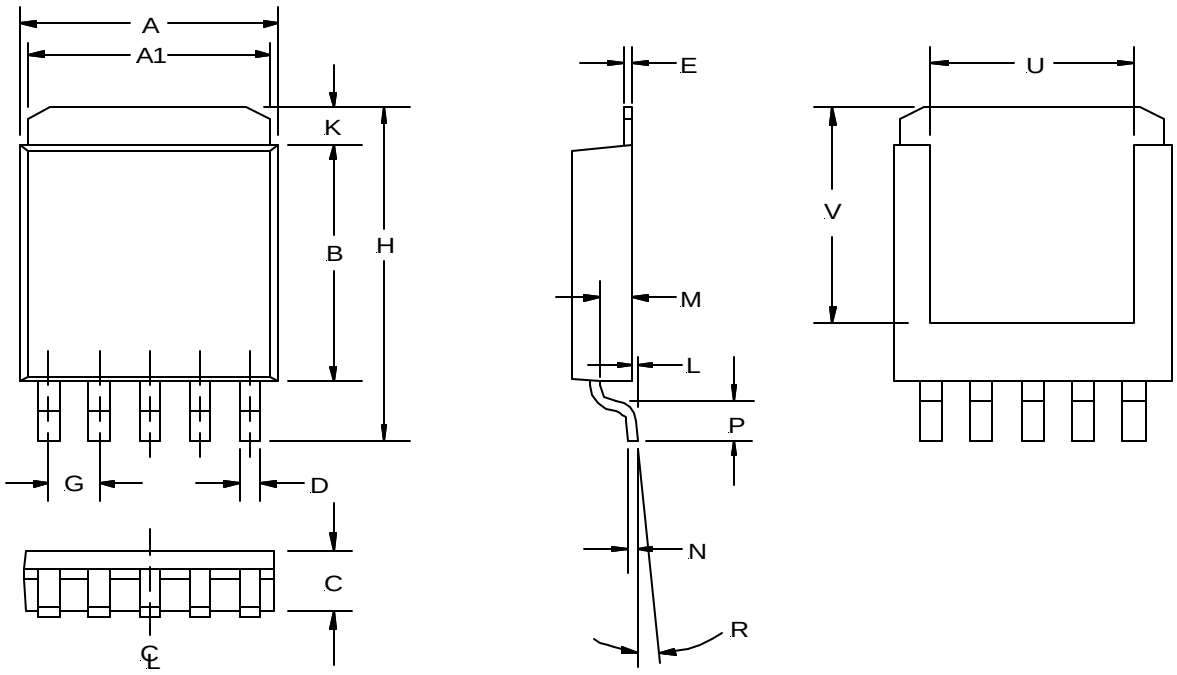
(M) TO-263 Package
5-Pin



SYMBOL	MIN	MAX
A	10.05	10.668
B	8.28	9.169
C	4.31	4.597
D	0.66	0.91
E	1.14	1.40
G	1.575	1.829
H	14.605	15.875
K	1.143	1.68
L	0.00	0.305
M	2.49	2.74
N	0.33	0.58
P	2.286	2.794
R	0°	8°
S	1.143	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

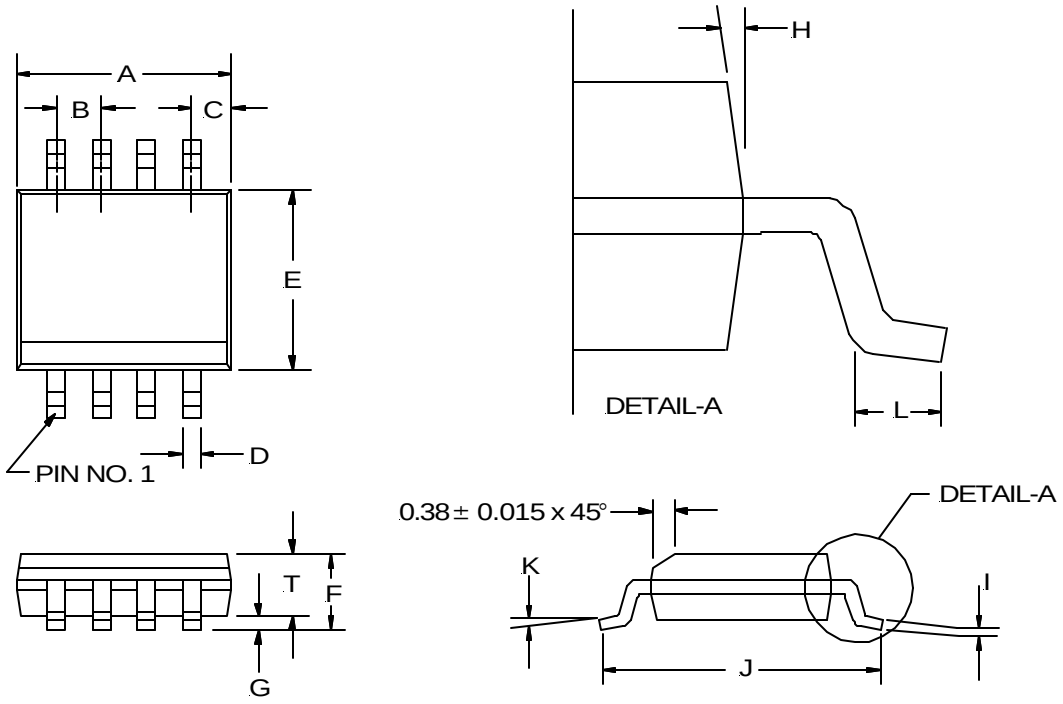
(P) Ultra Thin-Pak™
5-Pin



SYMBOL	MIN	MAX
A	9.27	9.52
A1	8.89	9.14
B	7.87	8.13
C	1.78	2.03
D	0.63	0.79
E	0.25 NOM	
G	1.72	
H	10.41	10.67
K	0.76	1.27
L	0.03	0.13
M	0.89	1.14
N	0.25	
P	0.79	1.04
R	3°	6°
U	5.59 NOM	
V	7.49 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(S) SOIC Package
8-Pin Surface Mount, Narrow Body

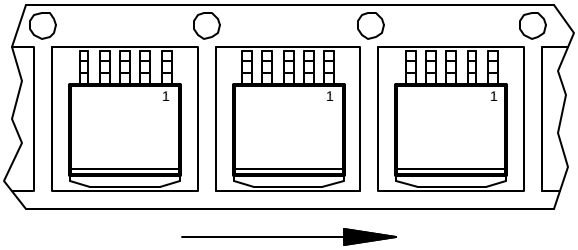


8-PIN		
SYMBOL	**MIN**	**MAX**
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

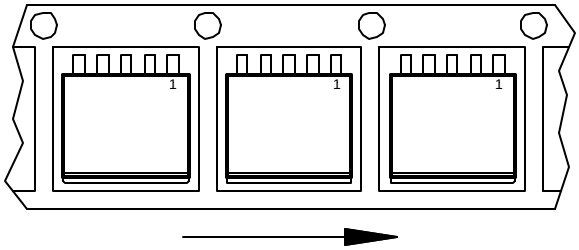
NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

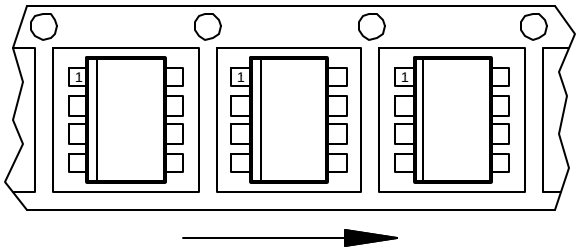
PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
M	TO-263	5	50	750	Fig A
P	Ultra Thin-Pak™	5	75	2500	Fig B
S	SOIC, Narrow Body	8	95	2500	Fig C



Feed Direction
Figure A



Feed Direction
Figure B



Feed Direction
Figure C

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information
Data and specifications subject to change without notice. 02/01

IRU1176

7.5A ULTRA LOW DROPOUT POSITIVE ADJUSTABLE REGULATOR WITH SHUTDOWN INPUT

FEATURES

- Guaranteed <0.65V Dropout at 7.5A
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown

APPLICATIONS

- 3.3V to 2.7V Intel I740 Chip Set

DESCRIPTION

The IRU1176 is a 7.5A regulator with extremely low dropout voltage using a proprietary Bipolar process that achieves comparable equivalent on resistance to that of discrete MOSFETs. The IRU1176 also provides a convenient shutdown pin that allows the regulator to be shutdown and reduce the input current consumption. Unlike the PNP type regulators this device does not have high quiescent current during the start up mode making it ideal for applications where there is limited current capability such operation from the 5V standby supply of the computer power supply. One application is the new generation of RDRAM memory that needs to provide 2.5V from 3.3V input and be able to operate from 5VSB as well.

TYPICAL APPLICATION

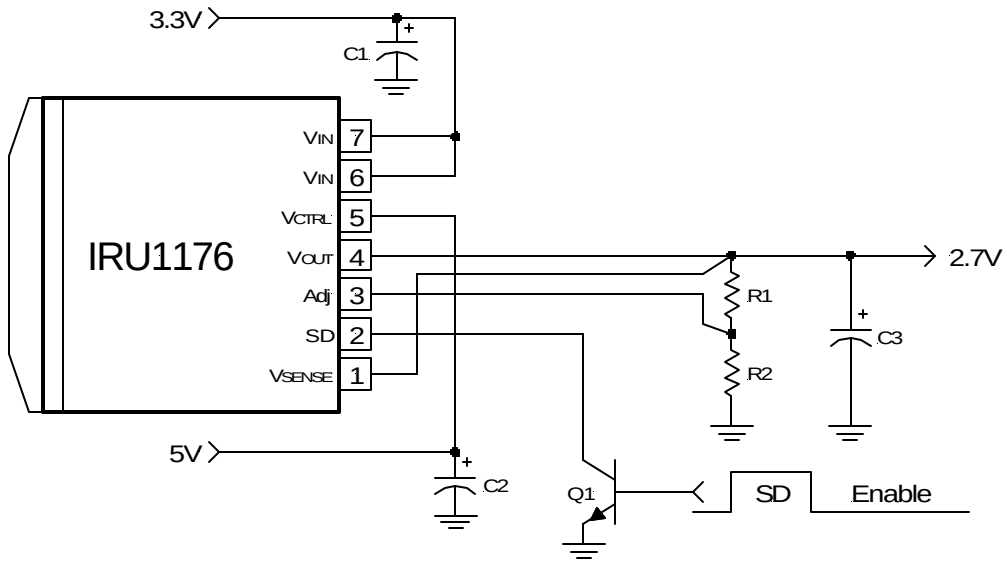


Figure 1 - Typical application of IRU1176.

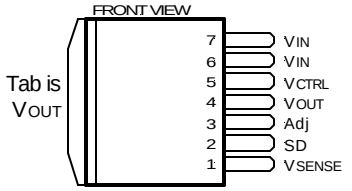
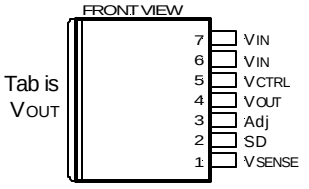
PACKAGE ORDER INFORMATION

T_J (°C)	7-PIN PLASTIC TO-263 (M)	7-PIN PLASTIC Ultra Thin-Pak™ (P)
0 To 125	IRU1176CM	IRU1176CP

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Control Input Voltage (V_{CTRL}) 14V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

7-PIN PLASTIC TO-263 (M)	7-PIN PLASTIC ULTRA THIN-PAK™ (P)
	
θ_{JA}=35°C/W for 0.5" square pad	θ_{JA}=35°C/W for 0.5" square pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=10µF and T_J=0 to 125°C. Typical values refer to T_J=25°C. V_{OUT}=V_{SENSE}.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	V_{CTRL}=2.75V, V_{IN}=2V, Io=10mA,				
		T_J=25°C, V_{ADJ}=0V	1.225	1.250	1.275	V
		V_{CTRL}=2.7 to 12V, V_{IN}=2.05V to 5.5V,				
		Io=10mA to 7.5A, V_{ADJ}=0V	1.225	1.250	1.275	
Line Regulation		V_{CTRL}=2.5V to 7V, V_{IN}=1.75V to 5.5V,				
		Io=10mA , V_{ADJ}=0V		0.5		mV
Load Regulation (Note 1)		V_{CTRL}=2.75V, V_{IN}=2.1V,				
		Io=10mA to 7.5A, V_{ADJ}=0V		5		mV
Dropout Voltage (Note 2)		V_{ADJ}=0V for all conditions below:				
(V_{CTRL} - V_{OUT})		V_{IN}=2.05V, Io=1.5A		0.95		V
		V_{IN}=2.05V, Io=3A		1.00		
		V_{IN}=2.05V, Io=4A		1.05		
		V_{IN}=2.05V, Io=7.5A		1.15		
Dropout Voltage (Note 2)		V_{ADJ}=0V for all conditions below:				
(V_{IN} - V_{OUT})		V_{CTRL}=2.75V, Io=1.5A		0.075		V
		V_{CTRL}=2.75V, Io=3A		0.150		
		V_{CTRL}=2.75V, Io=4A		0.200		
		V_{CTRL}=2.75V, Io=7.5A		0.375		
Current Limit		V_{CTRL}=2.75V, V_{IN}=2.05V,				
		ΔVo=100mV, V_{ADJ}=0V	7.7	9		A
Minimum Load Current (Note 3)		V_{CTRL}=5V, V_{IN}=3.3V, V_{ADJ}=0V		5	10	mA
Thermal Regulation		30ms Pulse		0.01	0.02	%/W
Ripple Rejection		V_{CTRL}=5V, V_{IN}=5V, Io=4A, V_{ADJ}=0V,				
		T_J=25°C, V_{RIPPLE}=1V_{PP} at 120Hz	60	70		dB
SD Threshold Voltage				V_{CTRL}-1.4	V_{CTRL}-2.2	V
SD Input Current		V_{CTRL}=5V, SD=0V		94	130	µA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Control Pin Current		V_{ADJ}=0V for all below conditions: V_{CTRL}=2.75V, V_{IN}=2.05V, Io=1.5A V_{CTRL}=2.75V, V_{IN}=2.05V, Io=3A V_{CTRL}=2.75V, V_{IN}=2.05V, Io=4A V_{CTRL}=2.75V, V_{IN}=2.05V, Io=7.5A				mA
Adjust Pin Current	I_{ADJ}	V_{CTRL}=2.75V, V_{IN}=2.05V, V_{ADJ}=0V		50	120	µA

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor dividers are selected such that it automatically maintains this current.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTIONS
1	V_{SENSE}	This pin is the positive side of the reference which allows remote load sensing to achieve excellent load regulation.
2	SD	When this pin is pulled lower than 1.4V with respect to the V_{CTRL} pin the device is shutdown. To enable the operation leave this pin open. Internal to device, there is a pull-up resistor.
3	Adj	A resistor divider from this pin to the V_{OUT} pin and ground sets the output voltage.
4	V_{OUT}	The output of the regulator. A minimum of 10µF capacitor must be connected from this pin to ground to insure stability.
5	V_{CTRL}	This pin is the supply pin for the internal control circuitry as well as the base drive for the pass transistor. This pin must always be higher than the V_{OUT} pin in order for the device to regulate. (See specifications)
6, 7	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be higher than V_{OUT} in order for the device to regulate. (See specifications)

BLOCK DIAGRAM

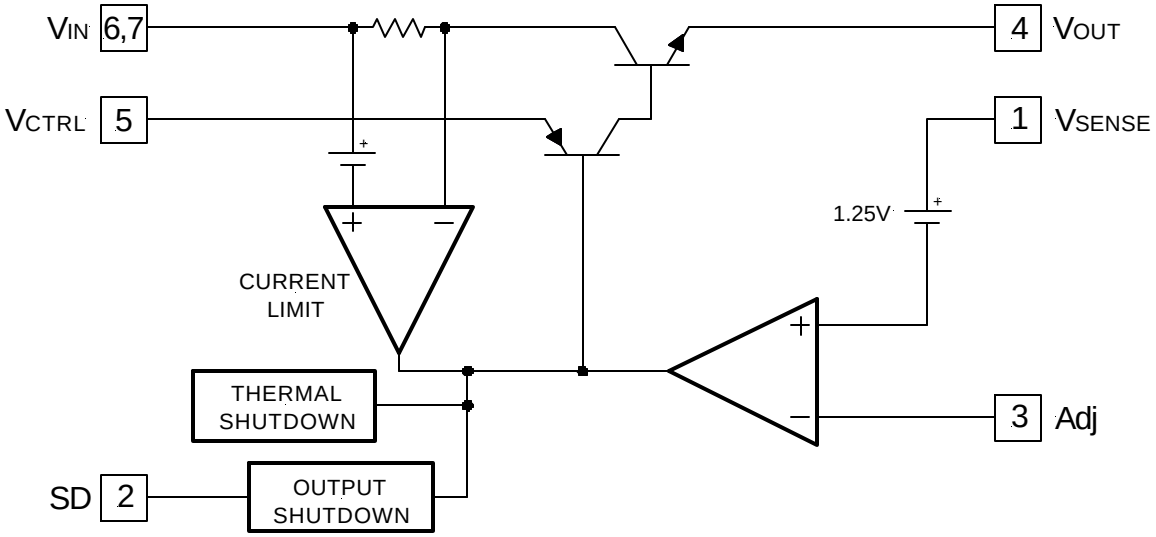


Figure 2 - Simplified block diagram of the IRU1176.

APPLICATION INFORMATION

Introduction

The IRU1176 adjustable regulator is a five-terminal device designed specifically to provide extremely low dropout voltages comparable to the PNP type without the disadvantage of the extra power dissipation due to the base current associated with PNP regulators. This is done by bringing out the control pin of the regulator that provides the base current to the power NPN and connecting it to a voltage that is grater than the voltage present at the V_{IN} pin. This flexibility makes the IRU1176 ideal for applications where dual inputs are available such as a computer mother board with an ATX style power supply that provides 5V and 3.3V to the board. One such application is the new graphic chip sets that require anywhere from 2.4V to 2.7V supply such as the Intel I740 chip set. The IRU1176 can easily be programmed with the addition of two external resistors to any voltages within the range of 1.25 to 5.5V. Another major requirement of these graphic chips is the need to switch the load current from zero to several amps in tens of nanoseconds at the processor pins, which translates to an approximately 300 to 500ns of current step at the regulator. In addition, the output voltage tolerances are also extremely tight and they include the transient response as part of the specification.

The IRU1176 is specifically designed to meet the fast current transient needs as well as providing an accurate initial voltage, reducing the overall system cost with the need for fewer number of output capacitors. Another feature of the device is its true remote sensing capability which allows accurate voltage setting at the load rather than at the device.

Output Voltage Setting

The IRU1176 can be programmed to any voltages in the range of 1.25V to 5.5V with the addition of R1 and R2 external resistors according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) + I_{ADJ} \times R2$$

Where:
V_{REF} = 1.25V Typically
I_{ADJ} = 50µA Typically
R_1 & R_2 as shown in Figure 3:

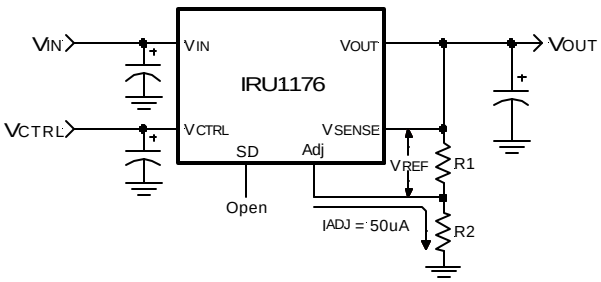


Figure 3 - Typical application of the IRU1176 for programming the output voltage.

The IRU1176 keeps a constant 1.25V between the V_{SENSE} pin and the V_{ADJ} pin. By placing a resistor R1 across these two pins and connecting the V_{SENSE} and V_{OUT} pin together, a constant current flows through R1, adding to the I_{ADJ} current and into the R2 resistor producing a voltage equal to the $(1.25/R1) \times R2 + I_{ADJ} \times R2$. This voltage is then added to the 1.25V to set the output voltage. This is summarized in the above equation. Since the minimum load current requirement of the IRU1176 is 10mA, R1 is typically selected to be a 121Ω resistor so that it automatically satisfies this condition. Notice that since the Iadj is typically in the range of 50μA it adds a small error to the output voltage and should be considered when very precise output voltage setting is required.

Load Regulation

Since the IRU1176 has separate pins for the output (V_{OUT}) and the sense (V_{SENSE}), it is ideal for providing true remote sensing of the output voltage at the load. This means that the voltage drops due to parasitic resistance such as PCB traces between the regulator and the load are compensated for using remote sensing. Figure 4 shows a typical application of the IRU1176 with remote sensing.

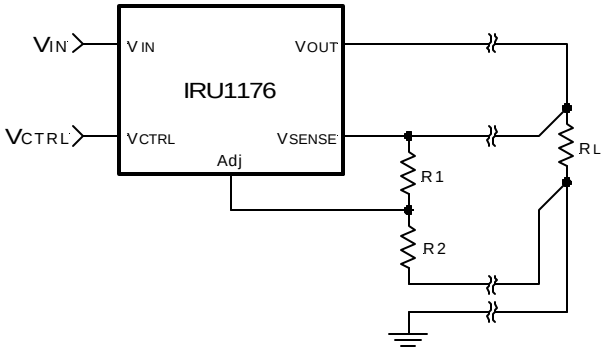


Figure 4 - Schematic showing connection for best load regulation.

Stability

The IRU1176 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for the microprocessor applications use standard electrolytic capacitors with typical ESR in the range of 50 to 100mΩ and an output capacitance of 500 to 1000μF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1176 takes advantage of this phenomena in making the overall regulator loop stable.

For most applications a minimum of 100μF aluminum electrolytic capacitor such as Sanyo, MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response.

Shutdown Operation

The IRU1176 can be disabled by pulling the SD pin low using an open collector device such as a low cost 2N3904 general purpose transistor as shown in the application circuit. The current sink of the pin is equal to:

$$I_{SINK} = \frac{(V_{CTRL} - 1.4)}{R} \qquad \text{Where: } R=50K\Omega \text{ Typically}$$

Thermal Design

The IRU1176 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the allowable maximum junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. The example below shows the steps in selecting the proper surface mount package.

Assuming, the following conditions:

V_{OUT} = 2.7V
V_{IN} = 3.3V
V_{CTRL} = 5V
I_{OUT} = 2A (DC Avg)

Calculate the maximum power dissipation using the following equation:

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + \left(\frac{I_{OUT}}{60}\right) \times (V_{CTRL} - V_{OUT})$$

$$P_D = 2 \times (3.3 - 2.7) + \left(\frac{2}{60}\right) \times (5 - 2.7) = 1.28W$$

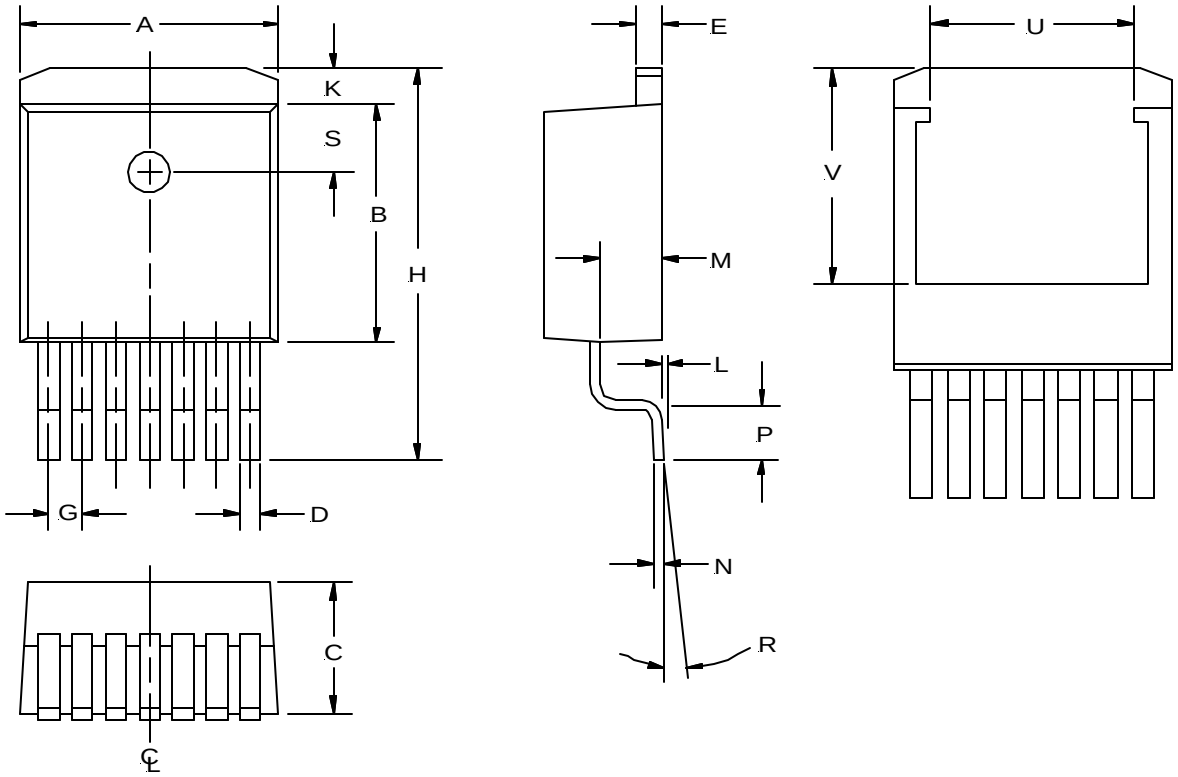
Using table below select the proper package and the amount of copper board needed.

Pkg	Copper Area	θ_{JA}(°C/W)	Max Pd (T_A=25°C)	Max Pd (T_A=45°C)
M or P	1.4"x1.4"	25	4.4W	3.6W
M or P	1.0"x1.0"	30	3.7W	3.0W
M or P	0.7"x0.7"	35	3.1W	2.6W
M or P	Pad Size	45	2.4W	2.0W

Note: Above table is based on the maximum junction temperature of 135°C.

As shown in the above table, any of the two packages will do the job. For lower cost applications the Ultra Thin-Pak is recommended.

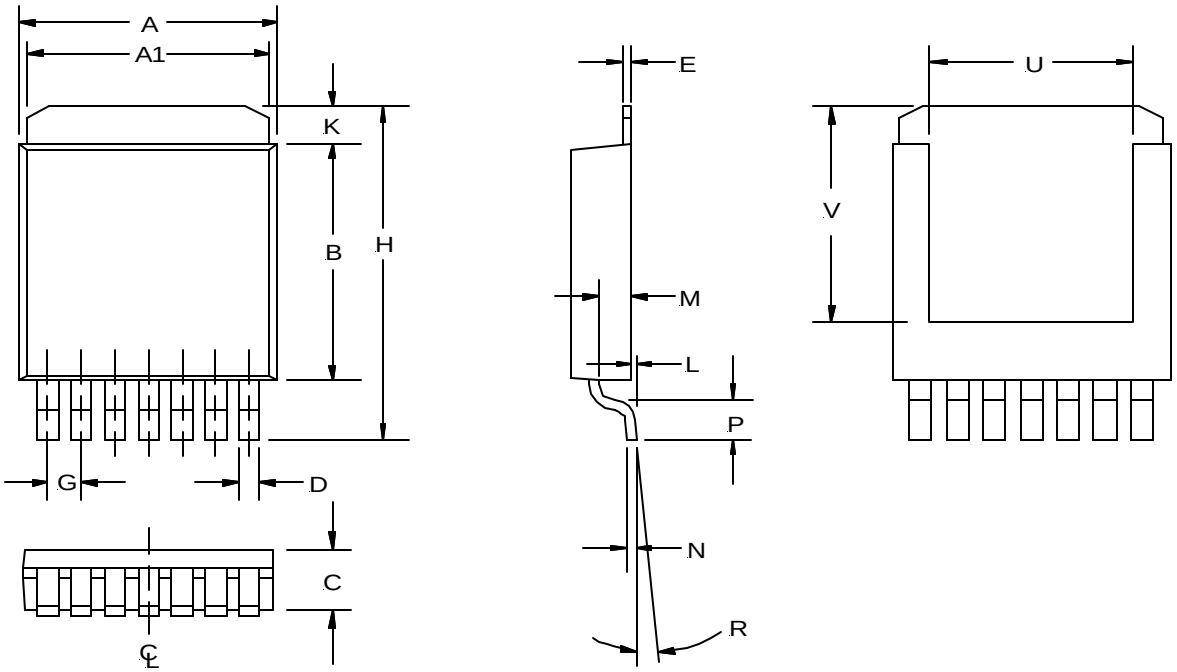
(M) TO-263 Package
7-Pin



SYMBOL	MIN	MAX
A	10.05	10.31
B	8.28	8.53
C	4.31	4.57
D	0.66	0.91
E	1.14	1.40
G	1.27 REF	
H	14.73	15.75
K	1.40	1.68
L	0.00	0.25
M	2.49	2.74
N	0.43	0.58
P	2.29	2.79
R	0°	8°
S	2.41	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(P) Ultra Thin-Pak™
7-Pin

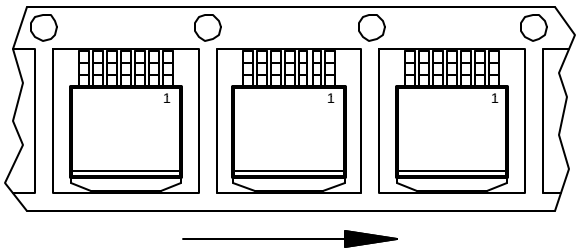


SYMBOL	MIN	MAX
A	9.27	9.52
A1	8.89	9.14
B	7.87	8.13
C	1.78	2.03
D	0.63	0.79
E	0.25 NOM	
G	1.27	
H	10.41	10.67
K	0.76	1.27
L	0.03	0.13
M	0.89	1.14
N	0.25	
P	0.79	1.04
R	3°	6°
U	5.59 NOM	
V	7.49 NOM	

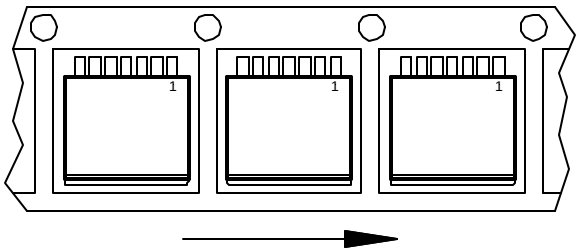
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
M	TO-263	7	50	750	Fig A
P	Ultra Thin-Pak™	7	75	2500	Fig B



Feed Direction
Figure A



Feed Direction
Figure B

International
IOR Rectifier

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TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information

IRU1205
IRU1205-18 / IRU1205-25 / IRU1205-28
IRU1205-30 / IRU1205-33 / IRU1205-36

300mA ULTRA LOW DROPOUT POSITIVE ADJUSTABLE AND FIXED REGULATORS

FEATURES

- SOT-23 Package
- Stable with 2.2μF Ceramic Capacitor
- 1% Voltage Reference Accuracy
- Only 270mV Dropout at 300mA and 170mV Dropout at 150mA
- 5μA Quiescent Current in Shutdown
- Current Limit and Thermal Shutdown
- Logic Input Enable Pin

APPLICATIONS

- Laptop, Notebook & Palmtop computers
- Battery Powered Equipments
- PCMCIA Vcc & Vpp Regulator
- Consumer Electronics
- High Efficiency Linear Power Supplies

DESCRIPTION

The IRU1205 device is an efficient linear voltage regulator with better than 1% initial voltage accuracy, very low dropout voltage and very low ground current designed especially for hand held, battery powered applications. Other features of the device are: TTL compatible enable/shutdown control input, current limiting and thermal shutdown.

The IRU1205 is available in fixed and adjustable output voltage versions in a small SOT-23 5-Pin package.

TYPICAL APPLICATION

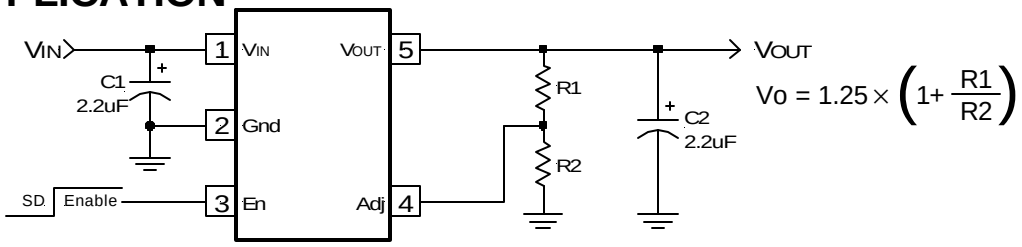


Figure 1 - Typical application of the IRU1205 ajustable voltage regulator.

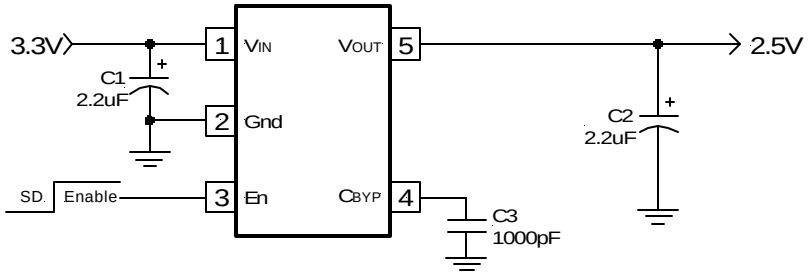


Figure 2 - Typical application of the IRU1205-25 fixed voltage regulator.

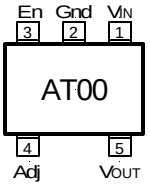
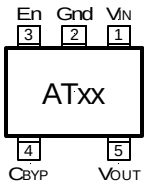
PACKAGE ORDER INFORMATION

T_J (°C)	5-PIN SOT-23 (L5)	SOT-23 MARKING	OUTPUT VOLTAGE
0 To 125	IRU1205CL	AT00	Adj
0 To 125	IRU1205-18CL	AT18	1.8V
0 To 125	IRU1205-25CL	AT25	2.5V
0 To 125	IRU1205-28CL	AT28	2.8V
0 To 125	IRU1205-30CL	AT30	3.0V
0 To 125	IRU1205-33CL	AT33	3.3V
0 To 125	IRU1205-36CL	AT36	3.6V

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 10V
Enable Input Voltage 10V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

5-PIN SOT-23 (L5)	5-PIN SOT-23 (L5)
	
Adjustable θ_{JA}=256°C/W	Fixed θ_{JA}=256°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=Co=22µF, Io=100µA, $V_{IN(MIN)}$=2.5V(Adjustable devices) V_{IN}=Vo + 1V(for fixed voltage devices), V_{OUT}=V_{FB}(for adjustable version only), C_{BYP}=470pF(for AT18, AT25, AT28, AT30, AT33 and AT36), V_{ENB}=2V and T_A=25°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	Vo		-1		1	%
(See Table 1 for typical values)		(Note 4)	-2		2	
Line Regulation	ΔV_I	Vo + 1V<V_{IN}<10V		0.005		%/V
Load Regulation (Note 1)	ΔV_L	1mA<Io<100mA		0.8		%
		100mA<Io<300mA		0.1		
Dropout Voltage (Note 2)	$\Delta V_{I(O)}$	Io=100µA		10	50	mV
		Io=100µA (Note 4)		13	70	
		Io=50mA		85	110	
		Io=50mA (Note 4)		100	140	
		Io=150mA		170	220	
		Io=150mA (Note 4)		204	260	
		Io=300mA		270	350	
		Io=300mA (Note 4)		324	400	
Ground Current (Note 3)	I_Q	V_{EN}=2V, Io=100µA		120	160	µA
		Io=100µA (Note 4)		240		
		Io=50mA		420	600	
		Io=50mA (Note 4)		540		
		Io=150mA		2200	2900	
		Io=150mA (Note 4)		2900		
		Io=300mA		7200	9500	
		Io=300mA (Note 4)		9300		
Ground Current-SD Activated	$I_{Q(SD)}$	V_{EN}=0V to 0.8V or Open		5		µA
Current Limit	I_{CL}	Vo=0V	320	420		mA
Thermal Regulation	ΔV_P	V_{IN}=10V, Io=150mA, 10ms Pulse		0.05		%/W
Adjust Pin Current	I_{ADJ}	V_{IN}=2.5V, Vo=V_{ADJ}		0.1		µA
Enable Pin Input LO Voltage	$V_{EN(L)}$	Regulator OFF			0.8	V
Enable Pin Input HI Voltage	$V_{EN(H)}$	Regulator ON	2			V
Enable Pin Input LO Current		$V_{EN(L)}$=0V to 0.8V		0.01		µA
Enable Pin Input HI Current		$V_{EN(H)}$=2V to V_{IN}		20		µA

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Ground current is the regulator quiescent current plus the pass transistor current. The total current from the supply is the sum of the load current plus the ground pin current.

Note 4: The specification applies for the junction temperature of 0 to +125°C.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be higher than V_{OUT} by at least the amount of the dropout voltage and some margin in order for the device to regulate properly.
2	Gnd	Ground pin. This pin must be connected to the lowest potential in the system and all other pins must be at higher potential with respect to this pin.
3	En	Enable pin. A low signal or left open on this pin shuts down the output. This pin must be tied HI or to V_{IN} for normal operation.
4	Adj (Adjustable Only)	A resistor divider from this pin to the V_{OUT} pin and ground sets the output voltage. To minimize the error due to the error amplifier, select the values of the resistor dividers to be less than 10KΩ.
4	C_{BYP} (Fixed Only)	A 470 to 1000pF bypass capacitor connected to this pin reduces the output noise.
5	V_{OUT}	The output of the regulator. A minimum of 2.2μF with max ESR of 1Ω capacitor must be connected from this pin to ground to insure stability.

5-PIN SOT-23	Output Voltage
IRU1205	1.25V
IRU1205-18	1.8V
IRU1205-25	2.5V
IRU1205-28	2.8V
IRU1205-30	3.0V
IRU1205-33	3.3V
IRU1205-36	3.6V

Table 1- Nominal output voltage vs. part number.

The output voltage of the adjustable device can be set using:

$$Vo = 1.25 \times \left(1 + \frac{R1}{R2}\right)$$

Where:
R1 = Resistor connected from output to the Adj pin
R2 = Resistor connected from Adj pin to Gnd

BLOCK DIAGRAM

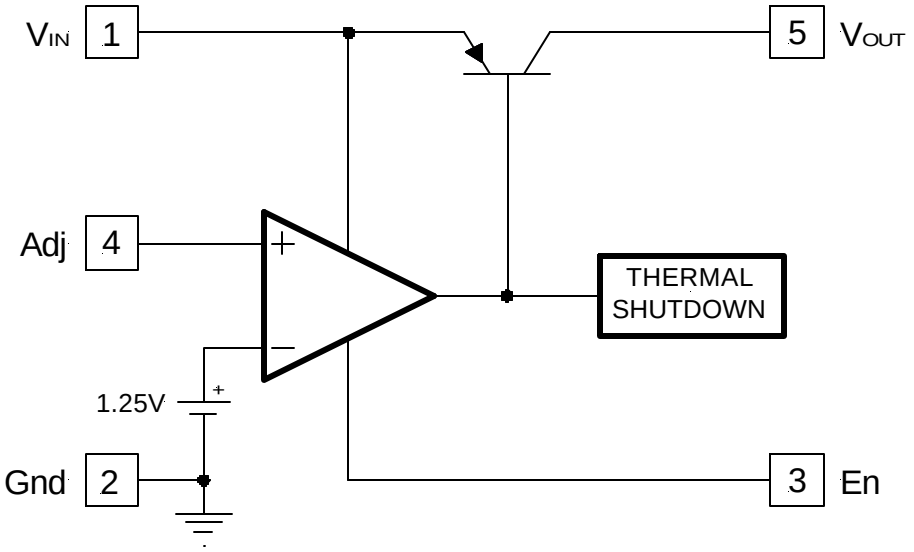


Figure 3 - IRU1205 Adjustable output block diagram.

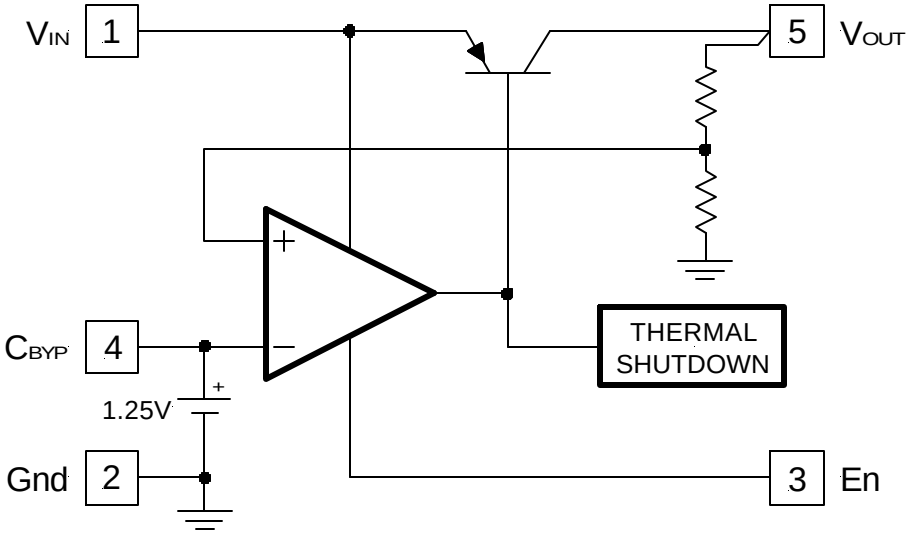


Figure 4 - IRU1205-18, IRU1205-25, IRU1205-28, IRU1205-30, IRU1205-33 and IRU1205-36 Fixed output block diagram.

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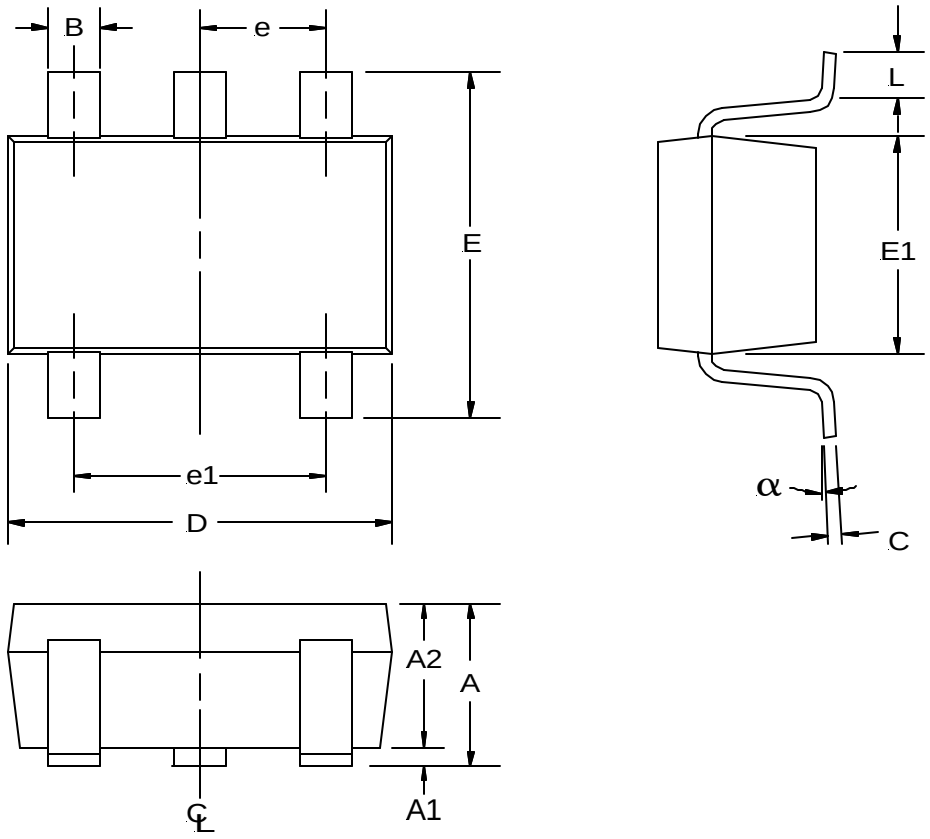
(L5) SOT-23 Package
5-Pin

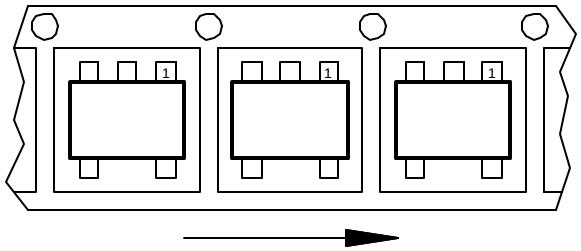


SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.25	0.50
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
e	0.95 REF	
e1	1.90 REF	
L	0.35	0.55
α	0°	10°

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
L5	SOT-23	5	---	3000	Fig A



Feed Direction
Figure A

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IRU1206 / IRU1207 / IRU1208 / IRU1209

1A VERY LOW DROPOUT POSITIVE FIXED AND ADJUSTABLE REGULATORS

FEATURES

- Low Dropout Voltage (500mV at 1A)
- 1% Voltage Reference Accuracy
- Low Ground Current
- 1μA Maximum Quiescent Current in Shutdown (IRU1207, IRU1208)
- Fast Transient Response
- Current Limit and Thermal Shutdown
- Error Flag Signal for Output out of Regulation (IRU1207, IRU1208)

APPLICATIONS

- 2.5V Supply from 3.3V Input for the new generation of Logic ICs
- Computer Mother Board, Add-On Cards
- High Efficiency Post Regulator in Switch Mode Power Supply (SMPS)

DESCRIPTION

The IRU1206 family of devices are ultra low dropout 1A regulators using PNP transistor as the pass element. These products are ideal when a single input supply is only available and the dropout voltage is less than 1V, exceeding the minimum dropout characteristics of NPN/ PNP hybrid regulators. One common application of these regulators is where input is 3.3V and a 2.5V output is needed.

Besides the low dropout of less than 0.5V, other features of the family of the parts are: micro-power shutdown capability and output UVLO detection where Flag pin is switched low when output is below 5% of its nominal point.

TYPICAL APPLICATION

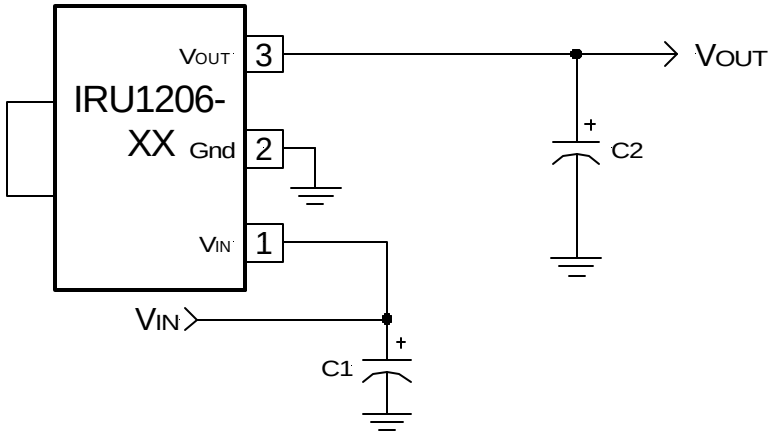


Figure 1 - Typical application of the 1206-XX in a 3-Pin SOT-223 package.

PACKAGE ORDER INFORMATION

T_J (°C)	2-PIN TO-252 (D-PAK)	3-PIN SOT-223 (Y)	8-PIN PLASTIC SOIC (S)	VOLTAGE	PIN FUNCTIONS
0 To 125	IRU1206-18CD	IRU1206-18CY	NA	1.8V	V_{IN}, V_{OUT}, Gnd
0 To 125	IRU1206-25CD	IRU1206-25CY	NA	2.5V	V_{IN}, V_{OUT}, Gnd
0 To 125	IRU1206-33CD	IRU1206-33CY	NA	3.3V	V_{IN}, V_{OUT}, Gnd
0 To 125	NA	NA	IRU1207-18CS	1.8V	V_{IN}, V_{OUT}, Gnd, Enable, Flag
0 To 125	NA	NA	IRU1207-25CS	2.5V	V_{IN}, V_{OUT}, Gnd, Enable, Flag
0 To 125	NA	NA	IRU1207-33CS	3.3V	V_{IN}, V_{OUT}, Gnd, Enable, Flag
0 To 125	NA	NA	IRU1208CS	Adj	V_{IN}, V_{OUT}, Gnd, Flag, Adj
0 To 125	NA	NA	IRU1209CS	Adj	V_{IN}, V_{OUT}, Gnd, Enable, Adj

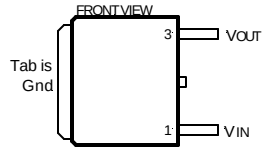
ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 12V
Enable Input Voltage 12V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 135°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)

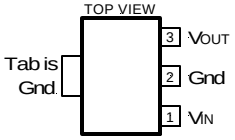
IRU1206



θ_{JA}=70°C/W for 0.5" Sq pad

3-PIN PLASTIC SOT-223 (Y)

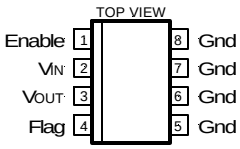
IRU1206



θ_{JA}=90°C/W for 0.4" Sq pad

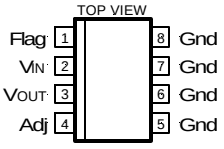
8-PIN PLASTIC SOIC (S)

IRU1207



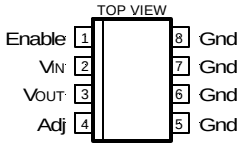
θ_{JA}=55°C/W for 1" Sq pad

IRU1208



θ_{JA}=55°C/W for 1" Sq pad

IRU1209



θ_{JA}=55°C/W for 1" Sq pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=C_{OUT}=10µF, V_{IN}=Vo+1V, V_{OUT}=V_{FB} (For adjustable version only), and T_A=25°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Initial Voltage Accuracy	Vo	Io=10mA, T_A=25°C	-1		1	%
(see Table 1 for nominal values)		(Note 4)	-1.3		1.3	
Line Regulation	ΔV_I	Vo + 1V<V_{IN}<12		0.5	1	%
Load Regulation (Note 1)	ΔV_L	10mA<Io<1A		0.5	0.7	%
		1mA<Io<150mA			0.5	
Output Voltage Temp Coef.	$\Delta V_{O(T)}$			20	100	ppm/°C
Dropout Voltage (Note 2)	$\Delta V_{I(O)}$	Io=100mA (Note 4)		100	200	mV
		Io=500mA (Note 4)		300	400	
		Io=1000mA (Note 4)		500	650	
Ground Current (Note 3)	I_Q	V_{IN}=Vo + 1 for all conditions:				
		Io=100mA (Note 4)			3	mA
		Io=500mA (Note 4)			15	
		Io=1000mA (Note 4)			50	
Current Limit	I_{CL}	Vo=5% Below Regulation Point	1.1	1.4		A
Minimum Input Voltage	$V_{IN(min)}$			2.1	2.3	V
IRU1208, IRU1209						
Adjust Pin Current	I_{ADJ}	V_{IN}=2.5V, Vo=V_{ADJ} (Note 4)			0.1	µA
Minimum Load Current	$I_{O(min)}$		1			mA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
IRU1207, IRU1209						
Ground Current - SD Activated	$I_{Q(SD)}$	Enable=Open		0.01	1	µA
Enable Pin Input LO Voltage	$V_{EN(L)}$	Regulator OFF (Note 4)			0.8	V
Enable Pin Input HI Voltage	$V_{EN(L)}$	Regulator ON (Note 4)	2			V
Enable Pin Input LO Current		$V_{EN(L)}$=0V to 0.8V (Note 4)		0.1	2	µA
Enable Pin Input HI Current		$V_{EN(L)}$=2V to Vin (Note 4)		100	600	µA
IRU1207, IRU1208						
Flag Output Threshold Voltage	$V_{TH(FG)}$			5		$\%V_O$
Flag Output Hysteresis Voltage	V_{HYS}	Output Ramping Up		0.8		$\%V_O$
Flag Output Saturation Voltage	$V_{F(SAT)}$	Io=5mA		400		mV
		Io=500µA		230		

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Ground current is the regulator quiescent current plus the pass transistor current. The total current from the supply is the sum of the load current plus the ground pin current.

Note 4: The specification applies for the junction temperature of 0 to +125°C.

PIN DESCRIPTIONS

PIN SYMBOL	PIN DESCRIPTION
V_{IN} (All devices)	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be 0.6V higher than V_{OUT} in order for the device to regulate properly.
V_{OUT} (All devices)	The output of the regulator. A minimum of 2.2µF capacitor must be connected from this pin to ground.
Gnd (All devices)	Ground pin. This pin must be connected to the lowest potential in the system and all other pins must be at higher potential with respect to this pin.
Enable (IRU1207, IRU1209)	Enable pin. A low signal or left open on this pin shuts down the output. This pin must be tied HI or to V_{IN} for normal operation.
Flag (IRU1207, IRU1208)	An open collector output that switches low when the output voltage drops about 4% below its expected regulated voltage.
Adj (IRU1208, IRU1209)	A resistor divider from this pin to the V_{OUT} pin and ground sets the output voltage.

APPLICATION INFORMATION

Stability

The IRU120X series of regulators require the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. A minimum of 2.2µF capacitance and the ESR in the range of 0.5 to 2Ω insures the stability of the system.

Part Number	Output Voltage
IRU1206-18	1.8V
IRU1206-25	2.5V
IRU1206-33	3.3V
IRU1207-18	1.8V
IRU1207-25	2.5V
IRU1207-33	3.3V
IRU1208	1.24V
IRU1209	1.24V

Table 1 - Output voltage vs. part number.

TYPICAL APPLICATION

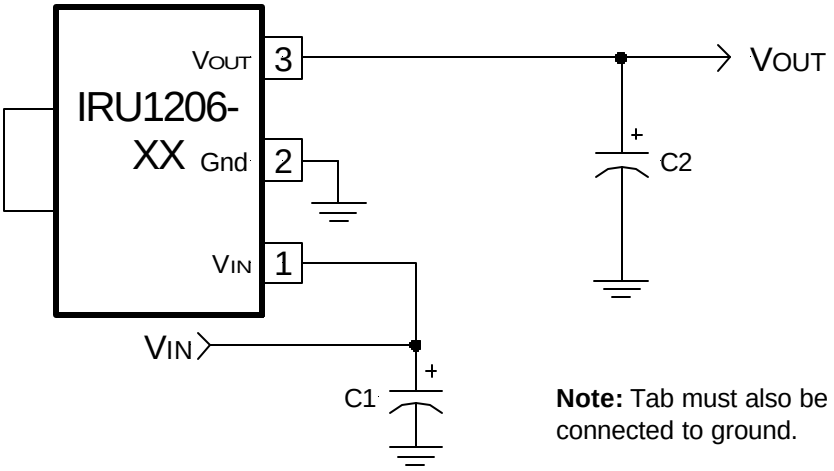


Figure 2 - Typical application of IRU1206.

Ref Desig	Description	Qty	Part #	Manuf
C1	Capacitor	1	10μF, Tantalum	AVX
C2	Capacitor	1	10μF, Tantalum	AVX

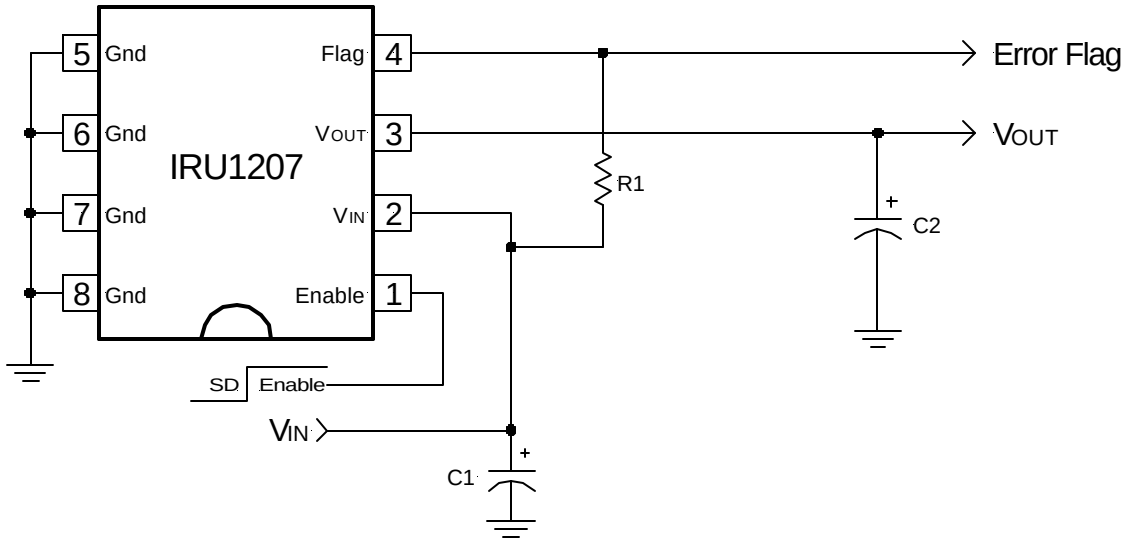


Figure 3 - Typical application of IRU1207.

Ref Desig	Description	Qty	Part #	Manuf
C1	Capacitor	1	10μF, Tantalum	AVX
C2	Capacitor	1	10μF, Tantalum	AVX
R1	Resistor	1	10KΩ, 5%	Panasonic

TYPICAL APPLICATION

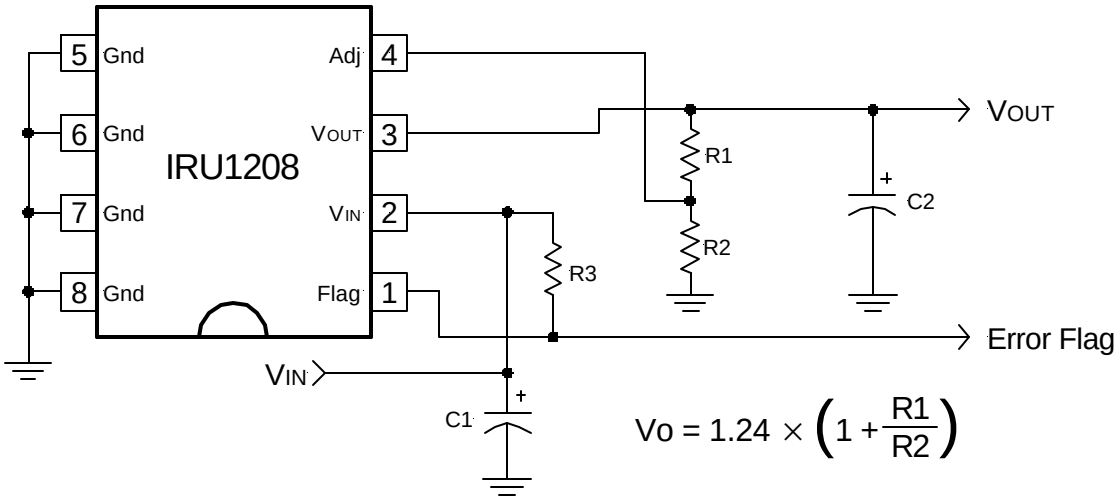


Figure 4 - Typical application of IRU1208 in 3.3V to 2.5V regulator.

Ref Desig	Description	Qty	Part #	Manuf
C1	Capacitor	1	10μF, Tantalum	AVX
C2	Capacitor	1	10μF, Tantalum	AVX
R1	Resistor	1	127Ω, 1%	
R2	Resistor	1	124Ω, 1%	
R3	Resistor	1	10KΩ, 5%	

TYPICAL APPLICATION

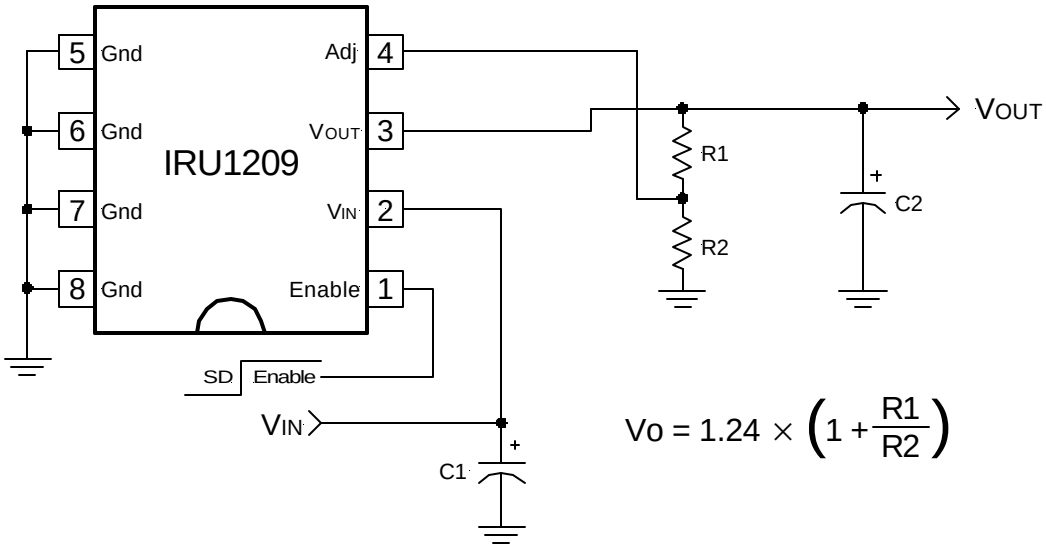


Figure 5 - Typical application of IRU1209 in 3.3V to 2.5V regulator.

Ref Desig	Description	Qty	Part #	Manuf
C1	Capacitor	1	10μF, Tantalum	AVX
C2	Capacitor	1	10μF, Tantalum	AVX
R1	Resistor	1	127Ω, 1%	
R2	Resistor	1	124Ω, 1%	

CHARACTERISTICS

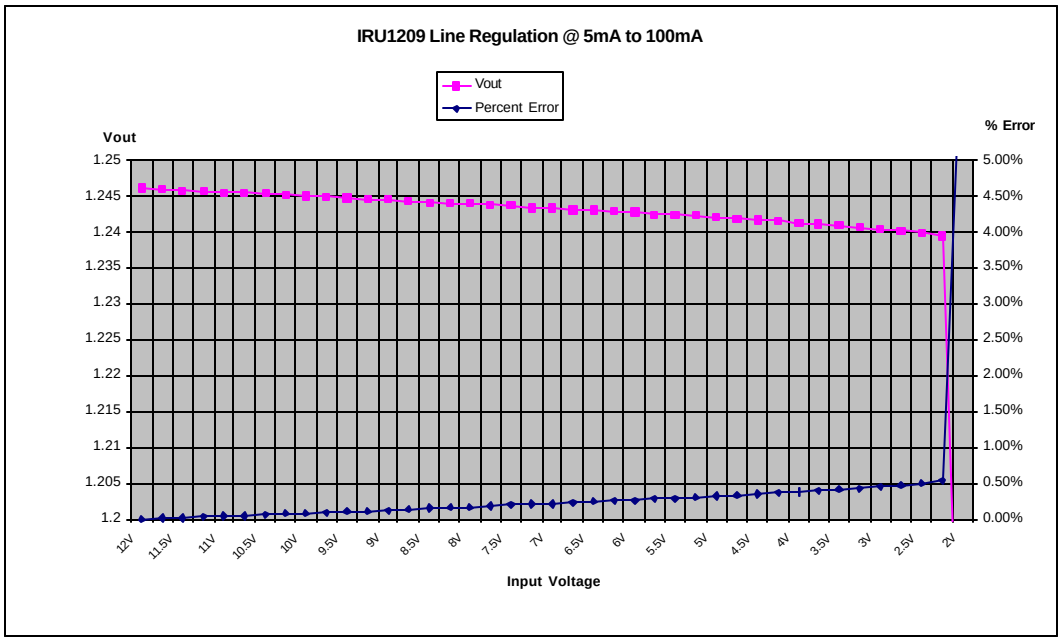


Figure 6

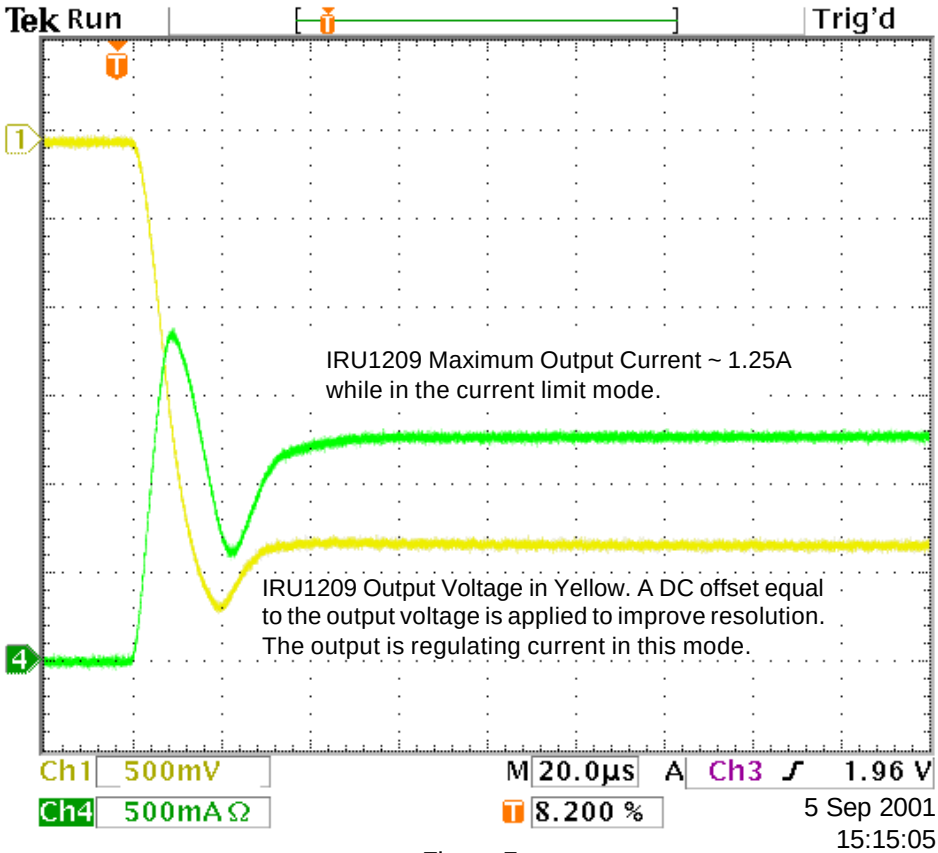


Figure 7

CHARACTERISTICS

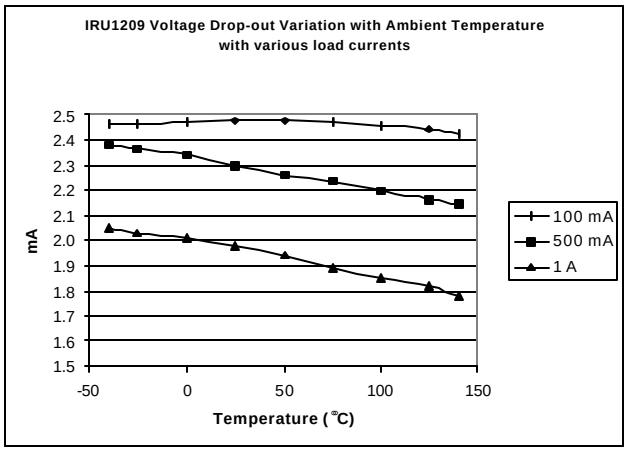


Figure 8

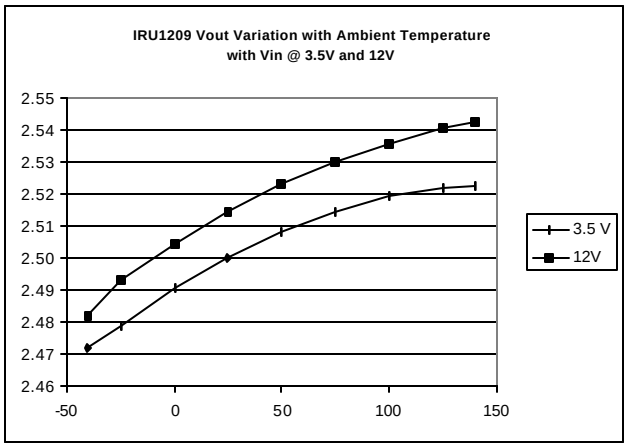


Figure 9

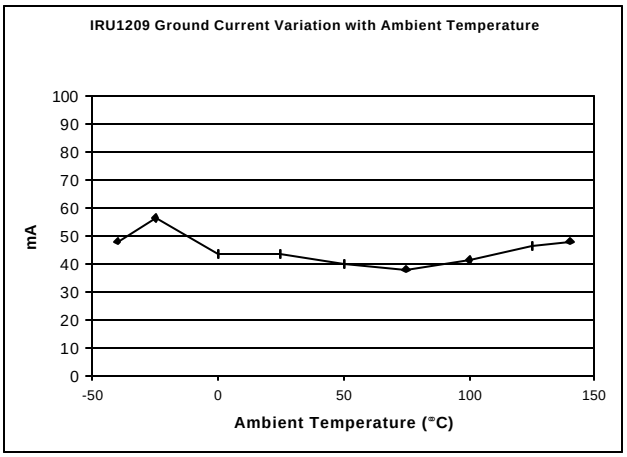


Figure 10

International
IOR Rectifier

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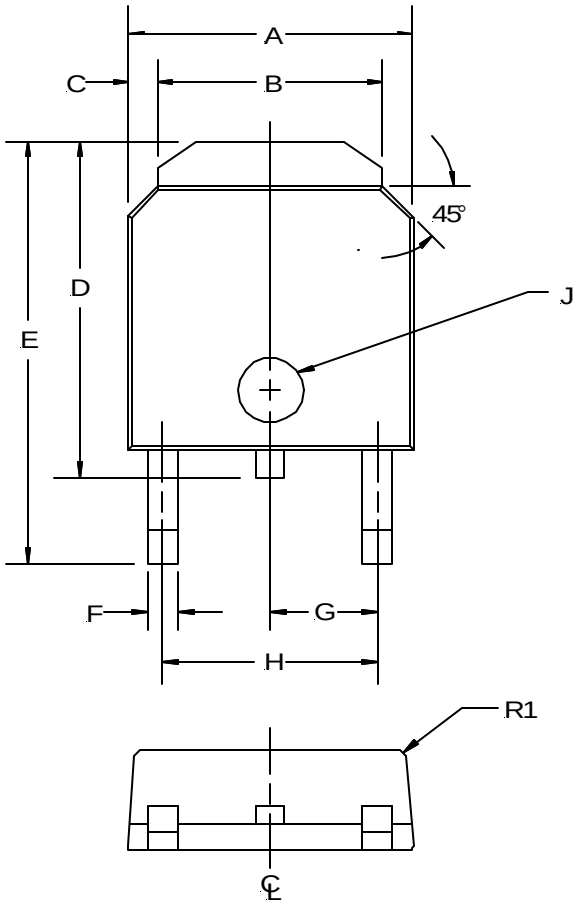
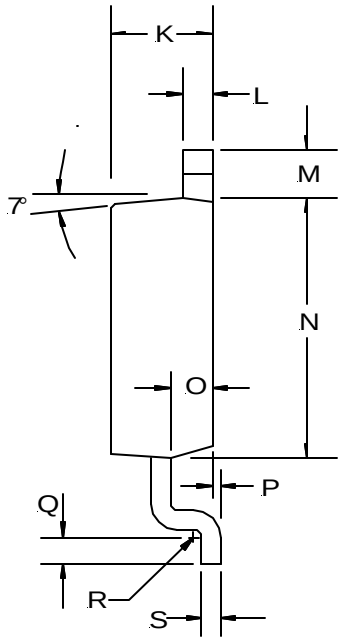
(D) TO-252 Package
2-Pin

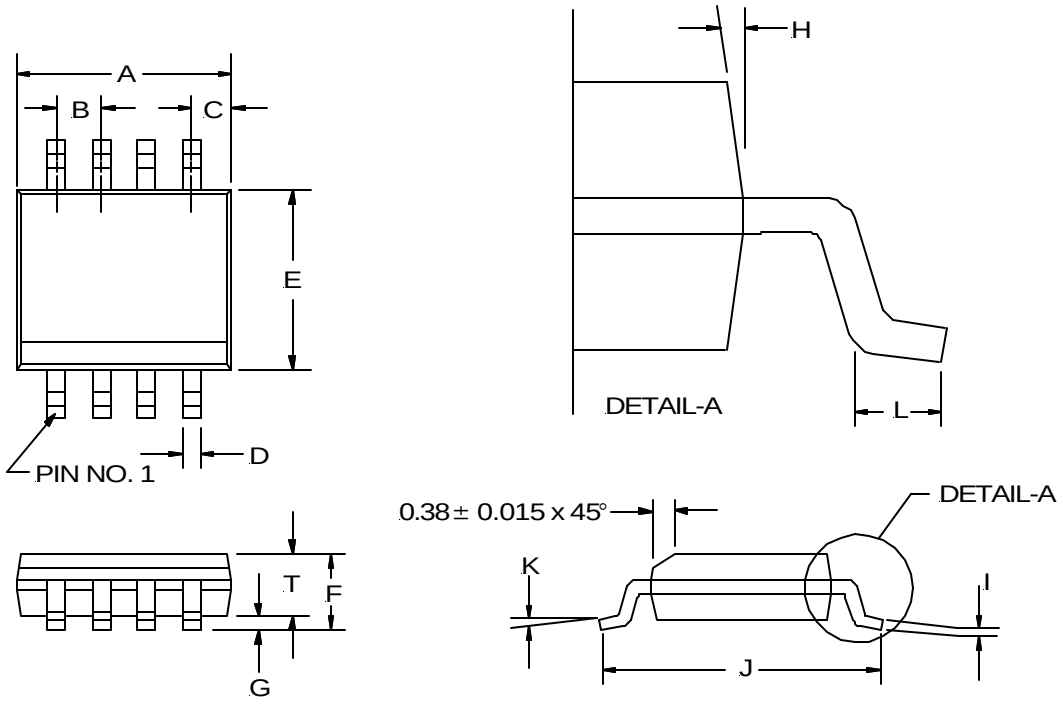




SYMBOL	MIN	MAX
A	6.477	6.731
B	5.004	5.207
C	0.686	0.838
D	7.417	8.179
E	9.703	10.084
F	0.635	0.889
G	2.286 BSC	
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

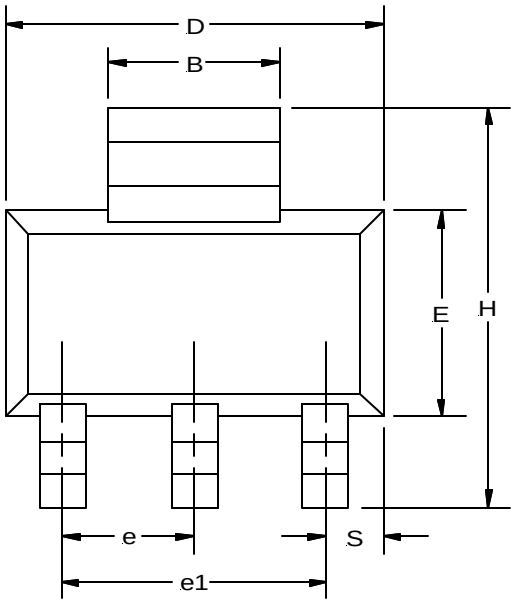
(S) SOIC Package
8-Pin Surface Mount, Narrow Body



8-PIN		
SYMBOL	**MIN**	**MAX**
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

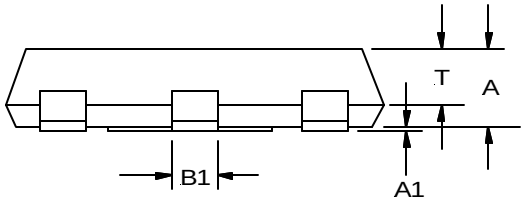
NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

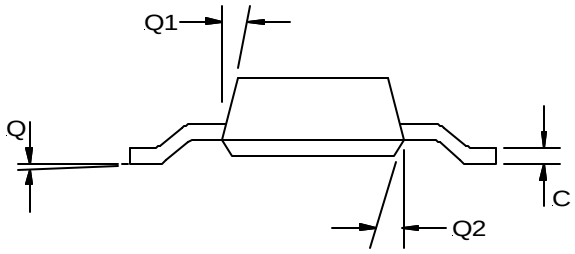
(Y) SOT-223 Package
3-Pin



SYMBOL	MIN	MAX
A	1.498	1.702
A1	0.02	0.11
B	2.895	3.15
B1	0.637	0.85
C	0.239	0.381
D	6.299	6.706
E	3.30	3.708
e	2.209	2.953
e1	4.496	4.699
H	6.70	7.30
Q	0°	10°
Q1	7°	16°
Q2	7°	16°
S	0.838	1.05
T	1.092	1.30

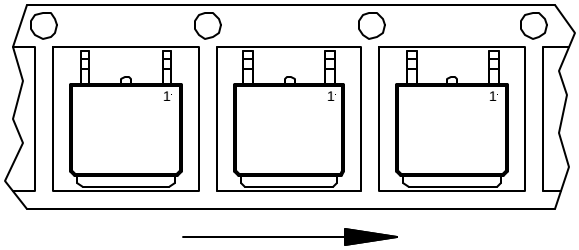
NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.



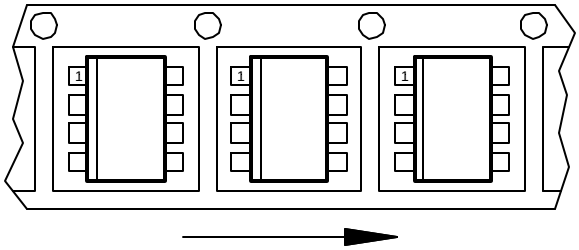


PACKAGE SHIPMENT METHOD

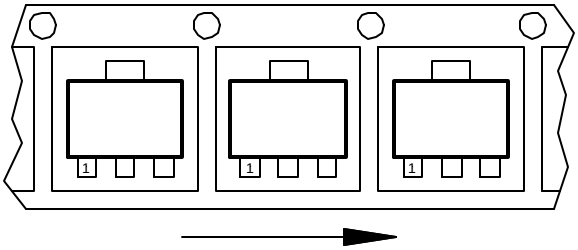
PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
S	SOIC, Narrow Body	8	95	2500	Fig B
Y	SOT-223	3	80	2500	Fig C



Feed Direction
Figure A



Feed Direction
Figure B



Feed Direction
Figure C

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information

Section 3: Dual Low Dropout Regulators

DUAL LOW DROPOUT SELECTION GUIDE

	FEATURES				PACKAGES							
Part #	Io (A)	Max Dropout (V)	Adj/ Fix (V)	NOTES	TO-252 5-Pin D-Pak	TO-263 5-Pin	TO-263 7-Pin	5-Pin UThin-Pak	7-Pin UThin-Pak	8-Pin SOIC Pwr	TO-220 5-Pin	TO-220 7-Pin
					D	M	M	P	P	S	T	T
IRU1260												
Output 1	1	1.3	ADJ	As single supply input			X		X			
	1	0.6	1.25 - 5.5	As dual supply input								
Output 2	6	1.3	ADJ	As single supply input								
	4	1.0	1.25 - 5.5	As dual supply input								
IRU1261												
Output 1	1	1.3	FIX	As single supply input		X		X				
	1	0.6	2.5	As dual supply input								
Output 2	6	1.3	FIX	As single supply input								
	4	1.0	1.5	As dual supply input								

International
IOR Rectifier

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TAC Fax: (310) 252-7903
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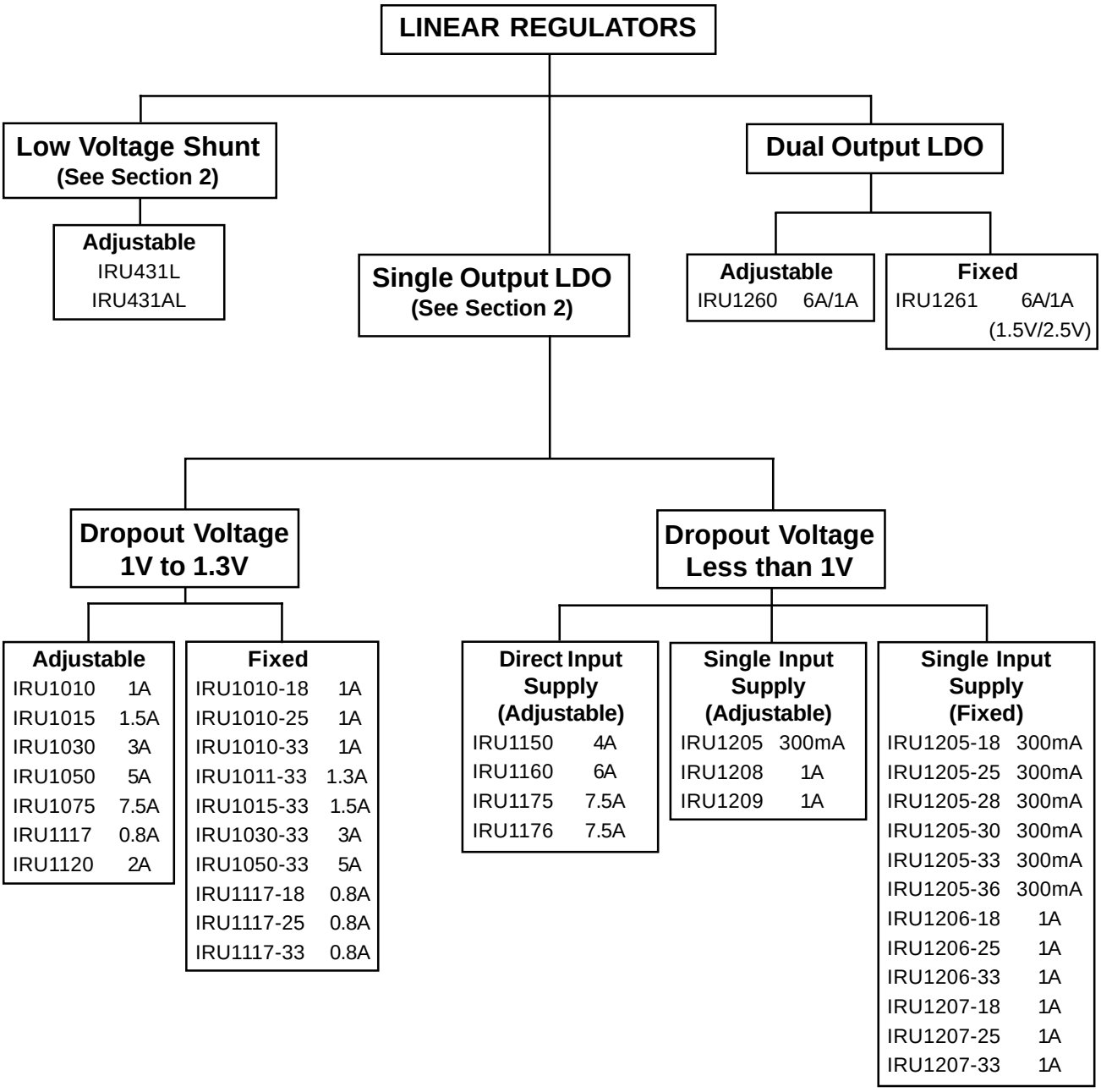
Selection Tree



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
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IRU1260

DUAL 6A AND 1A LOW DROPOUT POSITIVE ADJUSTABLE REGULATOR

FEATURES

- Guaranteed <1.3V Dropout at 6A (Output #2)
- Guaranteed <0.6V Dropout at 1A (Output #1)
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown

APPLICATIONS

- Providing a Single Package Solution for GTL+ and High Speed Bus Termination
- Dual Supply P55C™ Applications

DESCRIPTION

The IRU1260 uses a proprietary process and combines a dual low dropout adjustable output regulator in a single package with one output having a minimum of 6A and the other one having a 1A output current capability. This product is specifically designed to provide well regulated supplies for low voltage ICs such as 3.3V to 1.5V and 2.5V supplies for the GTL+ termination and the new clock for Pentium II™ applications. Other applications include low cost dual supply for processors such as Intel P55C™ where 2.8V and 3.3V are needed for the Core and the I/O supplies from the 5V input.

TYPICAL APPLICATION

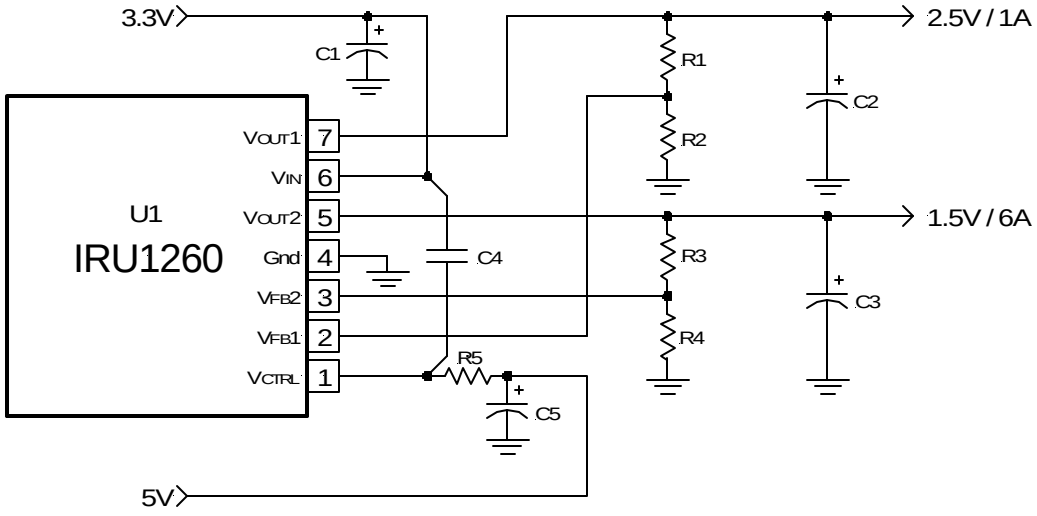


Figure 1 - Typical application of IRU1260 in the Pentium II™ design with the 1.5V output providing for GTL+ termination while 2.5V supplies the clock chip.

Notes: Pentium II™ is trademark of Intel Corp.
P55C™ is trademark of Intel Corp.

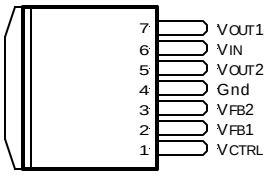
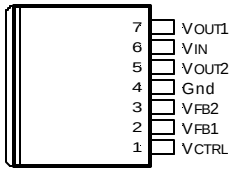
PACKAGE ORDER INFORMATION

T_J (°C)	7-PIN PLASTIC TO-263 (M)	7-PIN PLASTIC Ultra Thin-Pak™ (P)
0 To 150	IRU1260CM	IRU1260CP

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

7-PIN PLASTIC TO-263 (M)	7-PIN ULTRA THIN-PAK (P)
	
θ_{JA}=30°C/W for 1"sq pad	θ_{JA}=30°C/W for 1"sq pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=10µF and T_J=0 to 150°C. Typical values refer to T_J=25°C. I_{FL}=6A for output #1 and I_{FL}=1A for output #2. V_{FB}=V_{OUT} for both outputs. V_{CTRL}=V_{IN}=3.3V.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
V_{CTRL} Input Voltage			3.0			V
Reference Voltage	V_{REF}	Io=10mA, T_J=25°C	1.188	1.200	1.212	V
		Io=10mA	1.176	1.200	1.224	
Line Regulation		Io=10mA, V_{OUT}+1.3V<V_{IN}=V_{CTRL}<7V		0.2		%
Load Regulation (Note 1)		10mA<Io<I_{FL}		0.4		%
Dropout Voltage (Output #2)		Io=4A, V_{CTRL}=4.75V, V_{IN}=3.3V			1.0	V
(Note 2)		Io=3A, V_{CTRL}=4.75V, V_{IN}=3.3V			0.7	
		Io=2A, V_{CTRL}=4.75V, V_{IN}=3.3V		0.35	0.5	
Dropout Voltage (Output #1)		Io=1A, V_{CTRL}=4.75V, V_{IN}=3.3V		0.4	0.6	V
(Note 2)		Io=1A, V_{CTRL}=V_{IN}=4.75V			1.3	
Current Limit (Output #2)	I_{CL2}	ΔVo=100mV	6.1			A
Current Limit (Output #1)	I_{CL1}	ΔVo=100mV	1.1			A
Thermal Regulation		30ms pulse, Io=I_{FL}		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum, Io=0.5 × I_{FL}		70		dB
Feedback Pin Input Current	I_{FB}	Io=10mA		0.02		µA
Temperature Stability		Io=10mA		0.5		%
Long Term Stability		T_A=125°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_A=25°C, 10Hz<f<10KHz		0.003		%V_O
Minimum Load Current (Note 3)				5		mA

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor divider values are selected such that this current is automatically maintained.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	V_{CTRL}	The control input pin of the regulator. This pin via a 10Ω resistor is connected to the 5V supply to provide the base current for the pass transistor of both regulators. This allows the regulator to have very low dropout voltage which allows one to generate a well regulated 2.5V supply from the 3.3V input. A high frequency, 1µF capacitor is connected between this pin and V_{IN} pin to insure stability.
2	$V_{FB}1$	A resistor divider from this pin to $V_{OUT}1$ pin and ground sets the output voltage. See application circuit for the divider setting for 2.5V output.
3	$V_{FB}2$	A resistor divider from this pin to the $V_{OUT}2$ pin and ground sets the output voltage. See application circuit for the divider setting for 1.5V output.
4	Gnd	This pin is connected to ground. It is also the tab of the package.
5	$V_{OUT}2$	The output #2 (high current) of the regulator. A minimum of 100µF capacitor must be connected from this pin to ground to insure stability.
6	V_{IN}	The power input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum dropout voltage during the load transient response. This pin must always be higher than both V_{OUT} pins by the amount of the dropout voltage in order for the device to regulate properly.(See data sheet)
7	$V_{OUT}1$	The output #1 (low current) of the regulator. A minimum of 100µF capacitor must be connected from this pin to ground to insure stability.

BLOCK DIAGRAM

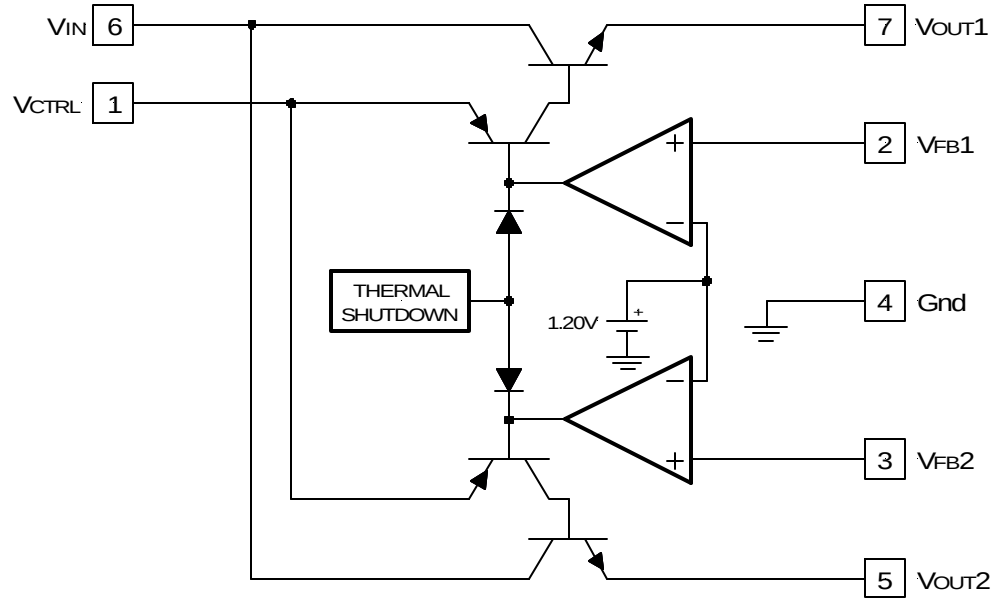


Figure 2 - Simplified block diagram of the IRU1260.

APPLICATION INFORMATION

Introduction

The IRU1260 is a dual adjustable Low Dropout (LDO) regulator which can easily be programmed with the addition of two external resistors to any voltages within the range of 1.20 to 5.5V. This voltage regulator is designed specifically for applications that require two separate regulators such as the Intel Pentium II™ processors requiring 1.5V and 2.5V supplies, eliminating the need for a second regulator which results in lower overall system cost. When V_{CTRL} pin is connected to a supply which is at least 1V higher than V_{IN}, the dropout voltage improves by 30% which makes it ideal for applications requiring less than the standard 1.3V dropout given in the LDO products such as IRU10XX series. The IRU1260 also provides an accurate 1.20V voltage reference common to both regulators for programming each output voltage. Other features of the device include: fast response to sudden load current changes, such as GTL+ termination application for Pentium II™ family of microprocessors. The IRU1260 also includes thermal shutdown protection to protect the device if an overload condition occurs.

Output Voltage Setting

The IRU1260 can be programmed to any voltages in the range of 1.20V to 5.5V with the addition of R1 and R2 external resistors according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1}\right) + R_2 \times I_B$$

Where:
V_{REF} = 1.20V Typically
I_B = 0.02μA Typical
R1 and R2 as shown in Figure 3:

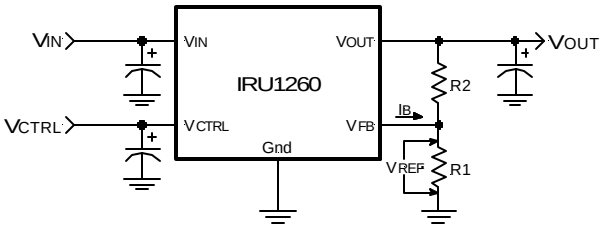


Figure 3 - Typical application of the IRU1260 for programming the output voltage. (Only one output is shown here)

The IRU1260 keeps a constant 1.2V between the V_{FB} pin and ground pin. By placing a resistor R1 across these two pins a constant current flows through R1, adding to the I_{FB} current and into the R2 resistor producing a voltage equal to the $(1.2/R1) \times R2 + I_{FB} \times R2$ which will be added to the 1.2V to set the output voltage as shown in the above equation. Since the input bias current of the amplifier (I_{FB}) is only 0.02μA typically, it adds a very small error to the output voltage and for most applications can be ignored. For example, in a typical 1.5V GTL+application if R1=10.2KΩ and R2=2.55KΩ the error due to the I_{ADJ} is only 0.05mV which is less than 0.004% of the nominal set point. The effective input impedance seen by the feedback pins (The parallel combination of R1 and R2) must always be higher than 1.8KΩ in order for the regulator to start up properly.

Load Regulation

Since the IRU1260 does not provide a separate ground pin for the reference voltage, it is not possible to provide true remote sensing of the output voltage at the load. Figure 4 shows that the best load regulation is achieved when the bottom side of R1 resistor is connected directly to the ground pin of IRU1260 (preferably to the tab of the device) and the top side of R2 resistor is connected to the load. In fact, if R1 is connected to the load side, the effective resistance between the regulator and the load is gained up by the factor of (1+R2/R1), or the effective resistance will be, $R_{P(eff)} = R_P \times (1+R2/R1)$. It is important to note that for high current applications, this can represent a significant percentage of the overall load regulation and one must keep the path from the regulator to the load as short as possible to minimize this effect.

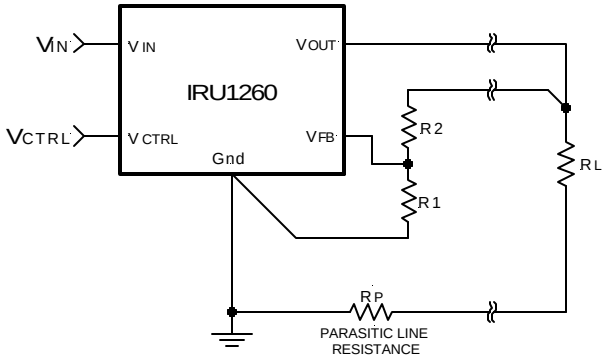


Figure 4 - Schematic showing connection for best load regulation. (Only one output is shown here)

Stability

The IRU1260 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for the microprocessor applications use standard electrolytic capacitors with typical ESR in the range of 50 to 100mΩ and the output capacitance of 500 to 1000μF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1260 takes advantage of this phenomena in making the overall regulator loop stable. For most applications a minimum of 100μF aluminum electrolytic capacitor with the maximum ESR of 0.3Ω such as Sanyo, MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response. The IRU1260 also requires a 1μF ceramic capacitor connected from V_{IN} to V_{CTRL} and a 10Ω, 0.1W resistor in series with V_{CTRL} pin in order to further insure stability.

Thermal Design

The IRU1260 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the maximum allowable junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. The example given shows the steps in selecting the proper regulator heat sink for driving the Pentium II™ processor GTL+ termination resistors and the Clock IC using the IRU1260 TO-263 package.

Example**:**

Assuming the following specifications:

V_{IN} = 3.3V
V_{OUT1} = 2.5V
V_{OUT2} = 1.5V
$I_{OUT1(MAX)}$ = 0.2A
$I_{OUT2(MAX)}$ = 1.5A
T_A = 35°C

The steps for selecting a proper heat sink to keep the junction temperature below 135°C is given as:

1) Calculate the maximum power dissipation using:

$$P_D = I_{OUT1} \times (V_{IN} - V_{OUT1}) + I_{OUT2} \times (V_{IN} - V_{OUT2})$$

$$P_D = 0.2 \times (3.3 - 2.5) + 1.5 \times (3.3 - 1.5) = 2.86W$$

2) Assuming a TO-263 surface mount package, the junction to ambient thermal resistance of the package is:

θ_{JA} = 30°C/W for 1" square pad area

3) The maximum junction temperature of the device is calculated using the equation below:

$$T_J = T_A + P_D \times \theta_{JA}$$

$$T_J = 35 + 2.86 \times 30 = 121°C$$

Since this is lower than our selected 135°C maximum junction temperature (150°C is the thermal shutdown of the device), TO-263 package is a suitable package for our application.

Layout Consideration

The IRU1260 like all other high speed linear regulators need to be properly laid out to insure stable operation. The most important component is the output capacitor, which needs to be placed close to the output pin and connected to this pin using a plane connection with a low inductance path.

IRU1260 in Ultra LDO, Single Output Application

The IRU1260 can also be used in single supply applications where the difference between input and output is much lower than the standard 1.5V dropout that is obtainable with standard LDO devices. The schematic in Figure 7 shows the application of the IRU1260 in a single supply with the second LDO being disabled.

In this application, the IRU1260 is used on the VGA card to convert 3.3V supply to 2.7V to power the Intel 740 chip rather than the conventional LDO which due to its 1.5V minimum dropout spec must use the 5V supply to achieve the same result. The difference is a substantial decrease in the power dissipation as shown below.

The maximum power dissipation of the Intel 740 chip is 5.8W, which at 2.7V results in:

$$Io = \frac{5.8}{2.7} = 2.15A$$

a) Using standard LDO, the power dissipated in the device is:

$$P_D = (V_{IN} - Vo) \times Io = (5 - 2.7) \times 2.15 = 4.94W$$

Using surface mount TO-263 package with 25°C/W junction to air thermal resistance results in:

$$T_J = P_D \times \theta_{JA} + T_A = 4.94 \times 25 + 25 = 148°C$$

This is very close to the thermal shutdown of the IC.

b) Using IRU1260, the power dissipated in the device is drastically reduced by using 3.3V supply instead of 5V.

$$P_D = (V_{IN} - Vo) \times Io = (3.3 - 2.7) \times 2.15 = 1.3W$$

Using surface mount TO-263 package with 25°C/W junction to air thermal resistance results in:

$$T_J = P_D \times \theta_{JA} + T_A = 1.3 \times 25 + 25 = 57°C$$

A reduction of 91°C in junction temperature.

TYPICAL APPLICATION

PENTIUM II ä APPLICATION

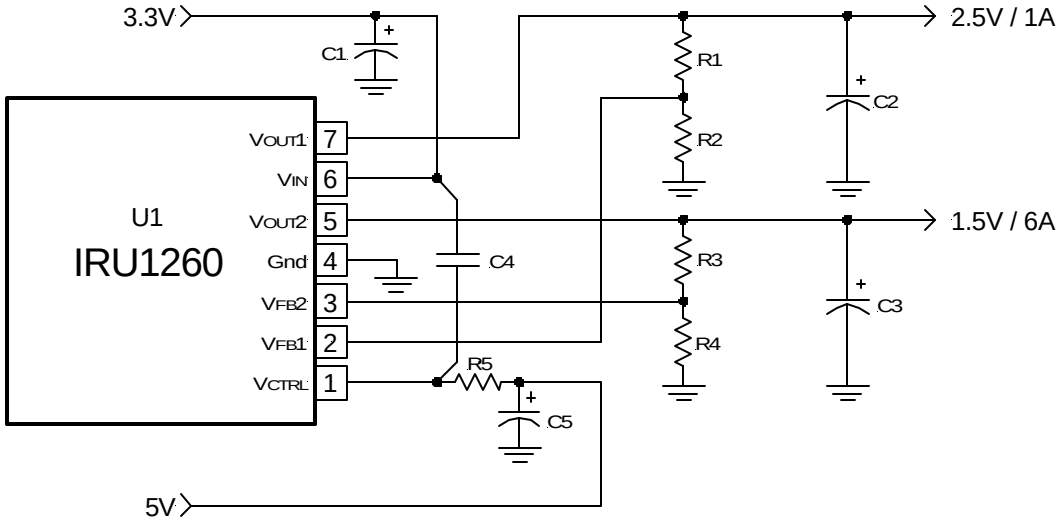


Figure 5 - Typical application of IRU1260 in the Pentium II™ design with the 1.5V output providing for GTL+ termination while 2.5V supplies the clock chip.

Note: Pentium II is trademark of Intel Corp.

Ref Desig	Description	Qty	Part #	Manuf
U1	Dual LDO Regulator	1	IRU1260CM	IR
C1, C3	Capacitor	2	Elect, 680µF, EEUFA1A681L	Panasonic
C2	Capacitor	1	Elect, 220µF, 6.3V, ECAOJFQ221	Panasonic
C4	Capacitor	1	Ceramic, 0.1µF, SMT, 0805	Panasonic
C5	Capacitor	1	Elect,100µF, 6.3V, ECAOJFQ101	Panasonic
R1	Resistor	1	11KΩ, 1%, SMT, 0805	Panasonic
R2, R4	Resistor	2	10.2KΩ, 1%, SMT, 0805	Panasonic
R3	Resistor	1	2.55KΩ, 1%, SMT, 0805	Panasonic
R5	Resistor	1	3Ω, 5%, SMT, 0805	Panasonic
HS1	Heat Sink		Use 1" Square Copper Pad area if I_{OUT2}<1.7A & I_{OUT1}<0.2A. For I_{OUT2}<3A & I_{OUT1}<0.5A, use IRU1260CT and Thermalloy 6030B	

TYPICAL APPLICATION

RAMBUS APPLICATION

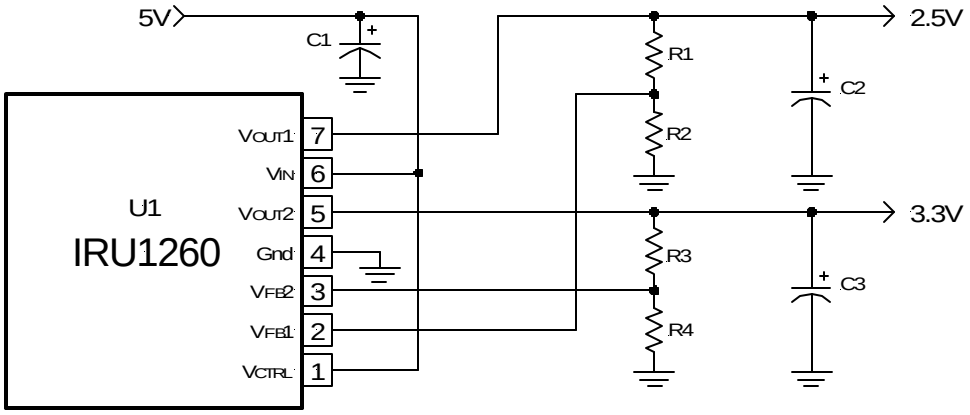


Figure 6 - Typical application of IRU1260 in the Rambus™ design with the 2.5V output providing for memory termination while 3.3V supplies the on board logic.

Note: Rambus™ is trademark of Rambus Corp.

Ref Desig	Description	Qty	Part #	Manuf
U1	Dual LDO Regulator	1	IRU1260CM	IR
C1, C2, C3	Capacitor	3	Elect, 220µF, 6.3V, ECAOJFQ221	Panasonic
R1	Resistor	1	11KΩ, 1%, SMT, 0805	Panasonic
R2, R4	Resistor	2	10.2KΩ, 1%, SMT, 0805	Panasonic
R3	Resistor	1	17.8KΩ, 1%, SMT, 0805	Panasonic
HS1	Heat Sink		1" Square Copper Pad area if I_{OUT2}<1.2A & I_{OUT1}<0.5A. For I_{OUT2}<3A & I_{OUT1}<0.5A, use Thermalloy 6030B	

TYPICAL APPLICATION

INTEL 740 GRAPHICS CHIP APPLICATION

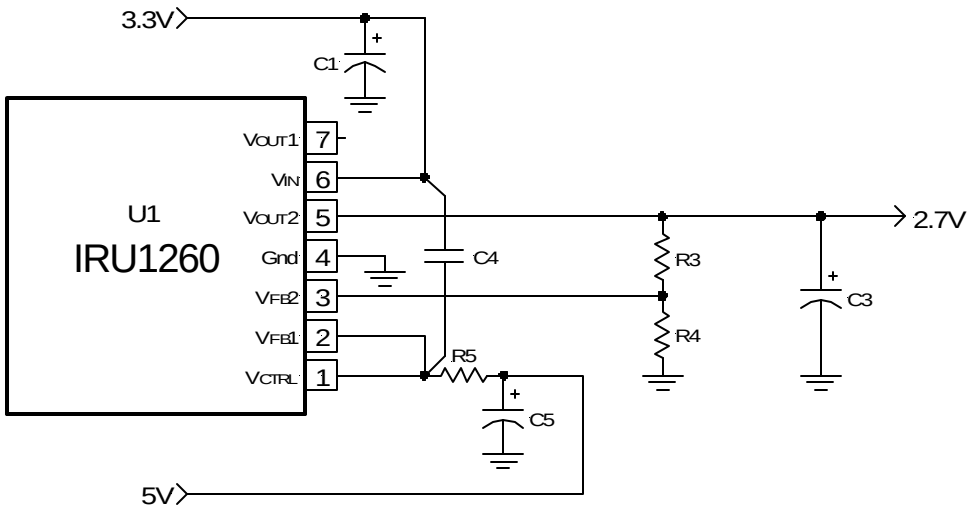


Figure 7 - Typical application of IRU1260 to provide 2.7V from the 3.3V bus for the Intel 740 graphics chip.

Ref Desig	Description	Qty	Part #	Manuf
U1	Dual LDO Regulator	1	IRU1260CM	IR
C1, C3	Capacitor	2	Elect, 680μF, EEUFA1A681L	Panasonic
C4	Capacitor	1	Ceramic, 0.1μF, SMT, 0805	Panasonic
C5	Capacitor	1	Elect,100μF, 6.3V, ECAOJFQ101	Panasonic
R4	Resistor	1	10.2KΩ, 1%, SMT, 0805	Panasonic
R3	Resistor	1	12.7KΩ, 1%, SMT, 0805	Panasonic
R5	Resistor	1	3Ω, 5%, SMT, 0805	Panasonic

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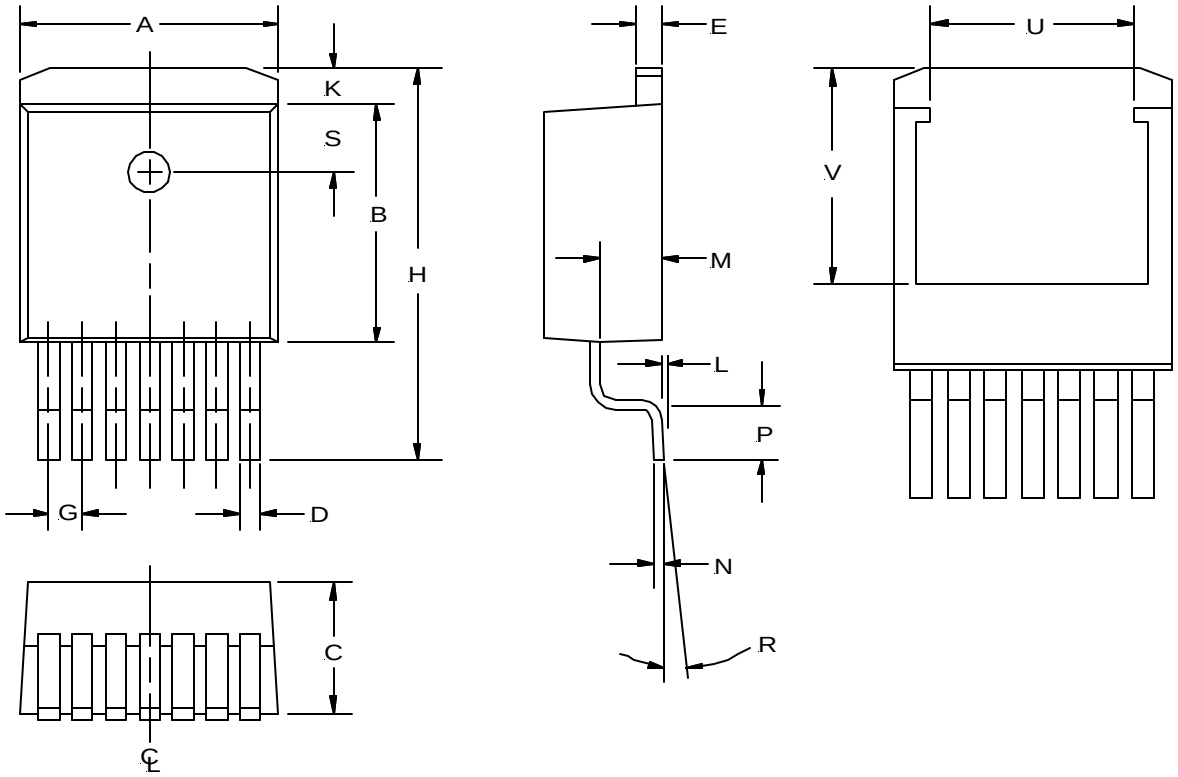
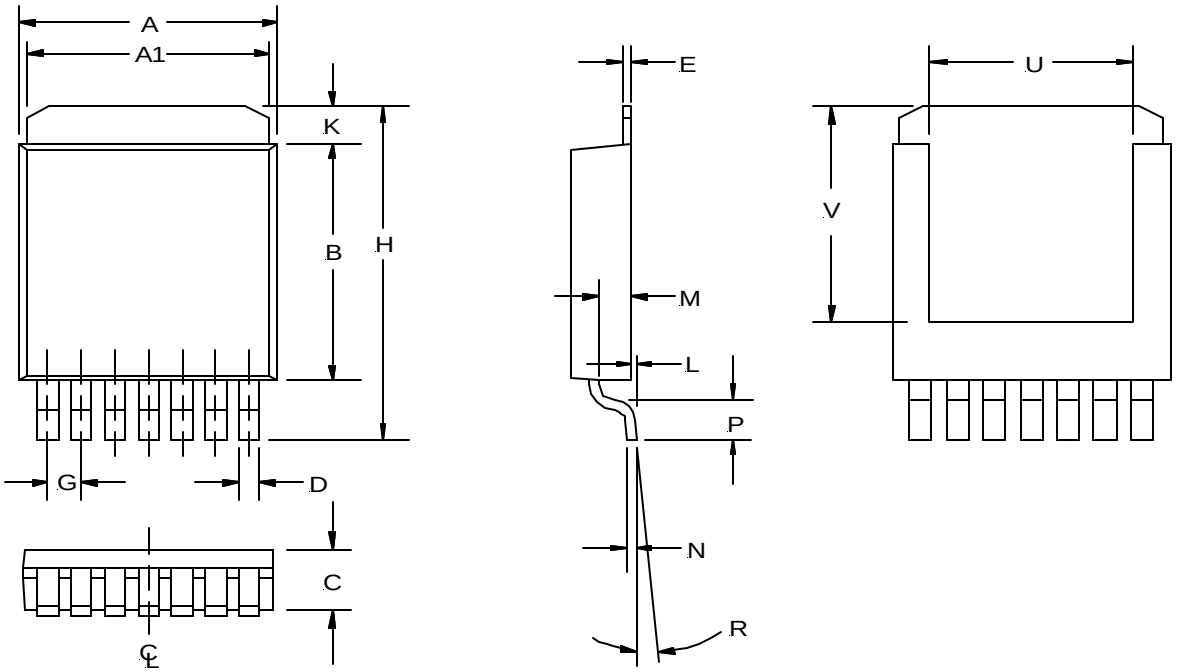
(M) TO-263 Package
7-Pin



SYMBOL	MIN	MAX
A	10.05	10.31
B	8.28	8.53
C	4.31	4.57
D	0.66	0.91
E	1.14	1.40
G	1.27 REF	
H	14.73	15.75
K	1.40	1.68
L	0.00	0.25
M	2.49	2.74
N	0.43	0.58
P	2.29	2.79
R	0°	8°
S	2.41	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(P) Ultra Thin-Pak™
7-Pin

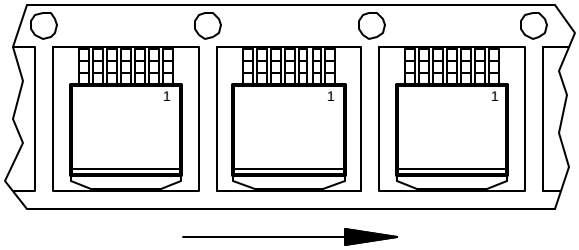


SYMBOL	MIN	MAX
A	9.27	9.52
A1	8.89	9.14
B	7.87	8.13
C	1.78	2.03
D	0.63	0.79
E	0.25 NOM	
G	1.27	
H	10.41	10.67
K	0.76	1.27
L	0.03	0.13
M	0.89	1.14
N	0.25	
P	0.79	1.04
R	3°	6°
U	5.59 NOM	
V	7.49 NOM	

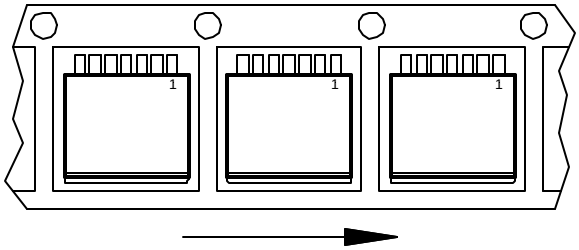
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
M	TO-263	7	50	750	Fig A
P	Ultra Thin-Pak™	7	75	2500	Fig B



Feed Direction
Figure A



Feed Direction
Figure B

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IRU1261

DUAL 6A AND 1A LOW DROPOUT POSITIVE FIXED 1.5V AND 2.5V REGULATOR

FEATURES

- Guaranteed to Provide 1.5V and 2.5V Supplies with 3.1V Input
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown

APPLICATIONS

- Pentium II™ Processor Applications

DESCRIPTION

The IRU1261, using a proprietary process, combines a dual low dropout regulator with fixed outputs of 1.5V and 2.5V in a single package with the 1.5V output having a minimum of 6A and the 2.5V having a 1A output current capability. This product is specifically designed to provide well regulated supplies from 3.3V to generate 1.5V for GTL+ termination resistor supply and 2.5V clock supply for the new generation of the Pentium II™ processor applications.

TYPICAL APPLICATION

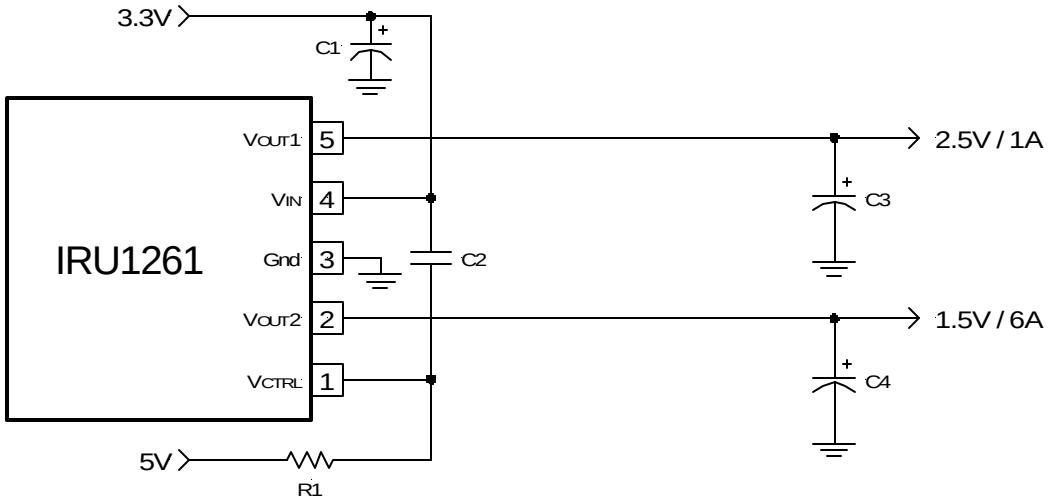


Figure 1 - Typical application of IRU1261 in a Pentium II™ processor application.

Note: Pentium II™ is trademark of Intel Corp.

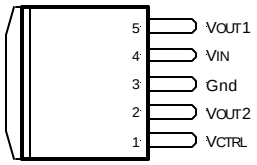
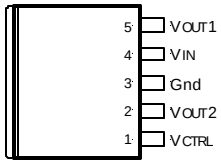
PACKAGE ORDER INFORMATION

T_J (°C)	5-PIN PLASTIC TO-263 (M)	5-PIN PLASTIC Ultra Thin-Pak™ (P)
0 To 150	IRU1261CM	IRU1261CP

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 7V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

5-PIN PLASTIC TO-263 (M)	5-PIN ULTRA THIN-PAK™ (P)
	
θ_{JA}=30°C/W for 1"sq pad	θ_{JA}=30°C/W for 1"sq pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=1µF, C_{OUT}=100µF and T_J=0 to 150°C. Typical values refer to T_J=25°C. I_{FL}=6A for output #2 and 1A for output #1. V_{CTRL}=5V, V_{IN}=3.3V.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
V_{CTRL} Input Voltage			3.0			V
Output Voltage #2	V_{O2}	Io=10mA, T_J=25°C	1.485	1.500	1.515	V
		Io=10mA	1.470	1.500	1.530	
Output Voltage #1	V_{O1}	Io=10mA, T_J=25°C	2.462	2.500	2.537	V
		Io=10mA	2.425	2.500	2.575	
Line Regulation		Io=10mA, 3.1V<V_{IN}<3.6V		0.2		%
Load Regulation (Note 1)		10mA<Io<I_{FL}		0.4		%
Dropout Voltage (Output #2)		Note 2, Io=6A, V_{CTRL}=4.75V			1.3	V
Dropout Voltage (Output #1)		Note 2, Io=1A, V_{CTRL}=4.75V		0.4	0.6	V
Current Limit (Output #2)		ΔVo=100mV	6.1			A
Current Limit (Output #1)		ΔVo=100mV	1.1			A
Minimum Load Current		Note 3		5	10	mA
Thermal Regulation		30ms Pulse, Io=I_{FL}		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25µF Tantalum, Io=0.5 × I_{FL}		70		dB
Temperature Stability		Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3		%
RMS Output Noise		10Hz<f<10KHz		0.003		%V_O

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor dividers are selected such that it automatically maintains this current.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	V_{CTRL}	The control input pin of the regulator. This pin is connected, via a 10Ω resistor, to the 5V supply to provide the base current for the pass transistor of both regulators. This allows the regulator to have very low dropout voltage which allows one to generate a well regulated 2.5V supply from the 3.3V input. A high frequency, 1µF capacitor is connected between this pin and V_{IN} pin to insure stability.
2	$V_{OUT}2$	The output #2 (high current) of the regulator. A minimum of 100µF capacitor must be connected from this pin to ground to insure stability.
3	Gnd	This pin is connected to ground. It is also the Tab of the package.
4	V_{IN}	The power input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be higher than both V_{OUT} pins by the amount of the dropout voltage (see data sheet) in order for the device to regulate properly.
5	$V_{OUT}1$	The output #1 (low current) of the regulator. A minimum of 100µF capacitor must be connected from this pin to ground to insure stability.

BLOCK DIAGRAM

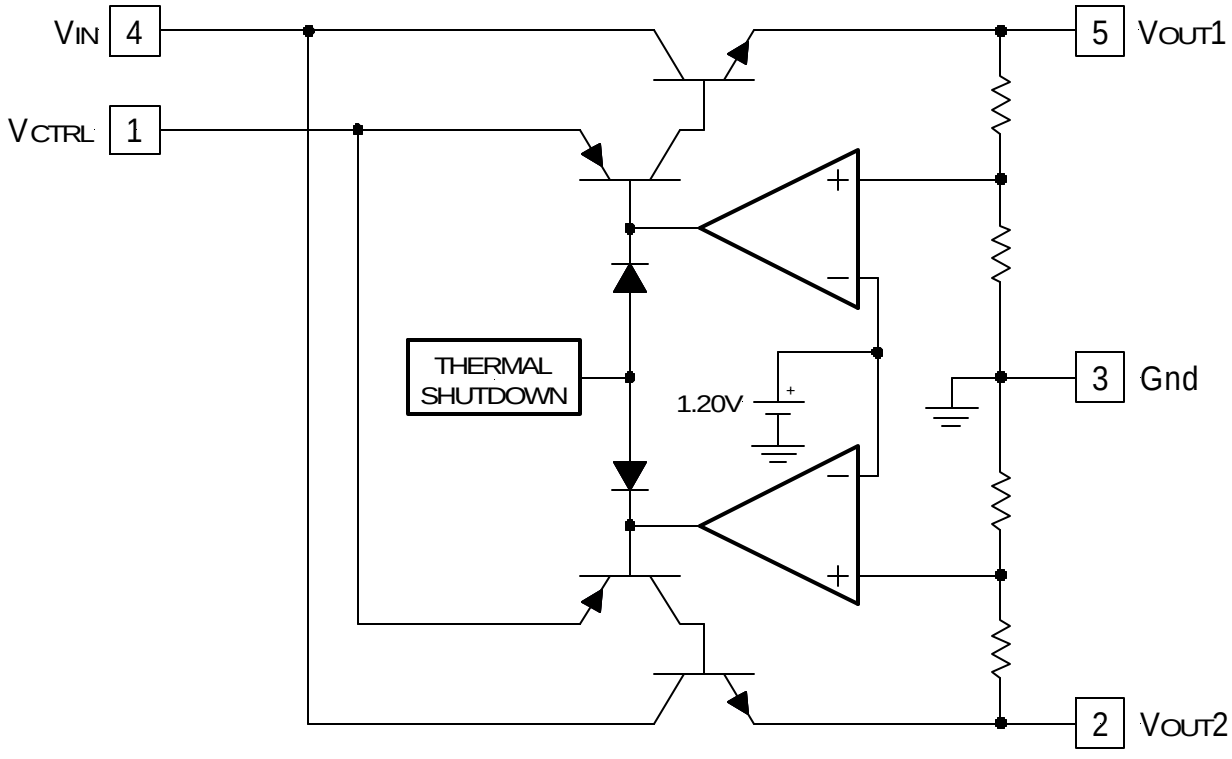


Figure 2 - Simplified block diagram of the IRU1261.

APPLICATION INFORMATION

Introduction

The IRU1261 is a dual fixed output Low Dropout (LDO) regulator available in a TO-263 package. This voltage regulator is designed specifically for Pentium II processor applications requiring 2.5V and 1.5V supplies, eliminating the need for a second regulator resulting in lower overall system cost. The IRU1261 is designed to take advantage of 5V supply to provide the drive for the pass transistor, allowing 2.5V supply to be generated from 3.3V input. This feature improves the power dissipation of the 2.5V regulator substantially allowing a smaller heat sink to be used for the application. Compared to the IRU1260 dual adjustable regulator, the IRU1261 includes the resistor dividers that are otherwise needed with the IRU1260, eliminating four external components and their tolerances, resulting in a more accurate initial accuracy for each output voltage. Other features of the device include: fast response to sudden load current changes, such as GTL+ termination application and thermal shutdown protection to protect the device if an overload condition occurs.

Stability

The IRU1261 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for the microprocessor applications use standard electrolytic capacitors with typical ESR in the range of 50 to 100mΩ and the output capacitance of 500 to 1000μF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1261 takes advantage of this phenomena in making the overall regulator loop stable. For most applications a minimum of 100μF aluminum electrolytic capacitor with the maximum ESR of 0.3Ω such as Sanyo, MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response. The IRU1261 also requires a 1μF ceramic capacitor connected from V_{IN} to V_{CTRL} and a 10Ω, 0.1W resistor in series with V_{CTRL} pin in order to further insure stability.

Thermal Design

The IRU1261 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the maximum allowable junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. The example given shows the steps in selecting the proper regulator heat sink for driving the Pentium II processor GTL+ termination resistors and the Clock IC using IRU1261 in TO-263 package.

Example**:**

Assuming the following specifications:

V_{IN} = 3.3V
V_{OUT1} = 2.5V
V_{OUT2} = 1.5V
$I_{OUT1(MAX)}$ = 0.2A
$I_{OUT2(MAX)}$ = 1.5A
T_A = 35°C

The steps for selecting a proper heat sink to keep the junction temperature below 135°C is given as:

1) Calculate the maximum power dissipation using:

$$P_D = I_{OUT1} \times (V_{IN} - V_{OUT1}) + I_{OUT2} \times (V_{IN} - V_{OUT2})$$

$$P_D = 0.2 \times (3.3 - 2.5) + 1.5 \times (3.3 - 1.5) = 2.86W$$

2) Assuming a TO-263 surface mount package, the junction to ambient thermal resistance of the package is:

θ_{JA} = 30°C/W for 1" square pad area

3) The maximum junction temperature of the device is calculated using the equation below:

$$T_J = T_A + P_D \times \theta_{JA}$$

$$T_J = 35 + 2.86 \times 30 = 121°C$$

Since this is lower than our selected 135°C maximum junction temperature (150°C is the thermal shutdown of the device), TO-263 package is a suitable package for our application.

Layout Consideration

The IRU1261 like all other high speed linear regulators need to be properly laid out to insure stable operation. The most important component is the output capacitor, which needs to be placed close to the output pin and connected to this pin using a plane connection with a low inductance path.

TYPICAL APPLICATION

PENTIUM II ã APPLICATION

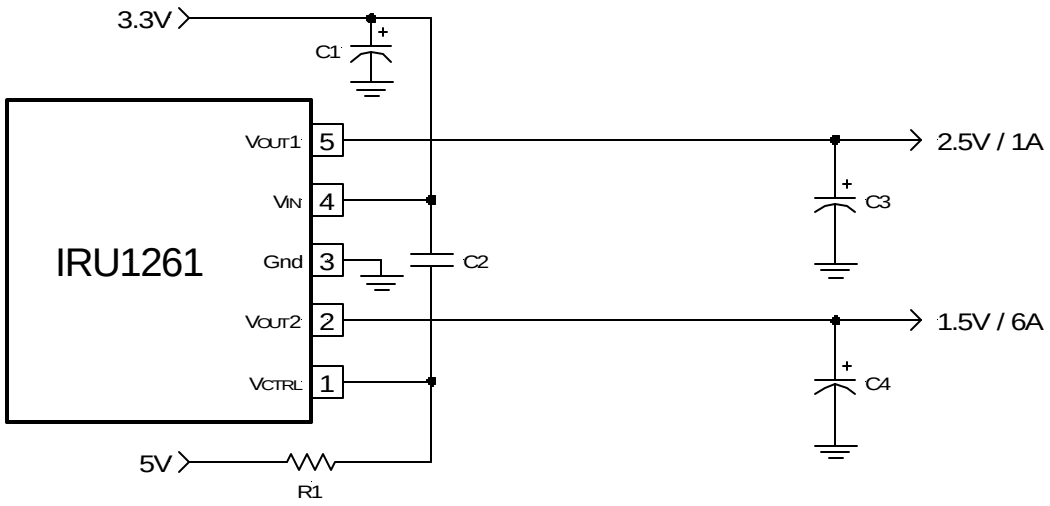


Figure 3 - Typical application of IRU1261 in the Pentium II™ design with the 1.5V output providing for GTL+ termination while 2.5V supplies the clock chip.

Note: Pentium II™ is trademark of Intel Corp.

Ref Desig	Description	Qty	Part #	Manuf
U1	Dual LDO Regulator	1	IRU1261CM	IR
C1, C4	Capacitor	2	Elect, 680µF, EEUFA1A681L	Panasonic
C3	Capacitor	1	Elect, 220µF, 6.3V, ECAOJFQ221	Panasonic
C2	Capacitor	1	Ceramic, 1µF, 16V, Z5U	
R1	Resistor	1	3Ω, 0.1W, 0805 SMT	Panasonic
HS1	Heat Sink	1) Use 1" Square Copper Pad area if I_{OUT2}<1.7A and I_{OUT1}<0.2A. 2) For I_{OUT2}<3A and I_{OUT1}<0.5A, use IRU1261CT and Thermalloy 6030B 3) For I_{OUT2}<5.4A and I_{OUT1}<0.5A, use IRU1261CT and Thermalloy 7021B		

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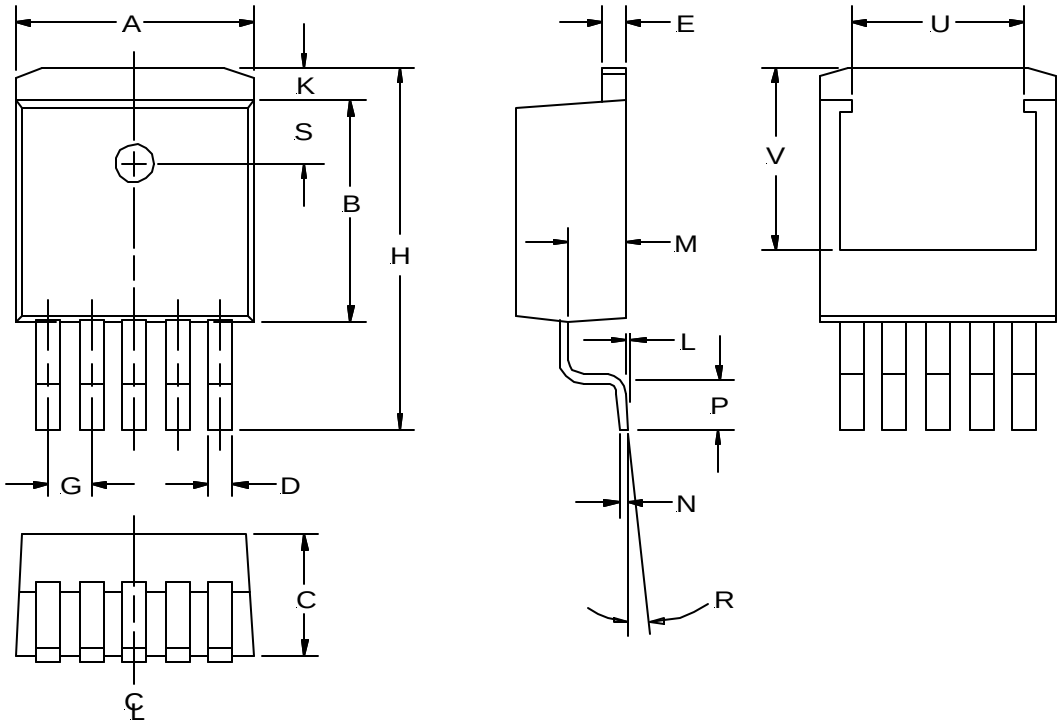
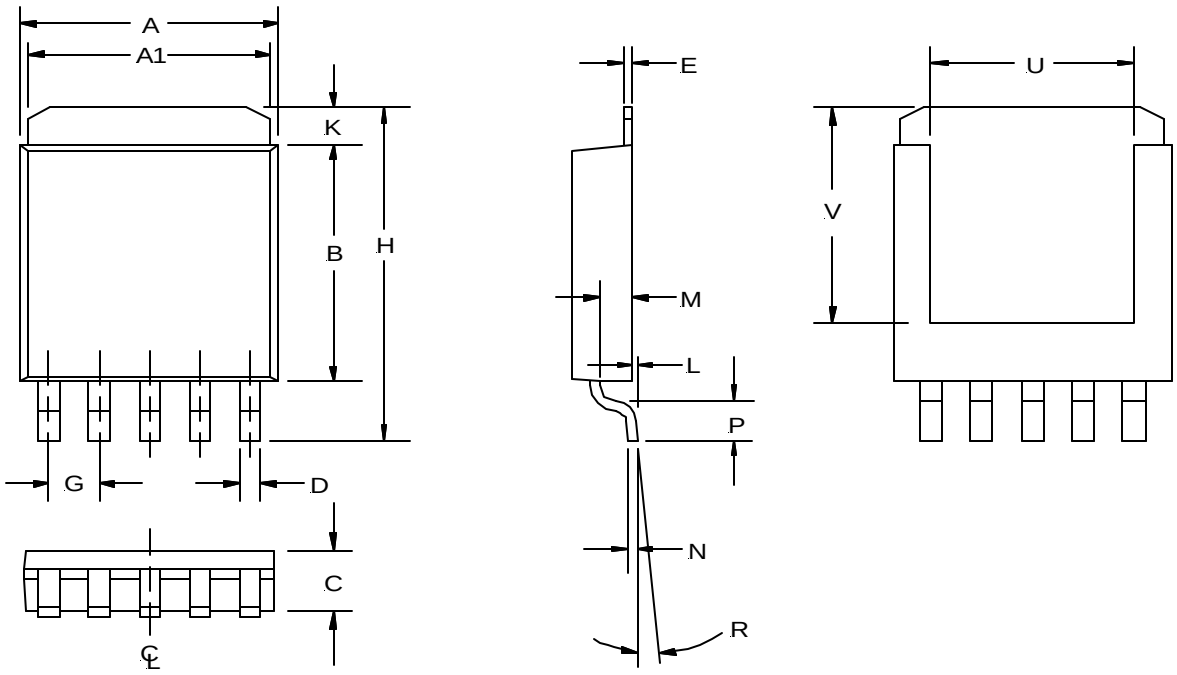
(M) TO-263 Package
5-Pin



SYMBOL	MIN	MAX
A	10.05	10.668
B	8.28	9.169
C	4.31	4.597
D	0.66	0.91
E	1.14	1.40
G	1.575	1.829
H	14.605	15.875
K	1.143	1.68
L	0.00	0.305
M	2.49	2.74
N	0.33	0.58
P	2.286	2.794
R	0°	8°
S	1.143	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(P) Ultra Thin-Pak™
5-Pin

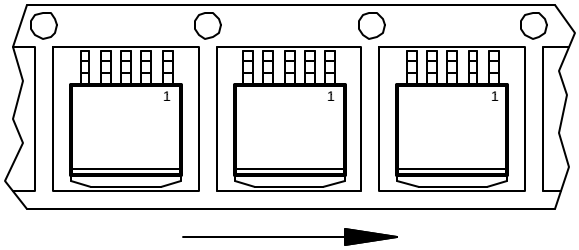


SYMBOL	MIN	MAX
A	9.27	9.52
A1	8.89	9.14
B	7.87	8.13
C	1.78	2.03
D	0.63	0.79
E	0.25 NOM	
G	1.72	
H	10.41	10.67
K	0.76	1.27
L	0.03	0.13
M	0.89	1.14
N	0.25	
P	0.79	1.04
R	3°	6°
U	5.59 NOM	
V	7.49 NOM	

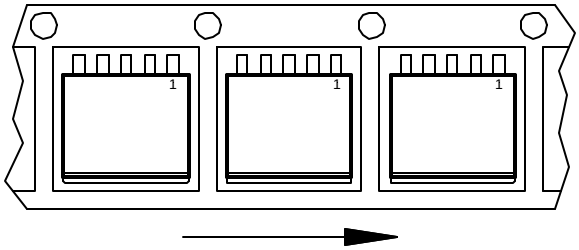
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
M	TO-263	5	50	750	Fig A
P	Ultra Thin-Pak™	5	75	2500	Fig B



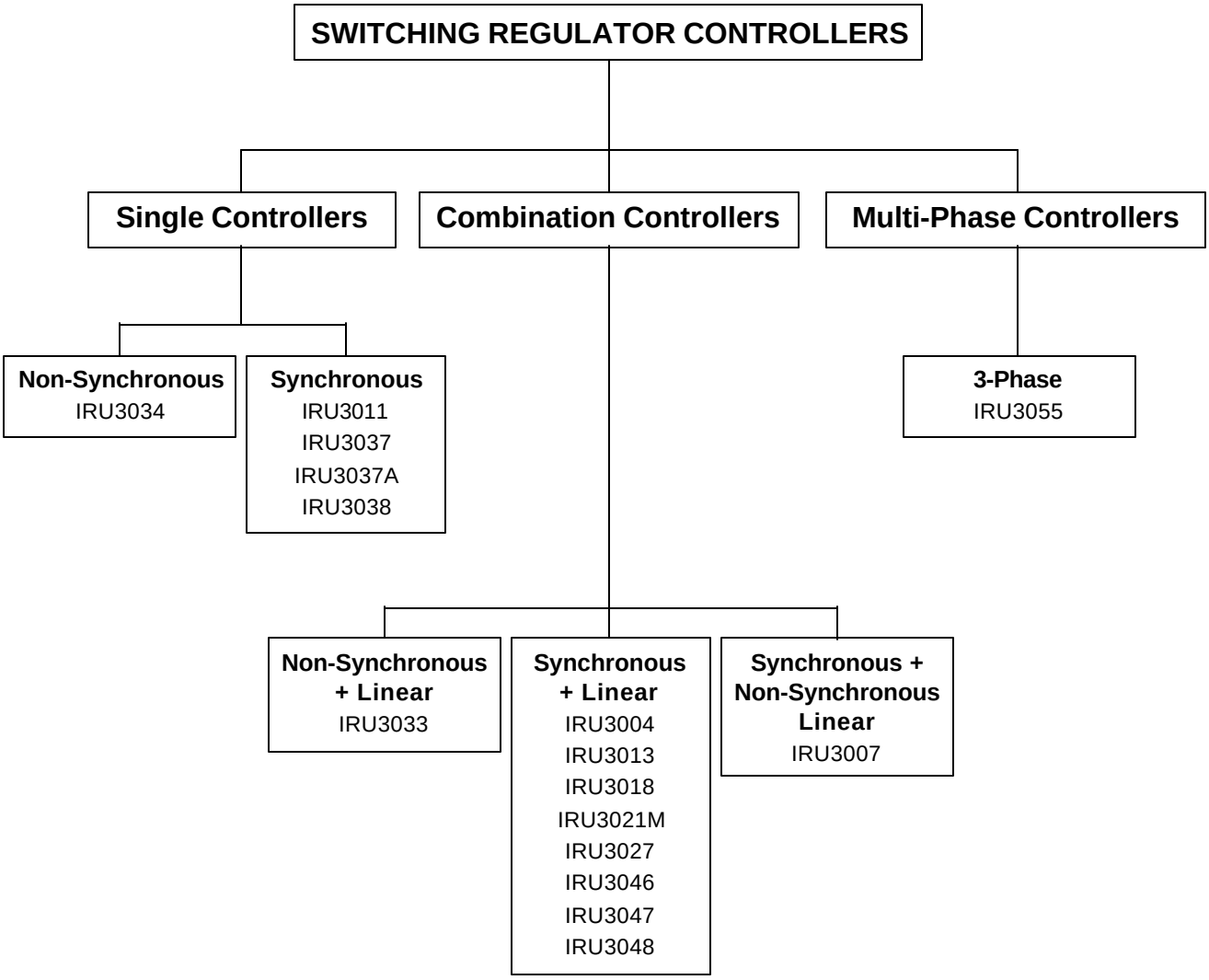
Feed Direction
Figure A



Feed Direction
Figure B

Section 4: Switching Regulator Controllers

Selection Tree



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5-BIT PROGRAMMABLE SYNCHRONOUS BUCK CONTROLLER IC WITH DUAL LDO CONTROLLER

FEATURES

- Meets latest VRM 8.4 specification for PentiumIII
- Provides single chip solution for Vcore, GTL+ and clock supply
- On-Board DAC programs the output voltage from 1.3V to 3.5V. The IRU3004 remains on for VID code of (11111)
- Dual linear regulator controller on-board for 1.5V GTL+ and 2.5V clock supplies
- Loss-less Short Circuit Protection
- Synchronous operation allows maximum efficiency
- Patented architecture allows fixed frequency operation as well as 100% duty cycle during dynamic load
- Minimum Part Count, No External Compensation
- Soft-Start Function
- High current totem pole driver for direct driving of the external power MOSFET
- Power Good Function

APPLICATIONS

- Pentium III & next generation processor DC to DC converter application
- Low Cost Pentium with AGP

DESCRIPTION

The IRU3004 controller IC is specifically designed to meet Intel specifications for Pentium III™ microprocessor applications as well as the next generation P6 family processors. The IC provides a single chip controller IC for the Vcore, GTL+ and clock supplies required for the Pentium III applications. The IRU3004 features a patented topology, that in combination with a few external components as shown in the typical application circuit, will provide in excess of 20A of output current for an on-board DC-DC converter while automatically providing the right output voltage via the 5-bit internal DAC meeting the latest VRM specification. The IRU3004 also features loss-less current sensing by using the $R_{DS(on)}$ of the high side power MOSFET as the sensing resistor and a Power Good window comparator that switches its open collector output low when the output is outside of a ±10% window. Other features of the device are: under-voltage lockout for both 5V and 12V supplies, an external programmable soft-start function as well as programming the oscillator frequency by using an external capacitor.

TYPICAL APPLICATION

Note: Pentium III is trademark of Intel Corp.

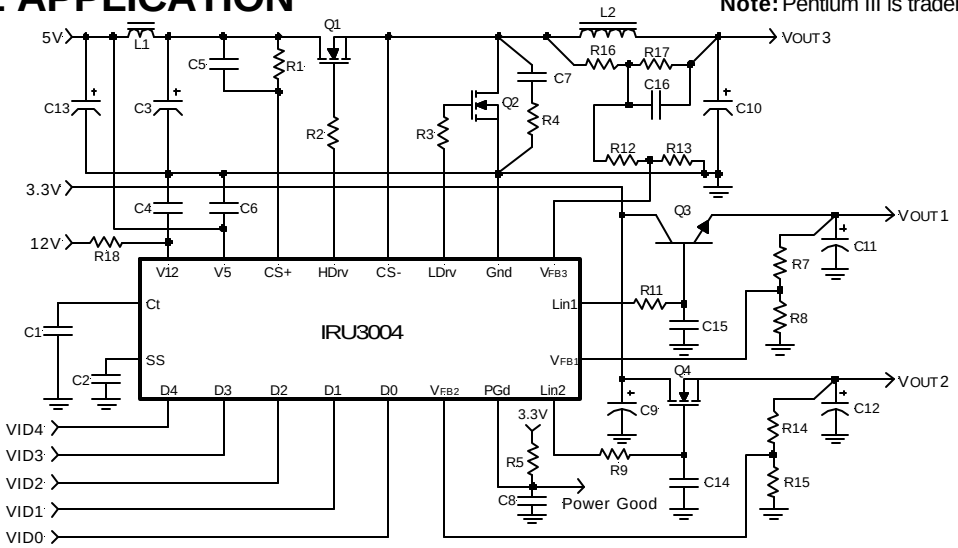


Figure 1 - Typical application of the IRU3004.

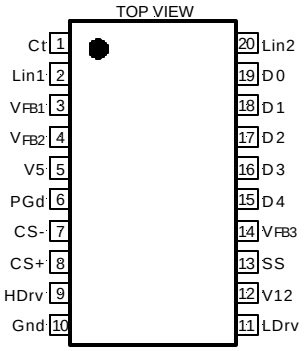
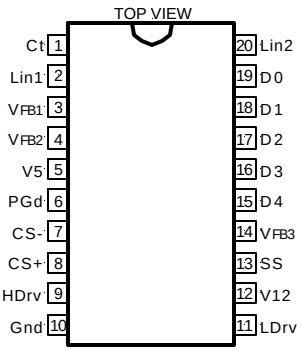
PACKAGE ORDER INFORMATION

T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3004CF	20-Pin Plastic TSSOP (F)
0 To 70	IRU3004CW	20-Pin Plastic SOIC (W)

ABSOLUTE MAXIMUM RATINGS

V5 Supply Voltage 10V
V12 Supply Voltage 20V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

20-PIN PLASTIC TSSOP (F)	20-PIN WIDE BODY PLASTIC SOIC (W)
	
θ_{JA} =90°C/W	θ_{JA} =85°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V12=12V, V5=5V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
VID Section						
DAC Output Voltage (Note 1)			0.98Vs	Vs	1.02Vs	V
DAC Output Line Regulation					0.1	%
DAC Output Temp Variation					0.5	%
VID Input LO					0.4	V
VID Input HI			2			V
VID Input Internal Pull-Up Resistor to V5				27		KΩ
Power Good Section						
Under-Voltage lower trip point		V_{OUT} Ramping Down	0.89Vs	0.90Vs	0.91Vs	V
Under-Voltage upper trip point		V_{OUT} Ramping Up		0.92Vs		V
UV Hysteresis			0.015Vs	0.02Vs	0.025Vs	V
Over-Voltage upper trip point		V_{OUT} Ramping Up	1.09Vs	1.10Vs	1.11Vs	V
Over-Voltage lower trip point		V_{OUT} Ramping Down		1.08Vs		V
OV Hysteresis			0.015Vs	0.02Vs	0.025Vs	V
Power Good Output LO		R_L=3mA			0.4	V
Power Good Output HI		R_L=5K Pull-Up to 5V	4.8			V
Soft-Start Section						
Soft-Start Current		CS+=0V, CS-=5V		10		μA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
UVLO Section						
UVLO Threshold-12V		Supply Ramping Up	9.2	10	10.8	V
UVLO Hysteresis-12V			0.3	0.4	0.5	V
UVLO Threshold-5V		Supply Ramping Up	4.1	4.3	4.5	V
UVLO Hysteresis-5V			0.2	0.3	0.4	V
Error Comparator Section						
Input Bias Current					2	µA
Input Offset Voltage			-2		+2	mV
Delay to Output		V_{DIFF}=10mV			100	ns
Current Limit Section						
CS Threshold Set Current			160	200	240	µA
CS Comp Offset Voltage			-5		+5	mV
Hiccup Duty Cycle		Css=0.1µF			2	%
Supply Current						
Operating Supply Current		C_L=3000pF: V5 V12		 20 14		 mA
Output Drivers Section						
Rise Time		C_L=3000pF		70	100	ns
Fall Time		C_L=3000pF		70	130	ns
Dead Band Time		C_L=3000pF	100	200	300	ns
Oscillator Section						
Osc Frequency		Ct=150pF	160	220	260	KHz
Osc Valley					0.2	V
Osc Peak				V5		V
LDO Controller Section						
V_{FB1} & V_{FB2}			1.455	1.500	1.545	V
Input Bias Current					2	µA
Lin1 or Lin2 Drive Current				50		mA

Note 1: Vs refers to the set point voltage given in Table 1.

D4	D3	D2	D1	D0	Vs
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05

D4	D3	D2	D1	D0	Vs
1	1	1	1	1	2.0
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

Table 1 - Set point voltage vs. VID codes.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Ct	This pin programs the oscillator frequency in the range of 50KHz to 500KHz with an external capacitor connected from this pin to the ground.
2	Lin1	This pin controls the gate of an external transistor for either the GTL+ linear regulator or Clock supply.
3	V_{FB1}	This pin provides the feedback for the linear regulator that its output drive is Lin1 pin.
4	V_{FB2}	This pin provides the feedback for the linear regulator that its output drive is Lin2 pin.
5	V5	5V supply voltage.
6	PGd	This pin is an open collector output that switches LO when the output of the converter is not within ±10% (typical) of the nominal output voltage. When Power Good pin switches LO the sat voltage is less than 0.4V at 3mA.
7	CS-	This pin is connected to the Source of the power MOSFET for the Core supply and it provides the negative sensing for the internal current sensing circuitry.
8	CS+	This pin is connected to the Drain of the power MOSFET of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the CS threshold depending on the R_{DS} of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.
9	HDrv	Output driver for the high-side power MOSFET.
10	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane. A high frequency capacitor (0.1 to 1μF) must be connected from V5 and V12 pins to this pin for noise free operation.
11	LDrv	Output driver for the synchronous power MOSFET.
12	V12	This pin is connected to the 12 V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (0.1 to 1μF) must be connected directly from this pin to ground pin in order to supply the peak current to the power MOSFET duringthe transitions.
13	SS	This pin provides the soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to the ground which ramps up the outputs of the switching regulator, preventing the outputs from overshooting as well as limiting the input current. The second function of the Soft-Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting.
14	V_{FB3}	This pin is connected directly to the output of the Core supply to provide feedback to the Error comparator.
15	D4	This pin selects a range of output voltages for the DAC. When in the LOW state the range is 1.3V to 2.05V. For VID codes of all "1" the IRU3004 keeps all the outputs on.
16	D3	MSB input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10K resistor to either 3.3V or 5V supply.
17	D2	Input to the DAC that programs the output voltage. This pin can be pulled up externally by a 10K resistor to either 3.3V or 5V supply.
18	D1	Input to the DAC that programs the output voltage. This pin can be pulled up externally by a 10KΩ resistor to either 3.3V or 5V supply.
19	D0	LSB input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10K resistor to either 3.3V or 5V supply.
20	Lin2	This pin controls the gate of an external transistor for either the GTL+ linear regulator or Clock supply.

BLOCK DIAGRAM

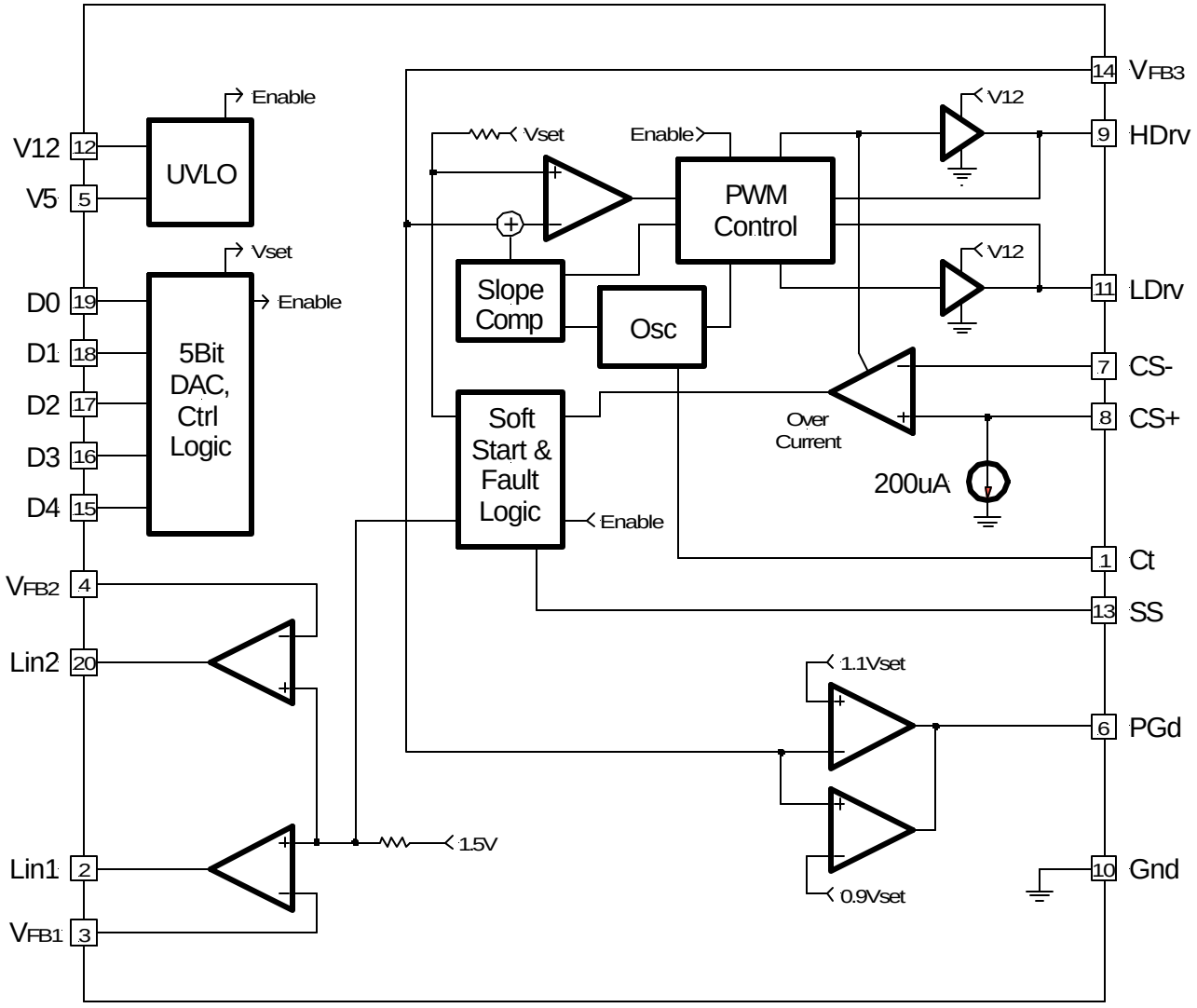


Figure 2 - Simplified block diagram of the IRU3004.

TYPICAL APPLICATION

Pentium III

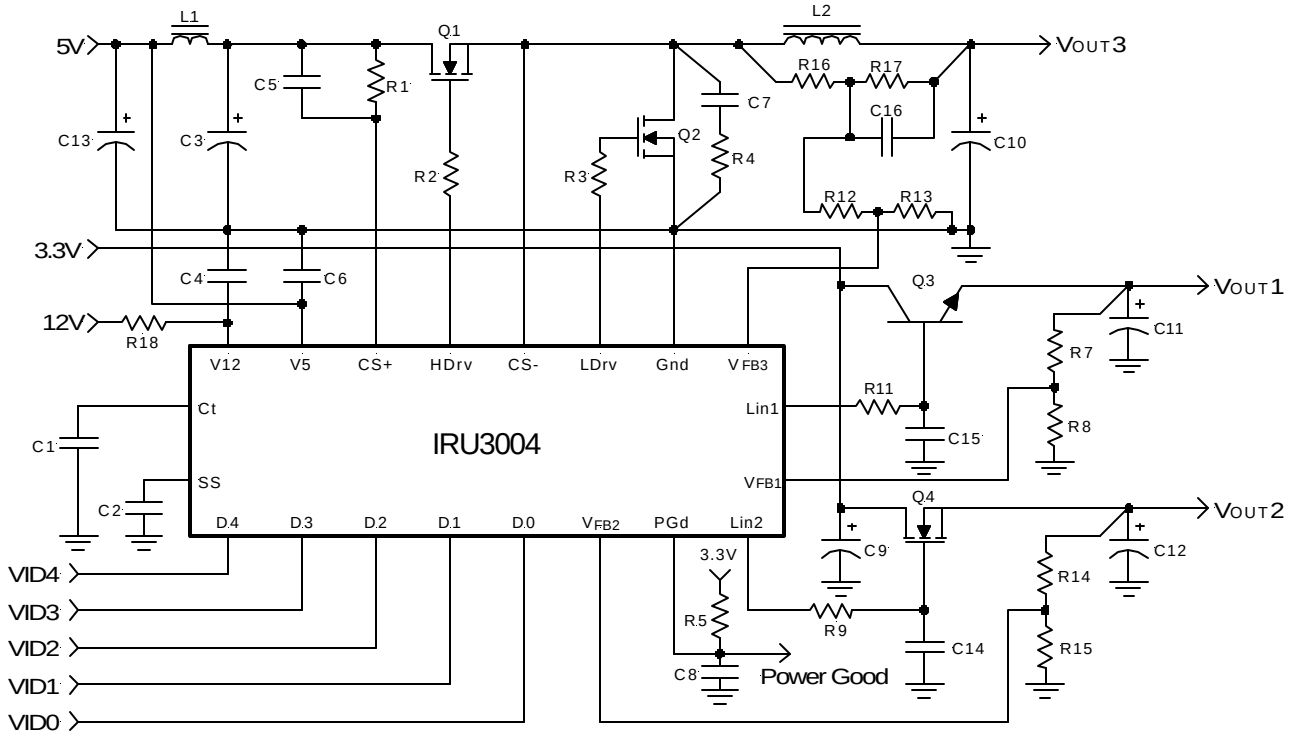


Figure 3 - Typical application of IRU3004 in an on-board DC-DC converter providing the Core, GTL+, and Clock supplies for the Pentium II microprocessor.

IRU3004 APPLICATION PARTS LIST

Ref Desig	Description	Qty	Part #	Manuf
Q1	MOSFET	1	IRL3103S, TO-263 package	IR
Q2	MOSFET	1	IRL3103D1S, TO-263 package	IR
Q3	Bipolar Trans, GP	1	MPS2222A, SOT-23 package	Motorola
Q4	MOSFET	1	IRLR024, TO-252 package	IR
L1	Inductor	1	L=1μH, 5052 core with 4 turns of 1.0mm wire	MicroMetal
L2	Inductor	1	L=2.7μH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1	Capacitor, Ceramic	1	150pF, 0603	
C2, 6	Capacitor, Ceramic	2	1μF, 0603	
C3	Capacitor, Electrolytic	2	10MV1200GX, 1200μF,10V	Sanyo
C4	Capacitor, Ceramic	1	1μF, 0805	
C5	Capacitor, Ceramic	1	220pF, 0603	
C7, 14, 15	Capacitor, Ceramic	3	1000pF, 0603	
C8	Capacitor, Ceramic	1	0.1μF, 0603	
C9	Capacitor, Electrolytic	1	6MV1000GX, 1000μF, 6.3V	Sanyo
C10	Capacitor, Electrolytic	6	6MV1500GX, 1500μF, 6.3V	Sanyo
C11	Capacitor, Electrolytic	1	6MV150GX, 150μF, 6.3V	Sanyo
C12	Capacitor, Electrolytic	1	6MV1000GX, 1000μF, 6.3V	Sanyo
C13	Capacitor, Electrolytic	1	10MV470GX, 470μF, 10V	Sanyo
C16	Capacitor, Ceramic	1	4.7μF, 1206	
R1	Resistor	1	3.3KΩ, 5%, 0603	
R2, 3, 4	Resistor	3	4.7Ω, 5%, 1206	
R5, 15	Resistor	2	10KΩ, 5%, 0603	
R7, 12	Resistor	2	100Ω, 1%, 0603	
R8	Resistor	1	150Ω, 1%, 0603	
R9, 11, 14	Resistor	3	100Ω, 5%, 0603	
R13	Resistor	1	22KΩ, 1%, 0603	
R16	Resistor	1	220Ω, 1%, 0603	
R17	Resistor	1	330Ω, 1%, 0603	
R18	Resistor	1	10Ω, 5%, 0603	

Note 1: R16, R17, C16, R12, and R13 set the Vcore 2% higher for level shift to reduce CPU transient voltage.

Note 2: R14 and R15 set the 1.5V approximately 1% higher to account for the trace resistance drop.

TYPICAL APPLICATION

Pentium with AGP

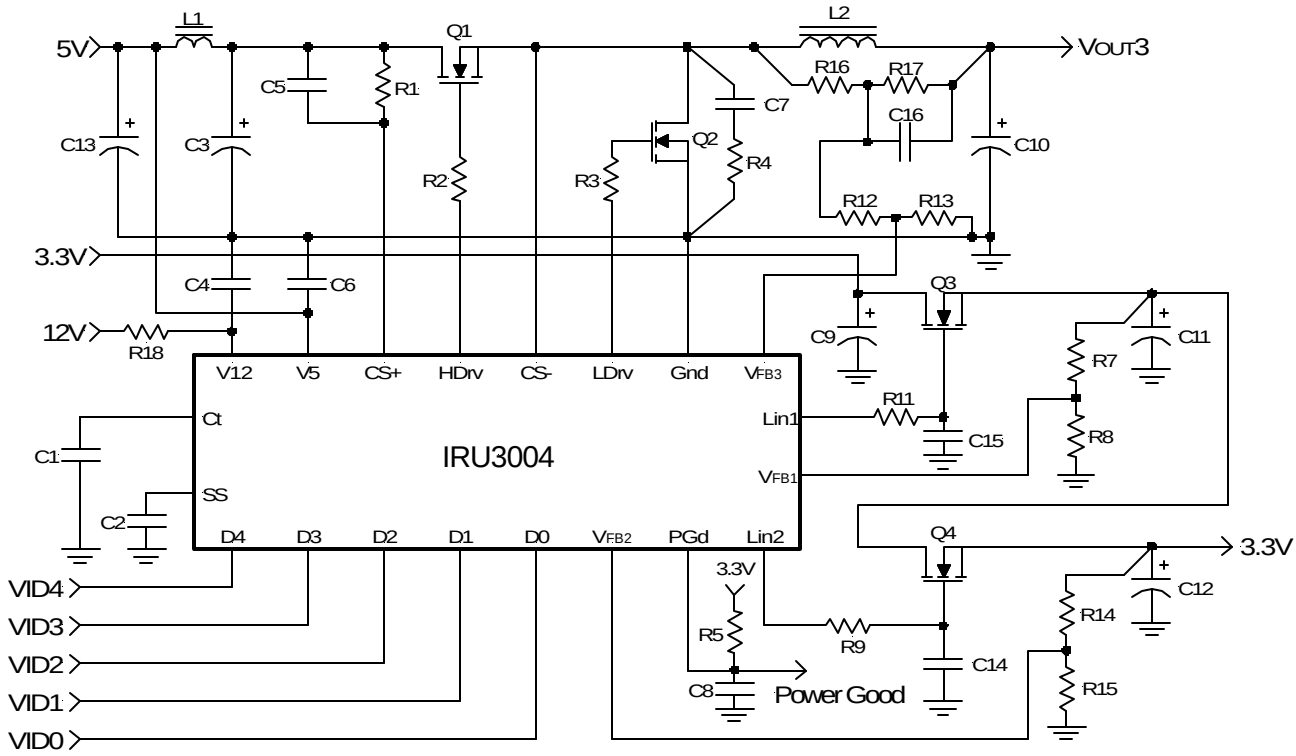


Figure 4 - Typical application of IRU3004 in a Pentium with AGP where the power dissipation of the 3.3V linear regulator is equally distributed between Q3 and Q4 pass transistors. This equal distribution is possible by accurately regulating the first regulator using the IRU3004 linear controller and its internal 1% reference voltage while the second controller regulates the output of the first regulator from 4.17V to 3.3V, thereby distributing the power dissipation equally.

IRU3004 APPLICATION PARTS LIST

Ref Desig	Description	Qty	Part #	Manuf
Q1	MOSFET	1	IRL3103s, TO-263 package	IR
Q2	MOSFET	1	IRL3103D1S, TO-263 package	IR
Q3, 4	MOSFET	2	IRL3303S, TO-263 package	IR
L1	Inductor	1	L=1μH, 5052 core with 4 turns of 1.0mm wire	Micro Metal
L2	Inductor	1	L=2.7μH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1	Capacitor, Ceramic	1	150pF, 0603	
C2, 6	Capacitor, Ceramic	2	1μF, 0603	
C3	Capacitor, Electrolytic	2	10MV1200GX, 1200μF, 10V	Sanyo
C4	Capacitor, Ceramic	1	1μF, 0805	
C5	Capacitor, Ceramic	1	220pF, 0603	
C7, 14, 15	Capacitor, Ceramic	3	1000pF, 0603	
C8	Capacitor, Ceramic	1	0.1μF, 0603	
C9	Capacitor, Electrolytic	1	6MV1000GX, 1000μF, 6.3V	Sanyo
C10	Capacitor, Electrolytic	6	6MV1500GX, 1500μF, 6.3V	Sanyo
C11	Capacitor, Electrolytic	1	6MV150GX, 150μF, 6.3V	Sanyo
C12	Capacitor, Electrolytic	1	6MV1000GX, 1000μF, 6.3V	Sanyo
C13	Capacitor, Electrolytic	1	10MV470GX, 470μF, 10V	Sanyo
C16	Capacitor, Ceramic	1	4.7μF, 1206	
R1	Resistor	1	3.3KΩ, 5%, 0603	
R2, 3, 4	Resistor	3	4.7Ω, 5%, 1206	
R5, 15	Resistor	2	10KΩ, 5%, 0603	
R7	Resistor	1	267Ω, 1%, 0603	
R8	Resistor	2	150Ω, 1%, 0603	
R9, 11, 14	Resistor	3	100Ω, 5%, 0603	
R12	Resistor	1	100Ω, 1%, 0603	
R13	Resistor	1	22KΩ, 1%, 0603	
R16	Resistor	1	220Ω, 1%, 0603	
R17	Resistor	1	330Ω, 1%, 0603	
R18	Resistor	1	10Ω, 5%, 0603	

Note 1: R16, R17, C16, R12, and R13 set the Vcore 2% higher for level shift to reduce CPU transient voltage.

APPLICATION INFORMATION

An example of how to calculate the components for the application circuit is given below.

Assuming, two sets of output conditions that this regulator must meet:

a) Vo=2.8V, Io=14.2A, ΔVo=185mV, ΔIo=14.2A

b) Vo=2V, Io=14.2A, ΔVo=140mV, ΔIo=14.2A

The regulator design will be done such that it meets the worst case requirement of each condition.

Output Capacitor Selection

The first step is to select the output capacitor. This is done primarily by selecting the maximum ESR value that meets the transient voltage budget of the total ΔVo specification. Assuming that the regulators DC initial accuracy plus the output ripple is 2% of the output voltage, then the maximum ESR of the output capacitor is calculated as:

$$ESR \leq \frac{100}{14.2} = 7m\Omega$$

The Sanyo MVGX series is a good choice to achieve both the price and performance goals. The 6MV1500GX, 1500μF, 6.3V has an ESR of less than 36mΩ typical. Selecting 6 of these capacitors in parallel has an ESR of ≈ 6mΩ which achieves our low ESR goal.

Other type of Electrolytic capacitors from other manufacturers to consider are the Panasonic FA series or the Nichicon PL series.

Reducing the Output Capacitors Using Voltage Level Shifting Technique

The trace resistance or an external resistor from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transition from light load to full load and vice versa. To accomplish this, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the Gnd pin of the device is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70mV or 35mV higher than the DAC voltage setting. This intentional voltage level shifting during the load transient eases the requirement for the output capacitor ESR at the cost of load regulation. One can show that the new ESR requirement eases up by half the total trace resistance. For example, if the ESR requirement of the output capacitors without voltage level shifting must be 7mΩ, then after level shifting the new ESR will only need to be 9.5mΩ if the trace resistance is 5mΩ (7 + 5/2=9.5). However, one must be careful that the combined "voltage level shifting" and the transient response is still within the maximum tolerance of the Intel specification. To insure this, the maximum trace resistance must be less than:

$$Rs \leq 2 \times \frac{(Vspec - 0.02 \times Vo - \Delta Vo)}{\Delta I}$$

Where:
Rs = Total maximum trace resistance allowed
Vspec = Intel total voltage specification
Vo = Output voltage
ΔVo = Output ripple voltage
ΔI = load current step

For example, assuming:
Vspec = ±140mV = ±0.1V for 2V output
Vo = 2V
ΔVo = assume 10mV = 0.01V
ΔI = 14.2A

Then the Rs is calculated to be:

$$Rs \leq 2 \times \frac{(0.140 - 0.02 \times 2 - 0.01)}{14.2} = 12.6m\Omega$$

However, if a resistor of this value is used, the maximum power dissipated in the trace (or if an external resistor is being used) must also be considered. For example if Rs=12.6mΩ, the power dissipated is:

$$Io^2 \times Rs = 14.2^2 \times 12.6 = 2.54W$$

This is a lot of power to be dissipated in a system. So, if the Rs=5mΩ, then the power dissipated is about 1W which is much more acceptable. If level shifting is not implemented, then the maximum output capacitor ESR was shown previously to be 7mΩ which translated to ≈ 6 of the 1500μF, 6MV1500GX type Sanyo capacitors. With Rs=5mΩ, the maximum ESR becomes 9.5mΩ which is equivalent to ≈ 4 caps. Another important consideration is that if a trace is being used to implement the resistor, the power dissipated by the trace increases the case temperature of the output capacitors which could seriously effect the life time of the output capacitors.

Output Inductor Selection
The output inductance must be selected such that under low line and the maximum output voltage condition, the inductor current slope times the output capacitor ESR is ramping up faster than the capacitor voltage is drooping during a load current step. However, if the inductor is too small, the output ripple current and ripple voltage become too large. One solution to bring the ripple current down is to increase the switching frequency, however that will be at the cost of reduced efficiency and higher system cost. The following set of formulas are derived to achieve the optimum performance without many design iterations.

The maximum output inductance is calculated using the following equation:

$$L = ESR \times C \times \left(\frac{V_{IN(MIN)} - Vo_{(MAX)}}{2 \times \Delta I}\right)$$

Where:
$V_{IN(MIN)}$ = Minimum input voltage
Vo = 2.8V , ΔI = 14.2A

$$L = 0.006 \times 9000 \times \left(\frac{4.75 - 2.8}{2 \times 14.2}\right) = 3.7\mu H$$

Assuming that the programmed switching frequency is set at 200KHz, an inductor is designed using the Micrometals' powder iron core material. The summary of the design is outlined below:

The selected core material is Powder Iron, the selected core is T50-52D from Micro Metal wound with 8 turns of #16 AWG wire, resulting in 3μH inductance with ≈ 3mΩ of DC resistance.

Assuming L=3μH and Fsw=200KHz (switching frequency), the inductor ripple current and the output ripple voltage is calculated using the following set of equations:

T ≡ Switching Period
D ≡ Duty Cycle
Vsw ≡ High side Mosfet ON Voltage
R_{DS} ≡ Mosfet On Resistance
Vsync ≡ Synchronous MOSFET ON Voltage
ΔIr ≡ Inductor Ripple Current
ΔVo ≡ Output Ripple Voltage

$$T = \frac{1}{Fsw}$$

$$Vsw = Vsync = Io \times R_{DS}$$

$$D \approx \frac{Vo + Vsync}{V_{IN} - Vsw + Vsync}$$

$$T_{ON} = D \times T$$

$$T_{OFF} = T - T_{ON}$$

$$\Delta Ir = (Vo + Vsync) \times \frac{T_{OFF}}{L}$$

$$\Delta Vo = \Delta Ir \times ESR$$

In our example for Vo=2.8V and 14.2A load, assuming IRL3103 MOSFET for both switches with maximum on-resistance of 19mΩ, we have:

$$T = \frac{1}{200000} = 5\mu s$$

$$Vsw = Vsync = 14.2 \times 0.019 = 0.27V$$

$$D \approx \frac{2.8 + 0.27}{5 - 0.27 + 0.27} = 0.61$$

$$T_{ON} = 0.61 \times 5 = 3.1\mu s$$

$$T_{OFF} = 5 - 3.1 = 1.9\mu s$$

$$\Delta Ir = (2.8 + 0.27) \times \frac{1.9}{3} = 1.94A$$

$$\Delta Vo = 1.94 \times 0.006 = 0.011V = 11mV$$

Power Component Selection
Assuming IRL3103 MOSFETs as power components, we will calculate the maximum power dissipation as follows:

For high-side switch the maximum power dissipation happens at maximum Vo and maximum duty cycle.

$$D_{MAX} \approx \frac{(2.8 + 0.27)}{(4.75 - 0.27 + 0.27)} = 0.65$$

$$P_{DH} = D_{MAX} \times Io^2 \times R_{DS(MAX)}$$

$$P_{DH} = 0.65 \times 14.2^2 \times 0.029 = 3.8W$$

$R_{DS(MAX)}$ = Maximum $R_{DS(ON)}$ of the MOSFET (125°C)

For synchronous MOSFET, maximum power dissipation happens at minimum Vo and minimum duty cycle.

$$D_{MIN} \approx \frac{(2 + 0.27)}{(5.25 - 0.27 + 0.27)} = 0.43$$

$$P_{DS} = (1 - D_{MIN}) \times Io^2 \times R_{DS(MAX)}$$

$$P_{DS} = (1 - 0.43) \times 14.2^2 \times 0.029 = 3.33W$$

Heat Sink Selection
Selection of the heat sink is based on the maximum allowable junction temperature of the MOSFETS. Since we previously selected the maximum $R_{DS(on)}$ at 125°C, then we must keep the junction below this temperature. Selecting TO-220 package gives θ_{JC}=1.8°C/W (from the venders' data sheet) and assuming that the selected heat sink is black anodized, the heat-sink-to-case thermal resistance is θ_{CS}=0.05°C/W, the maximum heat sink temperature is then calculated as:

$$T_S = T_J - P_D \times (\theta_{JC} + \theta_{CS})$$

$$T_S = 125 - 3.82 \times (1.8 + 0.05) = 118°C$$

With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance (θ_{SA}) is calculated as follows:

Assuming T_A = 35°C:

$\Delta T = Ts - T_A = 118 - 35 = 83°C$
Temperature Rise Above Ambient

$$\theta_{SA} = \frac{\Delta T}{P_D} = \frac{83}{3.82} = 22°C/W$$

Next, a heat sink with lower θ_{SA} than the one calculated in the previous step must be selected. One way is to simply look at the graphs of the "Heat Sink Temp Rise Above the Ambient" vs. the "Power Dissipation" given in the heat sink manufacturers' catalog and select a heat sink that results in lower temperature rise than the one calculated in previous step. The following heat sinks from AAVID and Thermalloy meet this criteria.

Company	**Part #**
Thermalloy	6078B
AAVID	577002

Following the same procedure for the Schottky diode results in a heat sink with θ_{SA}=25°C/W. Although it is possible to select a slightly smaller heat sink, for simplicity, the same heat sink as the one for the high side MOSFET is also selected for the synchronous MOSFET.

Switcher Current Limit Protection

The PWM controller uses the MOSFET $R_{DS(ON)}$ as the sensing resistor to sense the MOSFET current and compares to a programmed voltage which is set externally via a resistor (Rcs) placed between the drain of the MOSFET and the "CS+" terminal of the IC as shown in the application circuit. For example, if the desired current limit point is set to be 22A and from our previous selection, the maximum MOSFET $R_{DS(ON)}$=19mΩ, then the current sense resistor, Rcs is calculated as:

Where:
I_B = 200µA is the internal current setting of the device

$$Vcs = I_{CL} \times R_{DS} = 22 \times 0.019 = 0.418V$$

$$Rcs = \frac{Vcs}{I_B} = \frac{0.418V}{200\mu A} = 2.1K\Omega$$

Switcher Timing Capacitor Selection

The switching frequency can be programmed using an external timing capacitor. The value of Ct can be approximated using the equation below:

$$Fsw \approx \frac{3.5 \times 10^{-5}}{Ct}$$

Where:
Ct = Timing Capacitor
Fsw = Switching Frequency

If Fsw = 200KHz:

$$Ct \approx \frac{3.5 \times 10^{-5}}{200 \times 10^{3}} = 175pF$$

LDO Power MOSFET Selection

The first step in selecting the power MOSFET for the linear regulators is to select its maximum $R_{DS(ON)}$ based on the input to output Dropout voltage and the maximum load current.

For Vo = 1.5V, V_{IN} = 3.3V and I_L = 2A:

$$R_{DS(max)} = \frac{(V_{IN} - Vo)}{I_L} = \frac{(3.3 - 1.5)}{2} = 0.9\Omega$$

Note that since the MOSFETs $R_{DS(ON)}$ increases with temperature, this number must be divided by ≈ 1.5, in order to find the $R_{DS(on)}$ max at room temperature. The Motorola MTP3055VL has a maximum of 0.18Ω $R_{DS(ON)}$ at room temperature, which meets our requirement.

To select the heat sink for the LDO MOSFET the first step is to calculate the maximum power dissipation of the device and then follow the same procedure as for the switcher.

$$P_D = (V_{IN} - Vo) \times I_L$$

Where:
P_D = Power Dissipation of the Linear Regulator
I_L = Linear Regulator Load Current

For the 1.5V and 2A load:

$$P_D = (3.3 - 1.5) \times 2 = 3.6W$$

Assuming $T_{J(max)}$ = 125°C then:

$$Ts = T_J - P_D \times (\theta_{JC} + \theta_{CS})$$
$$Ts = 125 - 3.6 \times (1.8 + 0.05) = 118°C$$

With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance (θ_{SA}) is calculated as follows:

Assuming T_A = 35°C:

$\Delta T = Ts - T_A = 118 - 35 = 83°C$
Temperature Rise Above Ambient

$$\theta_{SA} = \frac{\Delta T}{P_D} = \frac{83}{3.6} = 23°C/W$$

The same heat sink as the one selected for the switcher MOSFETs is also suitable for the 1.5V regulator. It is also possible to use TO-263 package or even the MTD3055VL in D-Pak if the load current is less than 1.5A. For the 2.5V regulator, since the dropout voltage is only 0.8V and the load current is less than 0.5A, for most applications, the same MOSFET without heat sink or for low cost applications, one can use PN2222A in TO-92 or SOT-23 package.

LDO Regulator Component Selection
Since the internal voltage reference for the linear regulators is set at 1.5V for all devices, there is no need to divide the output voltage for the 1.5V, GTL+ regulator.

For the 2.5V Clock supply, the resistor dividers are selected per following:

$$Vo = \left(1 + \frac{Rt}{R_B}\right) \times V_{REF}$$

Where:
Rt = Top resistor divider
R_B = Bottom resistor divider
Vref = 1.5V typical

Assuming Rt = 100Ω, for Vo = 2.5V:

$$R_B = \frac{Rt}{\left(\frac{Vo}{V_{REF}}\right) - 1} = \frac{100}{\left(\frac{2.5}{1.5}\right) - 1} = 150\Omega$$

For 1.5V output, Rt can be shorted and R_B left open. However, it is recommended to leave the resistor dividers as shown in the typical application circuit so that the output voltage can be adjusted higher to account for the trace resistance in the final board layout.

It is also recommended that an external filter be added on the linear regulators to reduce the amount of the high frequency ripple at the output of the regulators. This can simply be done by the resistor capacitor combination as shown in the application circuit.

Disabling the LDO Regulators
The LDO controllers can easily be disabled by connecting the feedback pins (V_{FB1} and V_{FB2}) to a voltage higher than 1.5V such as 5V for all devices.

Switcher Output Voltage Adjust
As was discussed earlier, the trace resistance from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transitioning from light load to full load and vice versa. To account for the DC drop, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the Gnd pin of the part is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70mV or 35mV higher than the DAC voltage setting. To do this, the top resistor of the resistor divider (R12 in the application circuit) is set at 100Ω, and the R13 is calculated.

For example, if DAC voltage setting is for 2.8V and the desired output under light load is 2.835V, then R13 is calculated using the following formula:

$$R13 = 100 \times \left(\frac{V_{DAC}}{(Vo - 1.004 \times V_{DAC})}\right) \quad (\Omega)$$

$$R13 = 100 \times \left(\frac{2.8}{(2.835 - 1.004 \times 2.800)}\right) = 11.76K\Omega$$

Select 11.8KΩ, 1%

Note: The value of the top resistor must not exceed 100Ω. The bottom resistor can then be adjusted to raise the output voltage.

Soft-Start Capacitor Selection
The soft-start capacitor must be selected such that during the start up, when the output capacitors are charging up, the peak inductor current does not reach the current limit threshold. A minimum of 1μF capacitor insures this for most applications. An internal 10μA current source charges the soft-start capacitor which slowly ramps up the inverting input of the PWM comparator V_{FB3}. This insures the output voltage to ramp at the same rate as the soft-start cap thereby limiting the input current. For example, with 1μF and the 10μA internal current source the ramp up rate is (ΔV/Δt)=(I/C)=1V/100ms. Assuming that the output capacitance is 9000μF, the maximum start up current will be:

$I = 9000\mu F \times (1V / 100ms) = 0.09A$

Input Filter
It is recommended to place an inductor between the system 5V supply and the input capacitors of the switching regulator to isolate the 5V supply from the switching noise that occurs during the turn on and off of the switching components. Typically an inductor in the range of 1 to 3μH will be sufficient in this type of application.

Switcher External Shutdown
The best way to shutdown the switcher is to pull down on the soft-start pin using an external small signal transistor such as 2N3904 or 2N7002 small signal MOSFET. This allows slow ramp up of the output, the same as the power up.

Layout Considerations
Switching regulators require careful attention to the layout of the components, specifically power components since they switch large currents. These switching components can create large amount of voltage spikes and high frequency harmonics if some of the critical components are far away from each other and are connected with inductive traces. The following is a guideline of how to place the critical components and the connections between them in order to minimize the above issues.

Start the layout by first placing the power components:

1) Place the input capacitors C3 and the high side MOSFET, Q1 as close to each other as possible.

2) Place the synchronous MOSFET, Q2 and the Q1 as close to each other as possible with the intention that the source of Q1 and drain of the Q2 has the shortest length.

3) Place the snubber R4 & C7 between Q1 & Q2.

4) Place the output inductor, L2 and the output capacitors, C10 between the MOSFET and the load with output capacitors distributed along the slot 1 and close to it.

5) Place the bypass capacitors, C4 and C6 right next to 12V and 5V pins. C4 next to the 12V, pin 12 and C6 next to the 5V, pin 5.

6) Place the controller IC such that the PWM output drives, pins 9 and 11 are relatively short distance from gates of Q1 and Q2.

7) Place resistor dividers, R7 & R8 close to pin 3, R12 & R13 (see note) close to pin 14 and R14 and R15 (see note) close to pin 20.

Note: Although, the PWM controller does not require R12-15 resistors, and the feedback pins 3 and 14 can be directly connected to their respective outputs, they can be used to set the outputs slightly higher to account for any output drop at the load due to the trace resistance.

8) Place R11, C15, Q3 and C11 close to each other and do the same with R9, C14, Q4 and C12.

Note: It is better to place the linear regulator components close to the IC and then run a trace from the output of each regulator to its respective load such as 2.5V to the clock and 1.5V for GTL + termination. However, if this is not possible then the trace from the linear drive output pins, pins 2 and 20 must be routed away from any high frequency data signals. It is critical, to place high frequency ceramic capacitors close to the clock chip and termination resistors to provide local bypassing.

9) Place timing capacitor C1 close to pin 1 and soft start capacitor C2 close to pin 13.

Component connections:
Note: It is extremely important that no data bus should be passing through the switching regulator section specifically close to the fast transition nodes such as PWM drives or the inductor voltage.

Using the 4 layer board, dedicate on layer to ground, another layer as the power layer for the 5V, 3.3V, Vcore, 1.5V and if it is possible for the 2.5V. Connect all grounds to the ground plane using direct vias to the ground plane. Use large low inductance/low impedance plane to connect the following connections either using component side or the solder side:

a) C3 to Q1 Drain
b) Q1 Source to Q2 Drain
c) Q2 drain to L2
d) L2 to the output capacitors, C10
e) C10 to the slot 1
f) Input filter L1 to the C3
g) C9 to Q4 drain
h) C12 to the Q4 source

Connect the rest of the components using the shortest connection possible.

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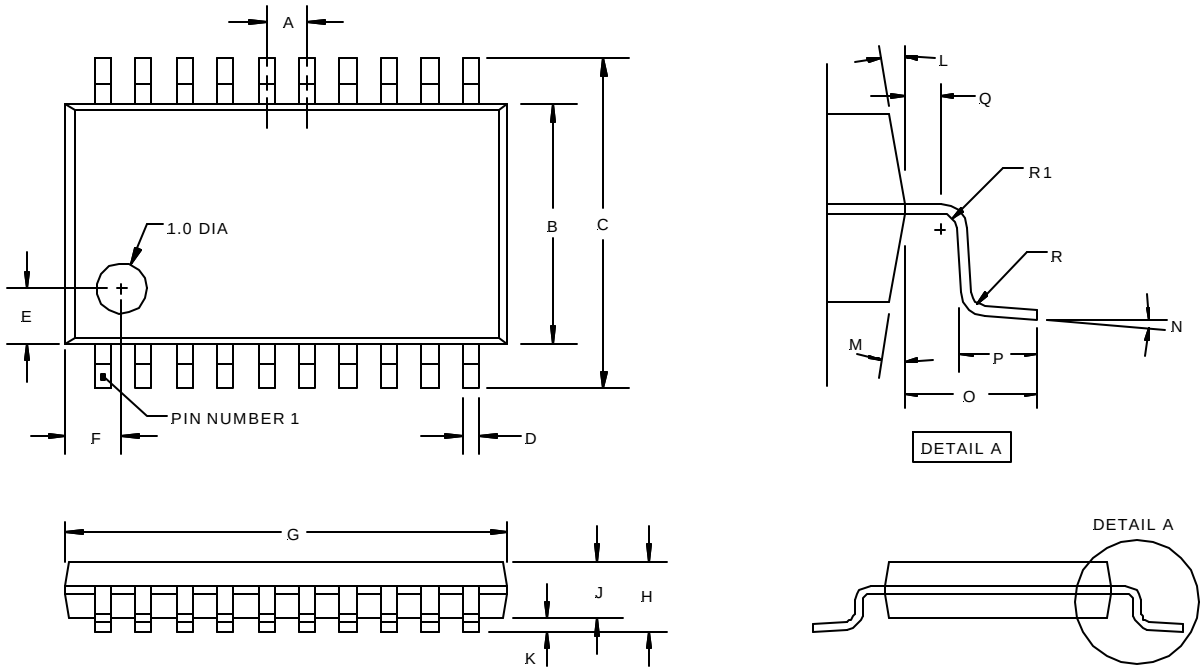
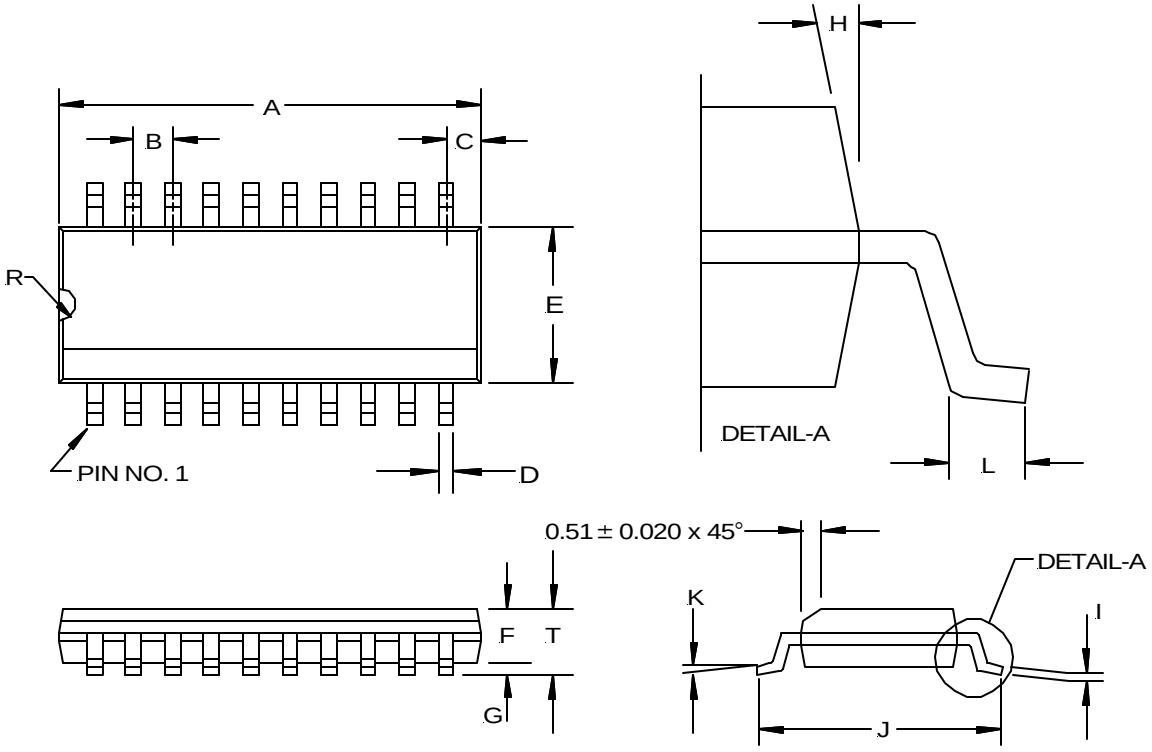
(F) TSSOP Package
20-Pin



SYMBOL DESIG	20-PIN		
	MIN	NOM	MAX
A		0.65 BSC	
B	4.30	4.40	4.50
C		6.40 BSC	
D	0.19	---	0.30
E		1.00	
F		1.00	
G	6.40	6.50	6.60
H	---	---	1.10
J	0.85	0.90	0.95
K	0.05	---	0.15
L		12° REF	
M		12° REF	
N	0°	---	8°
O		1.00 REF	
P	0.50	0.60	0.75
Q		0.20	
R	0.09	---	---
R1	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

(W) SOIC Package
20-Pin Surface Mount, Wide Body

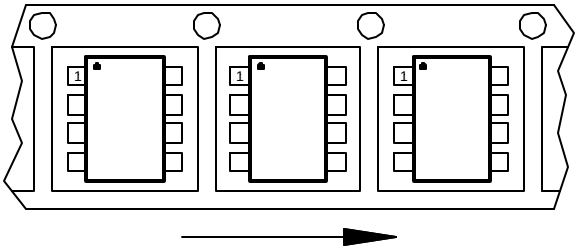


SYMBOL	20-PIN	
	MIN	MAX
A	12.598	12.979
B	1.018	1.524
C	0.66 REF	
D	0.33	0.508
E	7.40	7.60
F	2.032	2.64
G	0.10	0.30
I	0.229	0.32
J	10.008	10.654
K	0°	8°
L	0.406	1.270
R	0.63	0.89
T	2.337	2.642

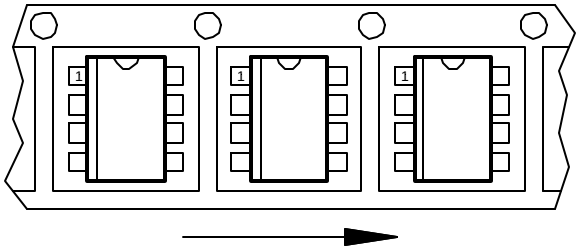
NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
F	TSSOP Plastic	20	74	2500	Fig A
W	SOIC, Wide Body	20	38	1000	Fig B



Feed Direction
Figure A



Feed Direction
Figure B

International
IOR Rectifier

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5-BIT PROGRAMMABLE SYNCHRONOUS BUCK, NON-SYNCHRONOUS, ADJUSTABLE LDO AND 200mA ON-BOARD LDO

FEATURES

- Provides Single Chip Solution for Vcore, GTL+, Clock Supply & 3.3V Switcher On-Board
- Second switcher provides simple control for the on-board 3.3V supply
- 200mA On-Board LDO Regulator
- Designed to meet Intel VRM 8.2 and 8.3 specification for Pentium II™
- On-Board DAC programs the output voltage from 1.3V to 3.5V
- Linear Regulator Controller On-Board for 1.5V GTL+ supply
- Loss-less Short Circuit Protection
- Synchronous Operation allows maximum efficiency
- Patented architecture allows fixed frequency operation as well as 100% duty cycle during dynamic load
- Minimum Part Count
- Soft-Start
- High current totem pole drivers for directly driving the external Power MOSFETs
- Power Good function monitors all outputs
- Over-Voltage Protection circuitry protects the switcher outputs and generates a fault output
- Thermal Shutdown

APPLICATIONS

- Total Power Solution for Pentium II processor application

DESCRIPTION

The IRU3007 controller IC is specifically designed to meet Intel specification for Pentium II™ microprocessor applications as well as the next generation of P6 family processors. The IRU3007 provides a single chip controller IC for the Vcore, LDO controller for GTL+ and an internal 200mA regulator for clock supply which are required for the Pentium II applications. It also contains a switching controller to convert 5V to 3.3V regulator for on-board applications that uses either AT type power supply or is desired not to rely on the ATX power supply's 3.3V output. These devices feature a patented topology that in combination with a few external components, as shown in the typical application circuit, will provide in excess of 14A of output current for an on-board DC/DC converter while automatically providing the right output voltage via the 5-bit internal DAC. The IRU3007 also features, loss-less current sensing for both switchers by using the $R_{DS(on)}$ of the high-side power MOSFET as the sensing resistor, internal current limiting for the clock supply, a Power Good window comparator that switches its open collector output low when any one of the outputs is outside of a pre-programmed window. Other features of the device are: Under-Voltage Lockout for both 5V and 12V supplies, an external programmable soft-start function, programming the oscillator frequency via an external resistor, Over-Voltage Protection (OVP) circuitry for both switcher outputs and an internal thermal shutdown.

TYPICAL APPLICATION

Note: Pentium II and Pentium Pro are trademarks of Intel Corp.

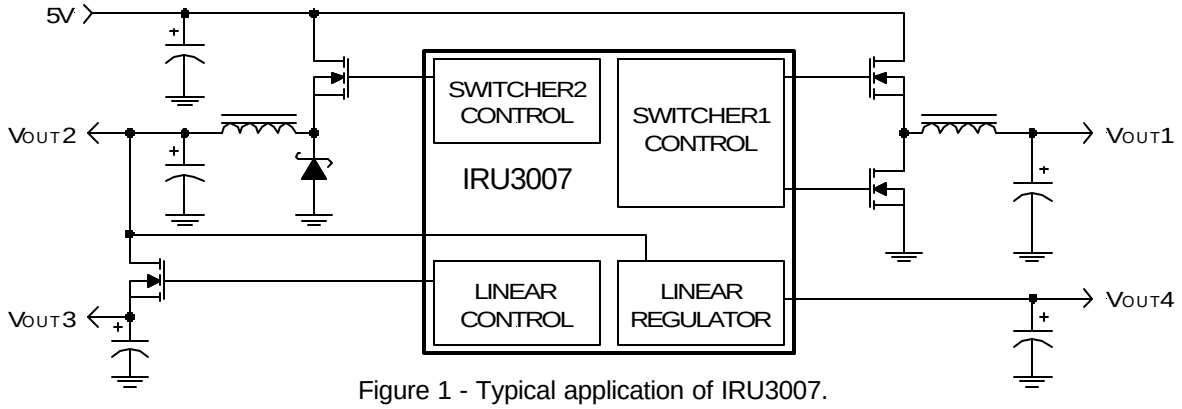


Figure 1 - Typical application of IRU3007.

PACKAGE ORDER INFORMATION

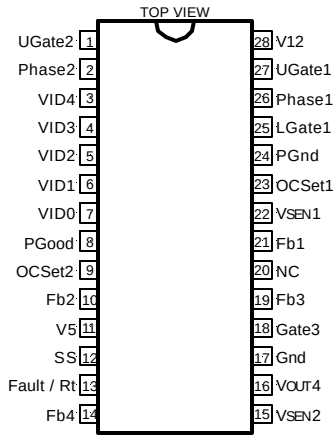
T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3007CW	28-pin Plastic SOIC WB (W)

ABSOLUTE MAXIMUM RATINGS

V5 Supply Voltage 7V
V12 Supply Voltage 20V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

28-PIN WIDE BODY PLASTIC SOIC (W)



θ_{JA} =80°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V12=12V, V5=5V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply UVLO Section						
UVLO Threshold-12V		Supply Ramping Up		10		V
UVLO Hysteresis-12V				0.4		V
UVLO Threshold-5V		Supply Ramping Up		4.3		V
UVLO Hysteresis-5V				0.3		V
Supply Current						
Operating Supply Current		V12 V5		6 30		mA
Switching Controllers; Vcore (V_{OUT}1) and I/O (V_{OUT}2)						
VID Section (Vcore only)						
DAC Output Voltage (Note 1)			0.99Vs	Vs	1.01Vs	V
DAC Output Line Regulation				0.1		%
DAC Output Temp Variation				0.5		%
VID Input LO					0.8	V
VID Input HI			2			V
VID Input Internal Pull-Up Resistor to V5			27			KΩ
V_{FB}2 Voltage				2		V
Oscillator Section (Internal)						KHz
Osc Frequency		Rt=Open		200		

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Comparator Section						
Input Bias Current					2	µA
Input Offset Voltage			-2		+2	mV
Delay to Output		V_{DIFF}=10mV			100	ns
Current Limit Section						
CS Threshold Set Current				200		µA
CS Comp Offset Voltage			-5		+5	mV
Hiccup Duty Cycle		C_{SS}=0.1µF		10		%
Output Drivers Section						
Rise Time		C_L=3000pF		70		ns
Fall Time		C_L=3000pF		70		ns
Dead Band Time Between High Side and Synch Drive (Vcore Switcher Only)		C_L=3000pF		200		ns
2.5V Regulator (V_{OUT}4)						
Reference Voltage	V_O4	T_A=25°C, V_{OUT}4=Fb4		1.260		V
Reference Voltage				1.260		V
Dropout Voltage		I_O=200mA		0.6		V
Load Regulation		1mA<I_O<200mA		0.5		%
Line Regulation		3.1V<$V_{I/O}$<4V, V_O=2.5V		0.2		%
Input Bias Current					2	µA
Output Current			200			mA
Current Limit			300			mA
Thermal Shutdown				145		°C
1.5V Regulator (V_{OUT}3)						
Reference Voltage	V_O3	T_A=25°C, Gate3=Fb3		1.260		V
Reference Voltage				1.260		V
Input Bias Current					2	µA
Output Drive Current			50			mA
Power Good Section						
Core UV Lower Trip Point		V_{SEN}1 Ramping Down		0.90Vs		V
Core UV Upper Trip Point		V_{SEN}1 Ramping Up		0.92Vs		V
Core UV Hysteresis				0.02Vs		V
Core OV Upper Trip Point		V_{SEN}1 Ramping Up		1.10Vs		V
Core OV Lower Trip Point		V_{SEN}1 Ramping Down		1.08Vs		V
Core OV Hysteresis				0.02Vs		V
I/O UV lower trip point		V_{SEN}2 Ramping Down		2.4		V
I/O UV Upper Trip Point		V_{SEN}2 Ramping Up		2.6		V
Fb4 Lower Trip Point		Fb4 Ramping Down		0.95		V
Fb4 Upper Trip Point		Fb4 Ramping Up		1.05		V
Fb3 Lower Trip Point		Fb3 Ramping Down		0.95		V
Fb3 Upper Trip Point		Fb3 Ramping Up		1.05		V
Power Good Output LO		R_L=3mA		0.4		V
Power Good Output HI		R_L=5K Pull Up to 5V		4.8		V
Fault (Over-Voltage) Section						
Core OV Upper Trip Point		V_{SEN}1 Ramping Up		1.17Vs		V
Core OV Lower Trip Point		V_{SEN}1 Ramping Down		1.15Vs		V
Soft-Start Section						
Pull-Up Resistor to 5V		OCSet=0V, Phase=5V		23		KΩ
I/O OV Upper Trip Point		V_{SEN}2 Ramping Up		4.3		V
I/O OV Lower Trip Point		V_{SEN}2 Ramping Down		4.2		V
Fault Output HI		I_O=3mA		10		V

Note 1: Vs refers to the set point voltage given in Table 1

D4	D3	D2	D1	D0	Vs
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05

D4	D3	D2	D1	D0	Vs
1	1	1	1	1	2.0
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

Table 1 - Set point voltage vs. VID codes

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	UGate2	Output driver for the high-side power MOSFET for the I/O supply.
2	Phase2	This pin is connected to the Source of the power MOSFET for the I/O supply and it provides the negative sensing for the internal current sensing circuitry.
3	VID4	This pin selects a range of output voltages for the DAC. When in the LO state the range is 1.3V to 2.05V and when it switches to HI state the range is 2.0V to 3.5V. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
4	VID3	MSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
5	VID2	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
6	VID1	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
7	VID0	LSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
8	PGood	This pin is an open collector output that switches LO when any of the outputs are outside of the specified under voltage trip point. It also switches low when $V_{SEN}1$ pin is more than 10% above the DAC voltage setting.
9	OCSet2	This pin is connected to the Drain of the power MOSFET of the I/O supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the CS threshold depending on the R_{DS} of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.

PIN#	PIN SYMBOL	PIN DESCRIPTION
10	Fb2	This pin provides the feedback for the non-synchronous switching regulator. A resistor divider is connected from this pin to $V_{OUT}2$ and ground that sets the output voltage. The value of the resistor connected from $V_{OUT}2$ to Fb2 must be less than 100Ω.
11	V5	5V supply voltage. A high frequency capacitor (0.1 to 1μF) must be placed close to this pin and connected from this pin to the ground plane for noise free operation.
12	SS	This pin provides the soft-start for the 2 switching regulators. An internal resistor charges an external capacitor that is connected from 5V supply to this pin which ramps up the outputs of the switching regulators, preventing the outputs from overshooting as well as limiting the input current. The second function of the Soft-Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting.
13	Fault / Rt	This pin has dual function. It acts as an output of the OVP circuitry or it can be used to program the frequency using an external resistor. When used as a fault detector, if any of the switcher outputs exceed the OVP trip point, the Fault pin switches to 12V and the soft-start cap is discharged. If the Fault pin is to be connected to any external circuitry, it needs to be buffered as shown in the application circuit.
14	Fb4	This pin provides the feedback for the internal LDO regulator that its output is $V_{OUT}4$.
15	$V_{SEN}2$	This pin is connected to the output of the I/O switching regulator. It is an input that provides sensing for the Under/Over-voltage circuitry for the I/O supply as well as the power for the internal LDO regulator.
16	$V_{OUT}4$	This pin is the output of the internal LDO regulator.
17	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane.
18	Gate3	This pin controls the gate of an external transistor for the 1.5V GTL+ linear regulator.
19	Fb3	This pin provides the feedback for the linear regulator that its output drive is Gate3.
20	NC	No connection.
21	Fb1	This pin provides the feedback for the synchronous switching regulator. Typically this pin can be connected directly to the output of the switching regulator. However, a resistor divider is recommended to be connected from this pin to $V_{OUT}1$ and ground to adjust the output voltage for any drop in the output voltage that is caused by the trace resistance. The value of the resistor connected from $V_{OUT}1$ to Fb1 must be less than 100Ω.
22	$V_{SEN}1$	This pin is internally connected to the undervoltage and overvoltage comparators sensing the Vcore status. It must be connected directly to the Vcore supply.
23	OCSet1	This pin is connected to the Drain of the power MOSFET of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the CS threshold depending on the R_{DS} of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.
24	PGnd	This pin serves as the Power ground pin and must be connected directly to the ground plane close to the source of the synchronous MOSFET. A high frequency capacitor (typically 1μF) must be connected from V12 pin to this pin for noise free operation.
25	LGate1	Output driver for the synchronous power MOSFET for the Core supply.
26	Phase1	This pin is connected to the Source of the power MOSFET for the Core supply and it provides the negative sensing for the internal current sensing circuitry.
27	UGate1	Output driver for the high-side power MOSFET for the Core supply.
28	V12	This pin is connected to the 12V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (typically 1μF) must be placed close to this pin and PGnd pin and be connected directly from this pin to the ground plane for noise free operation.

BLOCK DIAGRAM

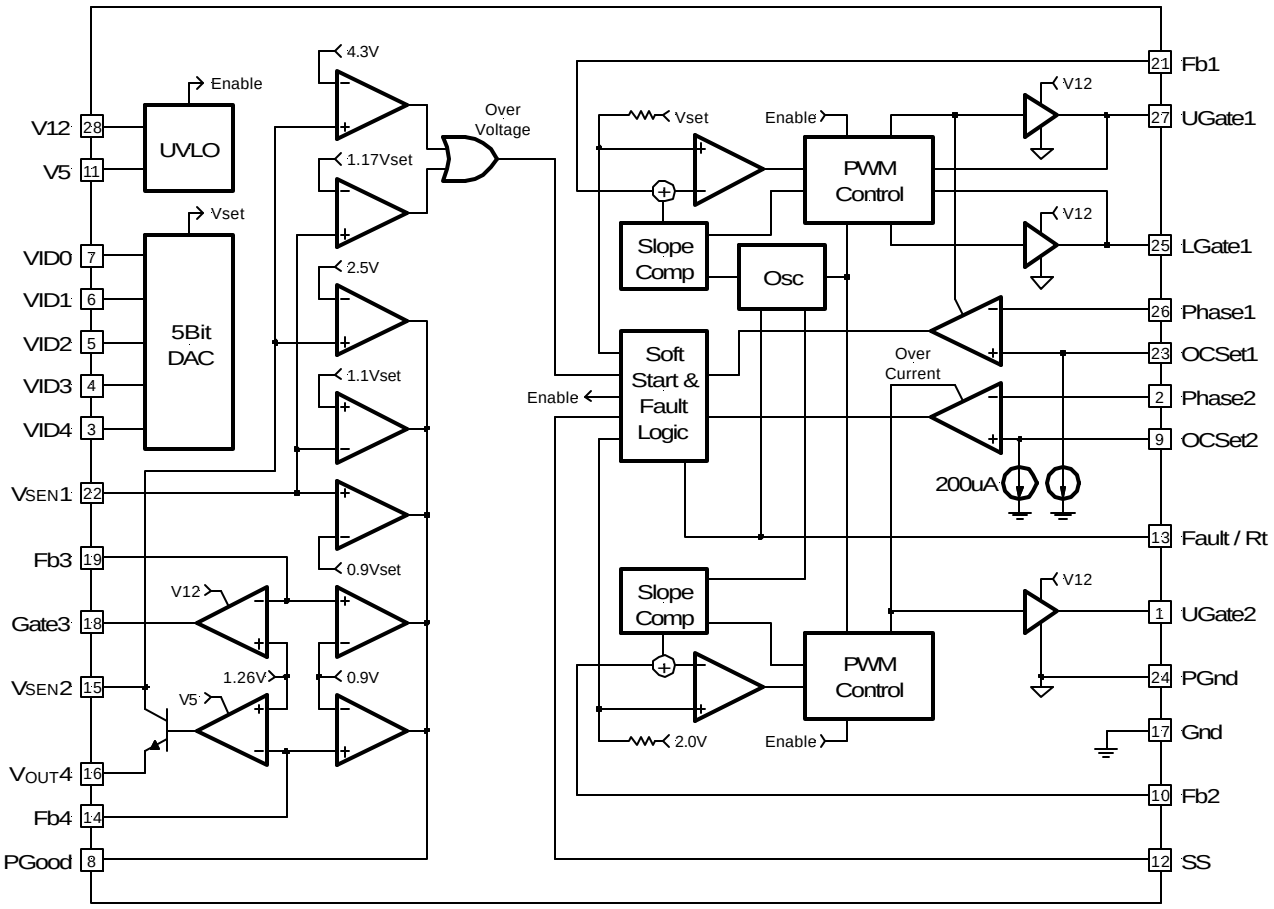


Figure 2 - Simplified block diagram of the IRU3007.

TYPICAL APPLICATION

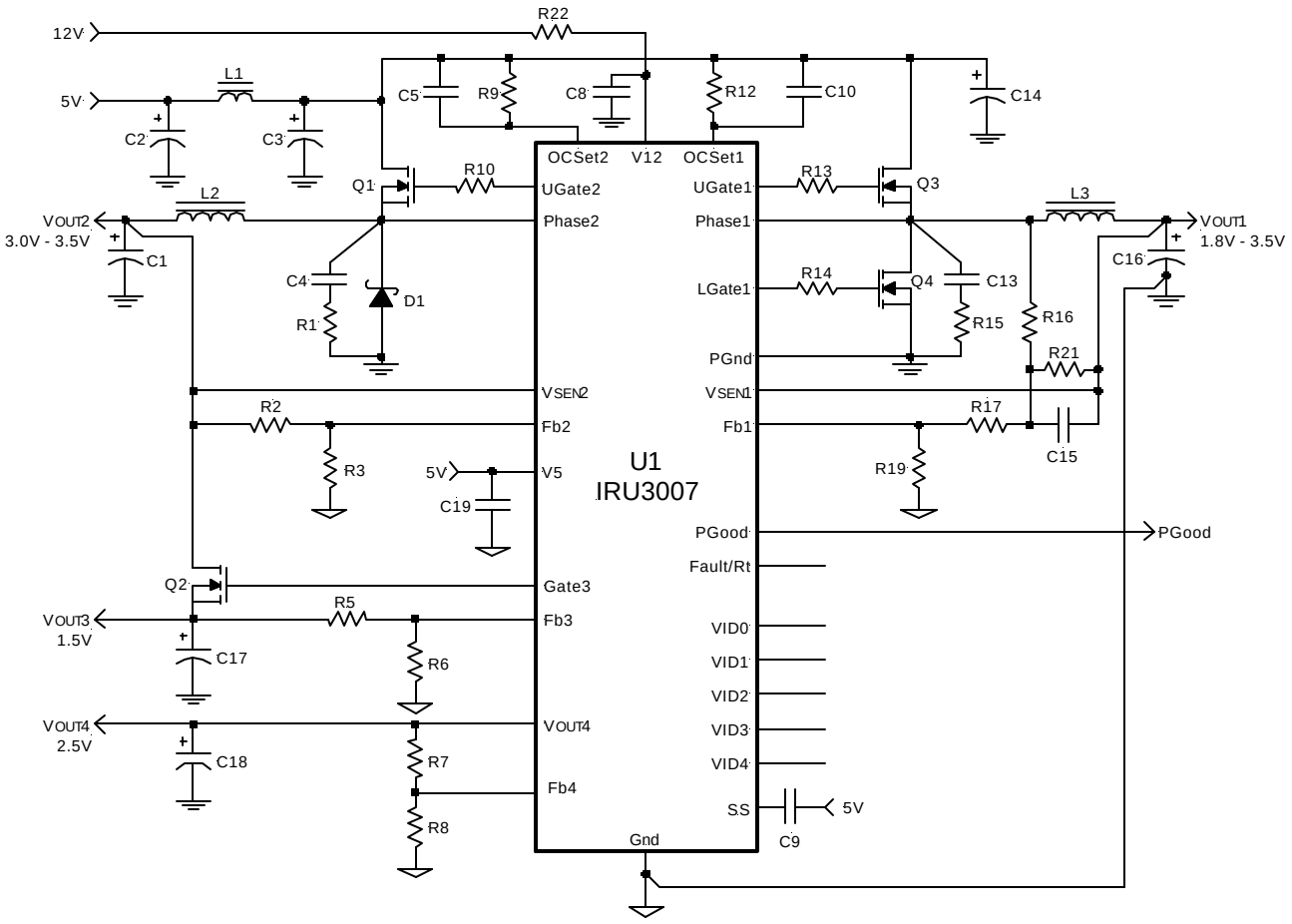


Figure 3 - Typical application of IRU3007 for an on-board DC-DC converter providing power for the Vcore, GTL+, Clock supply as well as an on-board 3.3V I/O supply for the Deschutes and the next generation processor applications.

IRU3007 APPLICATION PARTS LIST

Ref Desig	Description	Qty	Part #	Manuf
Q1	MOSFET	1	IRL3103S, TO-263 package	IR
Q2	MOSFET	1	IRLR024, TO-252 package	IR
Q3	MOSFET	1	IRL3103S, TO-263 package	IR
Q4	MOSFET with Schottky	1	IRL3103D1S, TO-263 package	IR
D1	Diode	1	MBRB1035, TO-263 package	IR
L1	Inductor	1	L=1μH, 5052 core with 4 turns of 1.0mm wire	Micro Metal
L2	Inductor	1	L=4.7μH, 5052 core with 11 turns of 1.0mm wire	Micro Metal
L3	Inductor	1	L=2.7μH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1	Capacitor, Electrolytic	2	6MV1500GX, 1500μF, 6.3V	Sanyo
C2	Capacitor, Electrolytic	1	10MV470GX, 470μF, 10V	Sanyo
C3	Capacitor, Electrolytic	1	10MV1200GX, 1200μF, 10V	Sanyo
C4, 13	Capacitor, Ceramic	2	1000pF, 0603	
C5, 10	Capacitor, Ceramic	2	220pF, 0603	
C8	Capacitor, Ceramic	1	1μF, 0805	
C9, 15, 19	Capacitor, Ceramic	3	1μF, 0603	
C14	Capacitor, Electrolytic	2	10MV1200GX, 1200μF, 10V	Sanyo
C16	Capacitor, Electrolytic	6	6MV1500GX, 1500μF, 6.3V	Sanyo
C17	Capacitor, Electrolytic	1	6MV1000GX, 1000μF, 6.3V	Sanyo
C18	Capacitor, Electrolytic	1	6MV150GX, 150μF, 6.3V	Sanyo
R1, 5, 13, 14	Resistor	4	4.7Ω, 5%, 1206	
R2	Resistor	1	75Ω, 1%, 0603	
R3, 6, 7, 8	Resistor	4	100Ω, 1%, 0603	
R5	Resistor	1	19.1Ω, 1%, 0603	
R9	Resistor	1	1.5KΩ, 5%, 0603	
R10	Resistor	1	10Ω, 5%, 1206	
R12	Resistor	1	3.3KΩ, 5%, 0603	
R16, 17, 21	Resistor	3	2.2KΩ, 1%, 0603	
R19	Resistor	1	220KΩ, 1%, 0603	
R22	Resistor	1	10Ω, 5%, 0603	

TYPICAL APPLICATION

(Dual Layout with HIP6019)

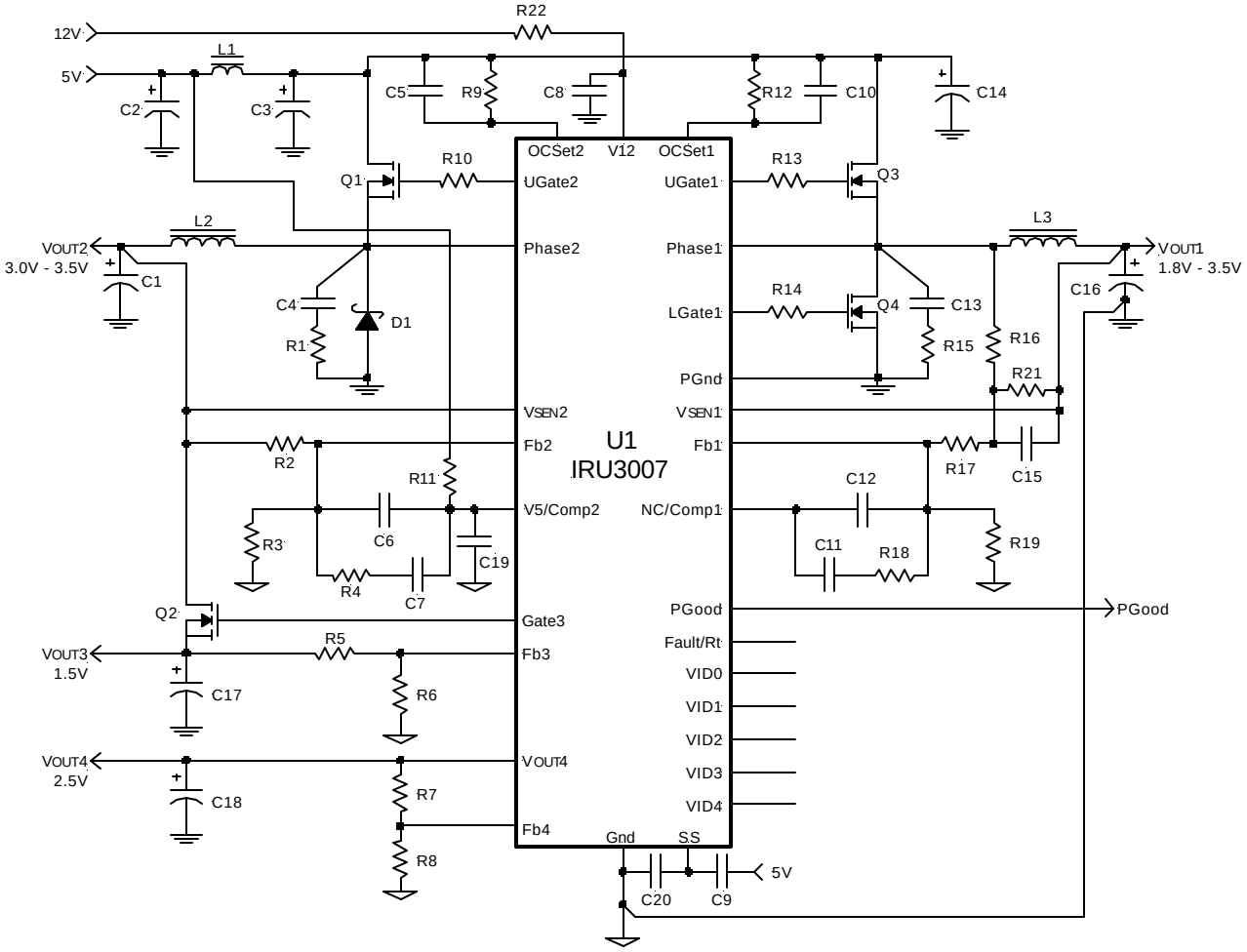


Figure 4 - Typical application of IRU3007 in a dual layout with HIP6019 for an on-board DC-DC converter providing power for the Vcore, GTL+, Clock supply as well as an on-board 3.3V I/O supply for the Deschutes and the next generation processor application.

Components that need to be modified to make the dual layout work for HIP6019 and IRU3007:

Part #	R4	R11	R18	C6	C7	C9	C11	C12	C19	C20
HIP6019	V	O	V	V	V	O	V	V	O	V
IRU3007	O	S	O	O	O	V	O	O	V	O

S - Short O - Open V - See IR or Harris parts list for the value

Table 2 - Dual layout component table.

IRU3007 APPLICATION PARTS LIST

Dual Layout with HIP6019

Ref Desig	Description	Qty	Part #	Manuf
Q1	MOSFET	1	IRL3103S, TO-263 package	IR
Q2	MOSFET	1	IRLR024, TO-252 package	IR
Q3	MOSFET	1	IRL3103S, TO-263 package	IR
Q4	MOSFET with Schottky	1	IRL3103D1S, TO-263 package	IR
D1	Diode	1	MBRB1035, TO-263 package	IR
L1	Inductor	1	L=1μH, 5052 core with 4 turns of 1.0 mm wire	Micro Metal
L2	Inductor	1	L=4.7μH, 5052 core with 11 turns of 1.0mm wire	Micro Metal
L3	Inductor	1	L=2.7μH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1	Capacitor, Electrolytic	2	6MV1500GX, 1500μF, 6.3V	Sanyo
C2	Capacitor, Electrolytic	1	10MV470GX, 470μF, 10V	Sanyo
C3	Capacitor, Electrolytic	1	10MV1200GX, 1200μF, 10V	Sanyo
C4, 13	Capacitor, Ceramic	2	1000pF, 0603	
C5, 10	Capacitor, Ceramic	2	220pF, 0603	
C6,7,11,12 20	Capacitor, Ceramic	5	See Table 2, dual layout component 0603 × 5	
C8	Capacitor, Ceramic	1	1μF, 0805	
C9,15,19	Capacitor, Ceramic	3	1μF, 0603	
C14	Capacitor, Electrolytic	2	10MV1200GX, 1200μF, 10V	Sanyo
C16	Capacitor, Electrolytic	6	6MV1500GX, 1500μF, 6.3V	Sanyo
C17	Capacitor, Electrolytic	1	6MV1000GX, 1000μF, 6.3V	Sanyo
C18	Capacitor, Electrolytic	1	6MV150GX, 150μF, 6.3V	Sanyo
R1,13,14 15	Resistor	4	4.7Ω, 5%, 1206	
R2	Resistor	1	75Ω, 1%, 0603	
R3,6,7,8	Resistor	4	100Ω, 1%, 0603	
R4, 18	Resistor	2	See Table 2, dual layout component 0603 × 2	
R5	Resistor	1	19.1Ω, 1%, 0603	
R9	Resistor	1	1.5KΩ, 5%, 0603	
R10	Resistor	1	10Ω, 5%, 1206	
R11	Resistor	1	0Ω, 0603	
R12	Resistor	1	3.3KΩ, 5%, 0603	
R16,17,21	Resistor	3	2.2KΩ, 1%, 0603	
R19	Resistor	1	220KΩ, 1%, 0603	
R22	Resistor	1	10Ω, 5%, 0603	

APPLICATION INFORMATION

An example of how to calculate the components for the application circuit is given below.

Assuming, two set of output conditions that this regulator must meet for Vcore:

a) Vo=2.8V , Io=14.2A, ΔVo=185mV, ΔIo=14.2A

b) Vo=2V , Io=14.2A, ΔVo=140mV, ΔIo=14.2A

Also, the on-board 3.3V supply must be able to provide 10A load current and maintain less than ±5% total output voltage variation.

The regulator design will be done such that it meets the worst case requirement of each condition.

Output Capacitor Selection

Vcore

The first step is to select the output capacitor. This is done primarily by selecting the maximum ESR value that meets the transient voltage budget of the total ΔVo specification. Assuming that the regulators DC initial accuracy plus the output ripple is 2% of the output voltage, then the maximum ESR of the output capacitor is calculated as:

$$ESR \leq \frac{100}{14.2} = 7m\Omega$$

The Sanyo MVGX series is a good choice to achieve both the price and performance goals. The 6MV1500GX, 1500μF, 6.3V has an ESR of less than 36mΩ typical. Selecting 6 of these capacitors in parallel has an ESR of ≈ 6mΩ which achieves our low ESR goal.

Other type of Electrolytic capacitors from other manufacturers to consider are the Panasonic FA series or the Nichicon PL series.

3.3V supply

For the 3.3V supply, since there is not a fast transient requirement, 2 of the 1500μF capacitors is sufficient.

Reducing the Output Capacitors Using Voltage Level Shifting Technique

The trace resistance or an external resistor from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transitioning from light load to full load and vice versa. To accomplish this, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the Gnd pin of the IRU3007 is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70mV or 35mV higher than the DAC voltage setting. This intentional voltage level shifting during the load transient eases the requirement for the output capacitor ESR at the cost of load regulation. One can show that the new ESR requirement eases up by half the total trace resistance. For example, if the ESR requirement of the output capacitors without voltage level shifting must be 7mΩ then after level shifting the new ESR will only need to be 8.5mΩ if the trace resistance is 5mΩ (7+5/2=9.5). However, one must be careful that the combined "voltage level shifting" and the transient response is still within the maximum tolerance of the Intel specification. To insure this, the maximum trace resistance must be less than:

$$Rs \leq 2 \times \frac{(Vspec - 0.02 \times Vo - \Delta Vo)}{\Delta I}$$

Where :

Rs = Total maximum trace resistance allowed

Vspec = Intel total voltage spec

Vo = Output voltage

ΔVo = Output ripple voltage

ΔI = load current step

For example, assuming:

Vspec = ±140mV = ±0.1V for 2V output

Vo = 2V

ΔVo = assume 10mV = 0.01V

ΔI = 14.2A

Then the Rs is calculated to be:

$$Rs \leq 2 \times \frac{(0.140 - 0.02 \times 2 - 0.01)}{14.2} = 12.6m\Omega$$

However, if a resistor of this value is used, the maximum power dissipated in the trace (or if an external resistor is being used) must also be considered. For example if Rs=12.6mΩ, the power dissipated is:

$$Io^2 \times Rs = 14.2^2 \times 12.6 = 2.54W$$

This is a lot of power to be dissipated in a system. So, if the Rs=5mΩ, then the power dissipated is about 1W, which is much more acceptable. If level shifting is not implemented, then the maximum output capacitor ESR was shown previously to be 7mΩ which translated to ≈ 6

of the 1500μF, 6MV1500GX type Sanyo capacitors. With Rs=5mΩ, the maximum ESR becomes 9.5mΩ which is equivalent to ≈ 4 caps. Another important consideration is that if a trace is being used to implement the resistor, the power dissipated by the trace increases the case temperature of the output capacitors which could seriously affect the life span of the output capacitors.

Output Inductor Selection

The output inductance must be selected such that under low line and the maximum output voltage condition, the inductor current slope times the output capacitor ESR is ramping up faster than the capacitor voltage is drooping during a load current step. However, if the inductor is made too small, the output ripple current and ripple voltage will become too large. One solution to bring the ripple current down is to increase the switching frequency, however that will be at the cost of reduced efficiency and higher system cost. The following set of formulas are derived to achieve optimum performance without many design iterations.

The maximum output inductance is calculated using the following equation:

$$L = ESR \times C \times \frac{(V_{IN(MIN)} - Vo_{(MAX)})}{(2 \times \Delta I)}$$

Where:

$V_{IN(MIN)}$ = Minimum input voltage

For Vo = 2.8V and ΔI = 14.2A, we get:

$$L = 0.006 \times 9000 \times \frac{(4.75 - 2.8)}{(2 \times 14.2)} = 3.7\mu H$$

Assuming that the programmed switching frequency is set at 200KHz, an inductor is designed using the Micrometals' powder iron core material. The summary of the design is outlined below:

The selected core material is Powder Iron, the selected core is T50-52D from Micro Metal wound with 8 turns of #16 AWG wire, resulting in 3μH inductance with ≈ 3 mΩ of DC resistance.

Assuming L=3μH and Fsw=200KHz (switching frequency), the inductor ripple current and the output ripple voltage is calculated using the following set of equations:

T ≡ Switching Period
D ≡ Duty Cycle
Vsw ≡ High-side MOSFET ON Voltage
R_{DS} ≡ MOSFET On-Resistance
Vsync ≡ Synchronous MOSFET ON Voltage
ΔIr ≡ Inductor Ripple Current
ΔVo ≡Output Ripple Voltage

$T = 1 / Fsw$

$Vsw = Vsync = Io \times R_{DS}$

$D \approx (Vo + Vsync) / (V_{IN} - Vsw + Vsync)$

$T_{ON} = D \times T$

$T_{OFF} = T - T_{ON}$

$\Delta Ir = (Vo + Vsync) \times T_{OFF} / L$

$\Delta Vo = \Delta Ir \times ESR$

In our example for Vo = 2.8V and 14.2 A load, assuming IRL3103 MOSFET for both switches with maximum on resistance of 19mΩ, we have:

$T = 1 / 200000 = 5\mu s$

$Vsw = Vsync = 14.2 \times 0.019 = 0.27V$

$D \approx (2.8 + 0.27) / (5 - 0.27 + 0.27) = 0.61$

$T_{ON} = 0.61 \times 5 = 3.1\mu s$

$T_{OFF} = 5 - 3.1 = 1.9\mu s$

$\Delta Ir = (2.8 + 0.27) \times 1.9 / 3 = 1.94A$

$\Delta Vo = 1.94 \times 0.006 = 0.011V = 11mV$

Power Component Selection

Vcore

Assuming IRL3103 MOSFETs as power components, we will calculate the maximum power dissipation as follows:

For high side switch the maximum power dissipation happens at maximum Vo and maximum duty cycle.

$D_{MAX} \approx (2.8 + 0.27) / (4.75 - 0.27 + 0.27) = 0.65$

$P_{DH} = D_{MAX} \times Io^2 \times R_{DS(MAX)}$

$P_{DH} = 0.65 \times 14.2^2 \times 0.029 = 3.8W$

$R_{DS(MAX)}$=Maximum $R_{DS(ON)}$ of the MOSFET at 125°C

For synch MOSFET, maximum power dissipation happens at minimum Vo and minimum duty cycle.

$D_{MIN} \approx (2 + 0.27) / (5.25 - 0.27 + 0.27) = 0.43$

$P_{DS} = (1 - D_{MIN}) \times Io^2 \times R_{DS(MAX)}$

$P_{DS} = (1 - 0.43) \times 14.2^2 \times 0.029 = 3.33W$

3.3V Supply

Again, for high side switch the maximum power dissipation happens at maximum Vo and maximum duty cycle. The duty cycle equation for non synchronous replaces the forward voltage of the diode with the Synch MOSFET on voltage. In equations below:

Vf = 0.5V

$D_{MAX} \approx (3.3 + 0.5) / (4.75 - 0.27 + 0.5) = 0.76$

$P_{DH} = D_{MAX} \times Io^2 \times R_{DS(MAX)}$

$P_{DH} = 0.76 \times 10^2 \times 0.029 = 2.21W$

$R_{DS(MAX)}$ = Maximum $R_{DS(ON)}$ of the MOSFET at 125°C

For diode, the maximum power dissipation happens at minimum Vo and minimum duty cycle.

$D_{MIN} \approx (3.3 + 0.5) / (5.25 - 0.27 + 0.5) = 0.69$

$P_{DD} = (1 - D_{MIN}) \times Io \times Vf$

$P_{DD} = (1 - 0.69) \times 10 \times 0.5 = 1.55W$

Switcher Current Limit Protection

The IRU3007 uses the MOSFET $R_{DS(ON)}$ as the sensing resistor to sense the MOSFET current and compares to a programmed voltage which is set externally via a resistor (Rcs) placed between the drain of the MOSFET and the "CS+" terminal of the IC as shown in the application circuit.

For example, if the desired current limit point is set to be 22A for the synchronous and 16A for the non synchronous, and from our previous selection, the maximum MOSFET $R_{DS(ON)}$=19mW, then the current sense resistor Rcs is calculated as:

Vcore

$Vcs = I_{CL} \times R_{DS} = 22 \times 0.019 = 0.418V$

$Rcs = Vcs / I_B = (0.418V) / (200\mu A) = 2.1K\Omega$

Where:
I_B=200μA is the internal current setting of the IRU3007

3.3V supply

$Vcs = I_{CL} \times R_{DS} = 16 \times 0.019 = 0.3V$

$Rcs = Vcs / I_B = (0.3V) / (200\mu A) = 1.50K\Omega$

1.5V, GTL+ Supply LDO Power MOSFET Selection

The first step in selecting the power MOSFET for the 1.5V linear regulator is to select its maximum $R_{DS(ON)}$ of the pass transistor based on the input to output Dropout voltage and the maximum load current.

For Vo = 1.5V, V_{IN} = 3.3V and I_L = 2A:

$R_{DS(MAX)} = (V_{IN} - Vo) / I_L = (3.3 - 1.5) / 2 = 0.9\Omega$

Note: Since the MOSFETs $R_{DS(ON)}$ increases with temperature, this number must be divided by ≈ 1.5, in order to find the $R_{DS(ON)}$ max at room temperature. The Motorola MTP3055VL has a maximum of 0.18Ω $R_{DS(ON)}$ at room temperature, which meets our requirement.

To select the heat sink for the LDO MOSFET the first step is to calculate the maximum power dissipation of the device and then follow the same procedure as for the switcher.

Where:
P_D = Power Dissipation of the Linear Regulator
I_L = Linear Regulator Load Current

For the 1.5V and 2A load:

$P_D = (V_{IN} - Vo) \times I_L$

$P_D = (3.3 - 1.5) \times 2 = 3.6W$

Assuming $T_{J(MAX)}$ = 125°C:

$Ts = T_J - P_D \times (\theta_{JC} + \theta cs)$

$Ts = 125 - 3.6 \times (1.8 + 0.05) = 118°C$

With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance (θ_{SA}) is calculated as follows:

Assuming T_A = 35°C:

$\Delta T = Ts - T_A = 118 - 35 = 83°C$
Temperature Rise Above Ambient

$\theta_{SA} = \Delta T / P_D = 83 / 3.6 = 23°C/W$

The same heat sink as the one selected for the switcher MOSFETs is also suitable for the 1.5V regulator.

2.5V Clock Supply

The IRU3007 provides a complete 2.5V regulator with a minimum of 200mA current capability. The internal regulator has short circuit protection with internal thermal shutdown.

1.5V and 2.5V Supply Resistor Divider Selection

Since the internal voltage reference for the linear regulators is set at 1.26V for IRU3007, there is a need to use external resistor dividers to step up the voltage. The resistor dividers are selected using the following equations:

$Vo = (1 + Rt / R_B) \times V_{REF}$

Where:
Rt = Top resistor divider
R_B = Bottom resistor divider
V_{REF} = 1.26V typical

For 1.5V supply
Assuming R_B = 1KΩ:

$Rt = R_B \times [(Vo / V_{REF}) - 1]$

$Rt = 1 \times [(1.5 / 1.26) - 1] = 191\Omega$

For 2.5V supply

Assuming R_B = 1.02KΩ:

$$Rt = R_B \times [(Vo / V_{REF}) - 1]$$

$$Rt = 1.02 \times [(2.5 / 1.26) - 1] = 1K\Omega$$

Switcher Output Voltage Adjust

Vcore

As it was discussed earlier, the trace resistance from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transitioning from light load to full load and vice versa. To account for the DC drop, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the Gnd pin of the IRU3007 is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70mV or 35mV higher than the DAC voltage setting. To do this, the top resistor of the resistor divider (R12 in the application circuit) is set at 100Ω, and the R19 is calculated. For example, if DAC voltage setting is for 2.8V and the desired output under light load is 2.835V, then R19 is calculated using the following formula:

$$R19 = 100 \times [V_{DAC} / (Vo - 1.004 \times V_{DAC})] \quad (\Omega)$$

$$R19 = 100 \times [2.8 / (2.835 - 1.004 \times 2.800)] = 11.76K\Omega$$

Select 11.8KΩ, 1%

Note: The value of the top resistor must not exceed 100Ω**.** The bottom resistor can then be adjusted to raise the output voltage.

3.3V supply

The loop gain for the non-synchronous switching regulator is intentionally set low to take advantage of the level shifting technique to reduce the number of output capacitors. Typically there is a 1% drop in the output voltage from light load (discontinuous conduction mode) to full load (continuous conduction mode) in the 3.3V supply. To account for this, the output voltage is set at 3.5V typically. The same procedure as for the synchronous is applied to the non-synch with the exception that the internal voltage reference of this regulator is internally set at 2V. The following is the set of equations to use for the output voltage setting for the non-synchronous assuming the Vo=3.5V and R2=75Ω (R2 is the top resistor in the application circuit).

The bottom resistor, R3 is calculated as follows:

$$R3 = R2 \times [2 / (Vo - 2)] \quad (\Omega)$$

$$R3 = 75 \times [2 / (3.5 - 2)] = 100\Omega, 1\%$$

Note: The value of the top resistor, R2 must not exceed 100Ω**.**

Soft-Start Capacitor Selection

The soft-start capacitor must be selected such that during the start up when the output capacitors are charging up, the peak inductor current does not reach the current limit threshold. A minimum of 1μF capacitor insures this for most applications. An internal 10μA current source charges the soft-start capacitor which slowly ramps up the inverting input of the PWM comparator Vfb3. This insures the output voltage to ramp at the same rate as the soft-start cap thereby limiting the input current. For example, with 1μF and the 10μA internal current source the ramp up rate is (ΔV/Δt)=I/C=1V/100ms. Assuming that the output capacitance is 9000μF, the maximum start up current will be:

$$I = 9000\mu F \times (1V / 100ms) = 0.09A$$

Input Filter

It is highly recommended to place an inductor between the system 5V supply and the input capacitors of the switching regulator to isolate the 5V supply from the switching noise that occurs during the turn on and off of the switching components. Typically an inductor in the range of 1 to 3μH will be sufficient in this type of application.

External Shutdown

The best way to shutdown the IRU3007 is to pull down on the soft-start pin using an external small signal transistor such as 2N3904 or 2N7002 small signal MOSFET. This allows slow ramp up of the output, the same as the power up.

Layout Considerations

Switching regulators require careful attention to the layout of the components, specifically power components since they switch large currents. These switching components can create large amount of voltage spikes and high frequency harmonics if some of the critical components are far away from each other and are connected with inductive traces. The following is a guideline of how to place the critical components and the connections between them in order to minimize the above issues.

Start the layout by first placing the power components:

1) Place the input capacitors C3 and C14 and the high side MOSFETs, Q1 and Q3 as close to their respective input caps as possible.

2) Place the synchronous MOSFET, Q2 and the Q3 as close to each other as possible with the intention that the source of Q3 and drain of the Q4 has the shortest length. Repeat this for the Q1 and D1 for the non-synchronous.

3) Place the snubber R15 and C13 between Q4 and Q3. Repeat this for R1 and C4 with respect to the Q1 and D1 for the non-synchronous.

4) Place the output inductor , L3 and the output capacitors, C16 between the MOSFET and the load with output capacitors distributed along the slot 1 and close to it. Repeat this for L2 with respect to the C1 for the non-synchronous.

5) Place the bypass capacitors, C8 and C19 right next to 12V and 5V pins. C8 next to the 12V, pin 28 and C19 next to the 5V, pin 11.

6) Place the IRU3007 such that the pwm output drives, pins 27 and 25 are relatively short distance from gates of Q3 and Q4. The non-synch MOSFET must also be situated such that the distance from its gate to the pin 1 of the IRU3007 is also relatively short.

7) Place all resistor dividers close to their respective feedback pins.

8) Place the 2.5V output capacitor, C18 close to the pin 16 of the IC and the 1.5V output capacitor, C17 close to the Q2 MOSFET.

   Note: It is better to place the 1.5V linear regulator components close to the IRU3007 and then run a trace from the output of the regulator to the load. However, if this is not possible then the trace from the linear drive output pin, pin 18 must be run away from any high frequency data signals.

   It is critical, to place high frequency ceramic capacitors close to the clock chip and termination resistors to provide local bypassing.

9) Place R12 and C10 close to pin 23 and R9 and C5 close to pin 9.

10) Place C9 close to pin 12

Component connections:

Note: It is extremely important that no data bus should be passing through the switching regulator section specifically close to the fast transition nodes such as PWM drives or the inductor voltage.

Using the 4 layer board, dedicate one layer to ground, another layer as the power layer for the 5V, 3.3V, Vcore, 1.5V and if it is possible, for the 2.5V.

Connect all grounds to the ground plane using direct vias to the ground plane.

Use large low inductance/low impedance plane to connect the following connections either using component side or the solder side.

a) C14 to Q3 Drain and C3 to Q1 drain
b) Q3 Source to Q4 Drain and Q1 Source to D1 cathode
c) Q4 drain to L3 and D1 cathode to L2
d) L3 to the output capacitors, C16 and L2 to the output capacitors, C1
e) C16 to the load, slot 1
f) Input filter L1 to the C16 and C3
g) C1 to Q2 drain
h) C17 to the Q2 source
I) A minimum of 0.2 inch width trace from the C18 capacitor to pin 16

Connect the rest of the components using the shortest connection possible.

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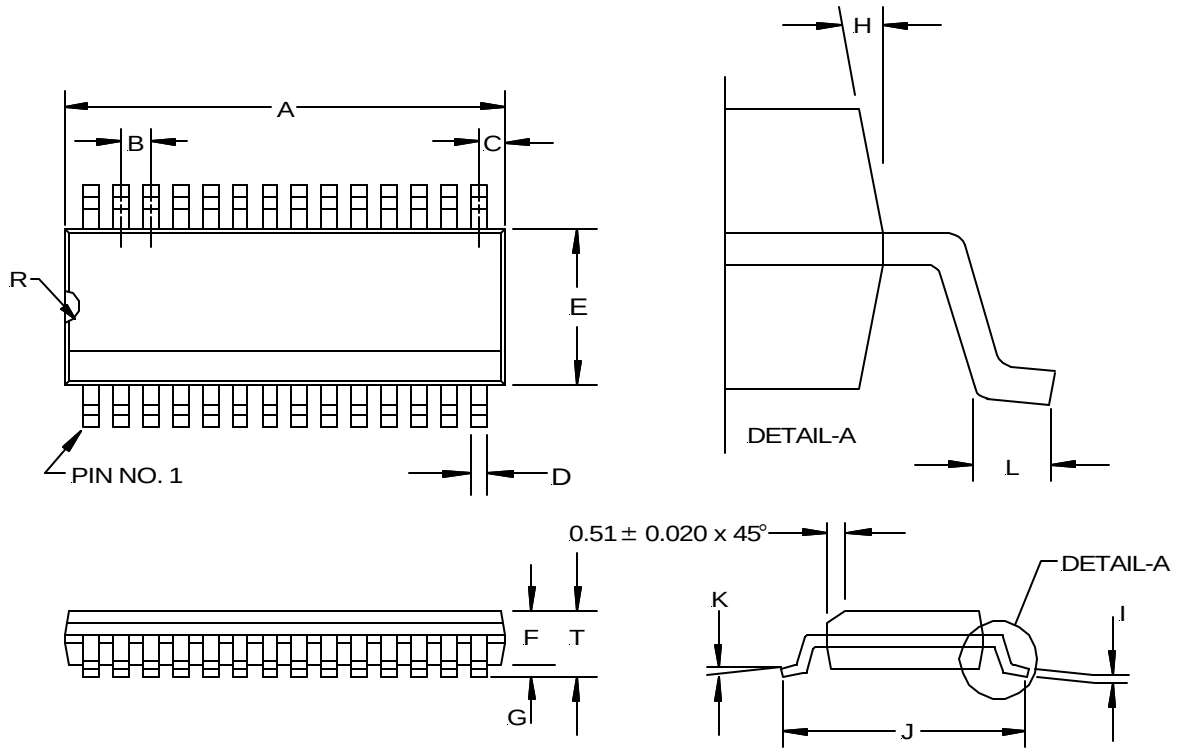
(W) SOIC Package
28-Pin Surface Mount, Wide Body

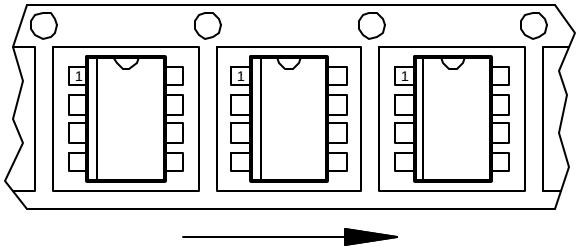


SYMBOL	28-PIN	
	MIN	MAX
A	17.73	17.93
B	1.27 BSC	
C	0.66 REF	
D	0.36	0.46
E	7.40	7.60
F	2.44	2.64
G	0.10	0.30
I	0.23	0.32
J	10.11	10.51
K	0°	8°
L	0.51	1.01
R	0.63	0.89
T	2.44	2.64

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
W	SOIC, Wide Body	28	27	1000	Fig A



Feed Direction
Figure A

IRU3011

5-BIT PROGRAMMABLE SYNCHRONOUS BUCK CONTROLLER IC

FEATURES

- Dual Layout compatible with HIP6004A
- Designed to meet Intel specification of VRM8.4 for Pentium III™
- On-Board DAC programs the output voltage from 1.3V to 3.5V. The IRU3011 remains on for VID code of (11111).
- Loss-less Short Circuit Protection
- Synchronous operation allows maximum efficiency
- Patented architecture allows fixed frequency operation as well as 100% duty cycle during dynamic load
- Over-Voltage Protection Output
- Soft-Start
- High current totem pole driver for direct driving of the external power MOSFET
- Power Good Function

APPLICATIONS

- Pentium III & Pentium II™ processor DC to DC converter application
- Low Cost Pentium with AGP

DESCRIPTION

The IRU3011 controller IC is specifically designed to meet Intel specification for latest Pentium III™ microprocessor applications as well as the next generation P6 family processors. These products feature a patented topology that in combination with a few external components as shown in the typical application circuit,will provide in excess of 20A of output current for an on-board DC/DC converter while automatically providing the right output voltage via the 5-bit internal DAC. These devices also features, loss less current sensing by using the $R_{DS(ON)}$ of the high side Power MOSFET as the sensing resistor, a Power Good window comparator that switches its open collector output low when the output is outside of a ±10% window and an Over-Voltage Protection output. Other features of the device are: Under-voltage lockout for both 5V and 12V supplies, an external programmable soft-start function as well as programming the oscillator frequency by using an external capacitor.

TYPICAL APPLICATION

Note: Pentium II and Pentium III are trade marks of Intel Corp.

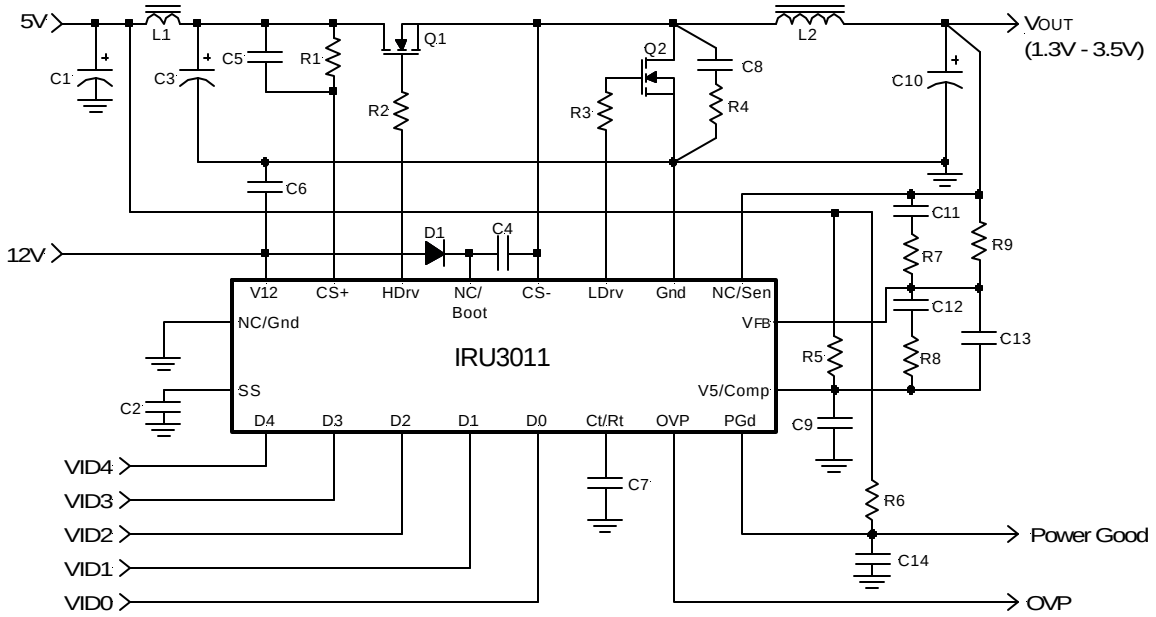


Figure 1 - Typical application of the IRU3011.

PACKAGE ORDER INFORMATION

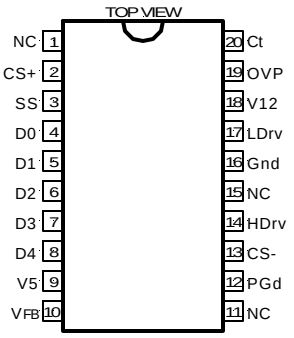
T_A (°C)	DEVICE	PACKAGE	VID VOLTAGE RANGE
0 To 70	IRU3011CW	20-Pin Plastic SOIC WB (W)	1.3V to 3.5V

ABSOLUTE MAXIMUM RATINGS

V5 Supply Voltage 7V
V12 Supply Voltage 20V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

20-PIN WIDE BODY PLASTIC SOIC (W)



θ_{JA} =85°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V12=12V, V5=5V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
VID Section						
DAC Output Voltage (Note 1)			0.99Vs	Vs	1.01Vs	V
DAC Output Line Regulation					0.1	%
DAC Output Temp Variation					0.5	%
VID Input LO					0.4	V
VID Input HI			2			V
VID Input Internal Pull-Up Resistor to V5				27		KΩ
Power Good Section						
Under-Voltage lower trip point		V_{OUT} Ramping Down	0.89Vs	0.90Vs	0.91Vs	V
Under-Voltage upper trip point		V_{OUT} Ramping Up		0.92Vs		V
UV Hysterises			0.015Vs	0.02Vs	0.025Vs	V
Over-Voltage upper trip point		V_{OUT} Ramping Up	1.09Vs	1.10Vs	1.11Vs	V
Over-Voltage lower trip point		V_{OUT} Ramping Down		1.08Vs		V
OV Hysteresis			0.015Vs	0.02Vs	0.025Vs	V
Power Good Output LO		R_L=3mA			0.4	V
Power Good Output HI		R_L=5K Pull-Up to 5V	4.8			V
Soft-Start Section						
Soft-Start Current		CS+=0V, CS-=5V		10		μA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
UVLO Section						
UVLO Threshold-12V		Supply Ramping Up	9.2	10	10.8	V
UVLO Hysteresis-12V			0.3	0.4	0.5	V
UVLO Threshold-5V		Supply Ramping Up	4.1	4.3	4.5	V
UVLO Hysteresis-5V			0.2	0.3	0.4	V
Error Comparator Section						
Input Bias Current					2	µA
Input Offset Voltage			-2		+2	mV
Delay to Output		V_{DIFF}=10mV			100	ns
Current Limit Section						
CS Threshold Set Current			160	200	240	µA
CS Comp Offset Voltage			-5		+5	mV
Hiccup Duty Cycle		Css=0.1µF			2	%
Supply Current						
Operating Supply Current		C_L=3000pF: V5 V12		 20 14		 mA
Output Drivers Section						
Rise Time		C_L=3000pF		70	100	ns
Fall Time		C_L=3000pF		70	130	ns
Dead Band Time		C_L=3000pF	100	200	300	ns
Oscillator Section						
Osc Frequency		Ct=150pF	190	220	250	KHz
Osc Valley					0.2	V
Osc Peak				V5		V
Over-Voltage Section						
OVP Drive Current						mA

Note 1: Vs refers to the set point voltage given in Table 1.

D4	D3	D2	D1	D0	Vs
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05

D4	D3	D2	D1	D0	Vs
1	1	1	1	1	2.0
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

Table 1 - Set point voltage vs. VID codes.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	NC	No connection.
2	CS+	This pin is connected to the Drain of the power MOSFET of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the CS threshold depending on the R_{DS} of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.
3	SS	This pin provides the soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to the ground which ramps up the outputs of the switching regulator, preventing the outputs from overshooting as well as limiting the input current. The second function of the Soft-Start cap is to provide long off time for the synchronous MOSFET or the Catch diode (HICCUP) during current limiting.
4	D0	LSB input to the DAC that programs the output voltage. This pin can be pulled up externally by a 10K resistor to either 3.3V or 5V supply.
5	D1	Input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10KΩ resistor to either 3.3V or 5V supply.
6	D2	Input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10K resistor to either 3.3V or 5V supply.
7	D3	MSB input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10K resistor to either 3.3V or 5V supply.
8	D4	This pin selects a range of output voltages for the DAC.
9	V5	5V supply voltage.
10	V_{FB}	This pin is connected directly to the output of the Core supply to provide feedback to the Error comparator.
11	NC	No connection.
12	PGd	This pin is an open collector output that switches LO when the output of the converter is not within ±10% (typ) of the nominal output voltage. When PGd pin switches LO the saturation voltage is less than 0.4V at 3mA.
13	CS-	This pin is connected to the Source of the power MOSFET for the Core supply and it provides the negative sensing for the internal current sensing circuitry.
14	HDrv	Output driver for the high side power MOSFET.
15	NC	No connection.
16	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane. A high frequency capacitor (0.1 to 1μF) must be connected from V5 and V12 pins to this pin for noise free operation.
17	LDrv	Output driver for the synchronous power MOSFET.
18	V12	This pin is connected to the 12 V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (0.1 to 1μF) must be connected directly from this pin to ground pin in order to supply the peak current to the power MOSFET during the transitions.
19	OVP	Over-voltage comparator output.
20	Ct	This pin programs the oscillator frequency in the range of 50KHz to 500KHz with an external capacitor connected from this pin to the ground.

BLOCK DIAGRAM

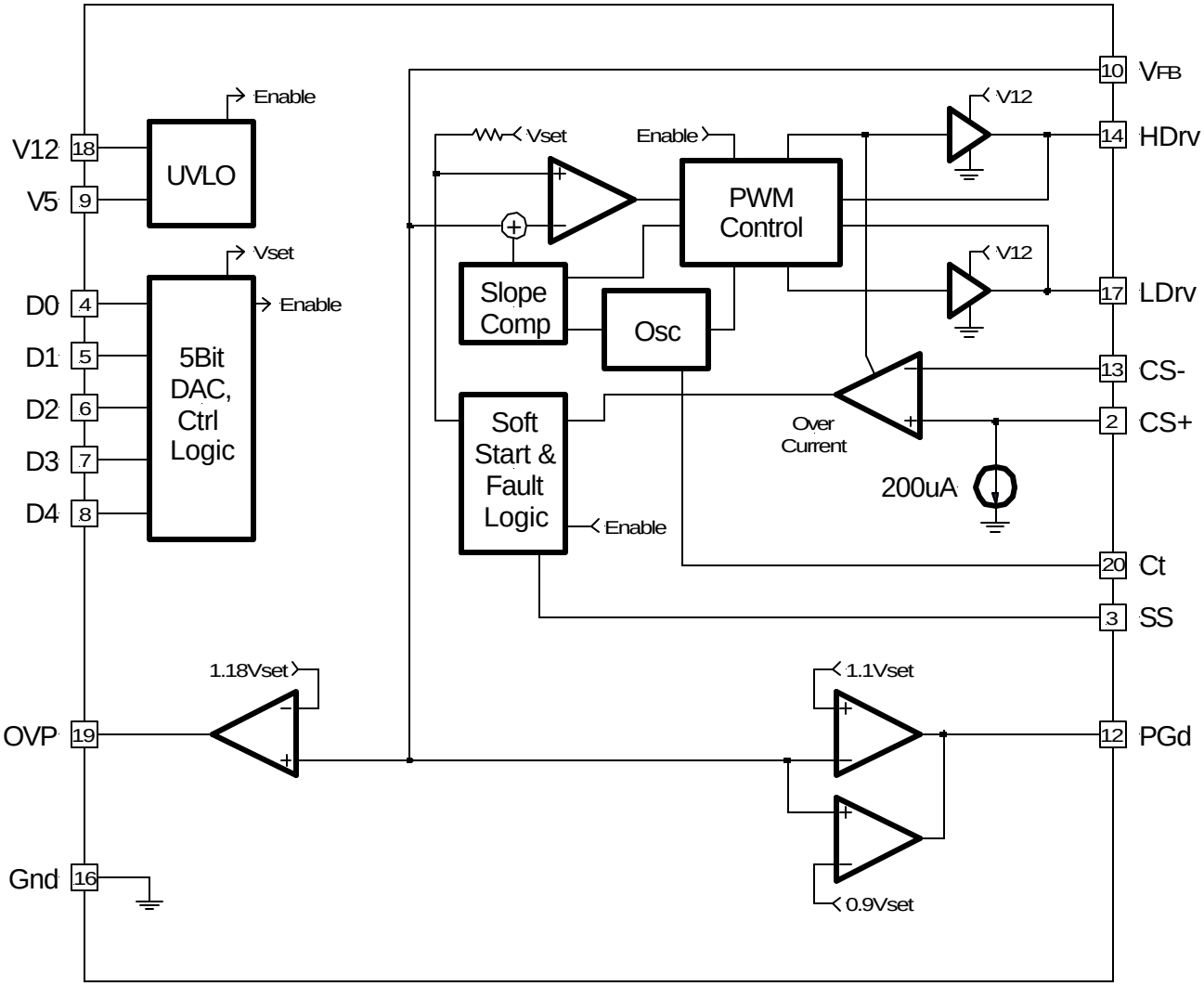


Figure 2 - Simplified block diagram of the IRU3011.

TYPICAL APPLICATION

Synchronous Operation

(Dual Layout with HIP6004B)

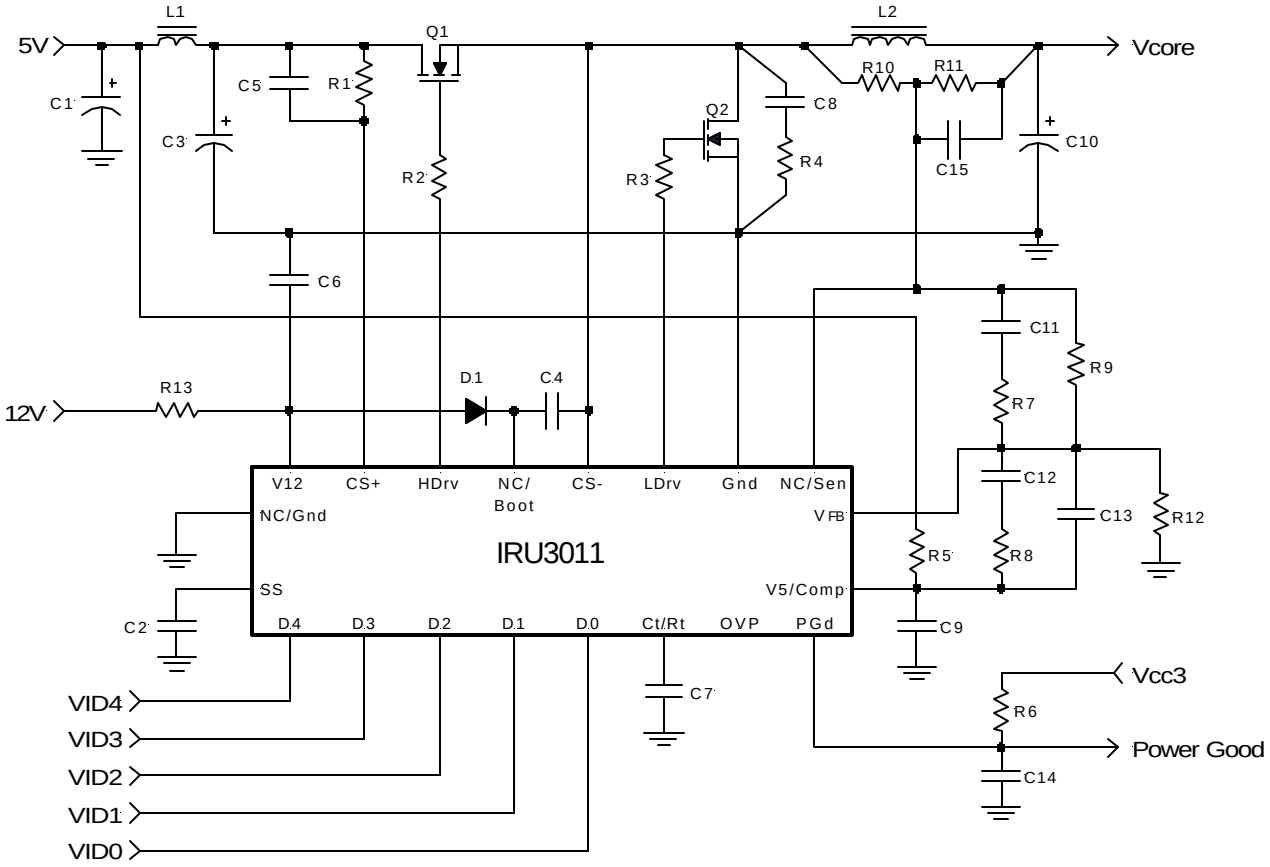


Figure 3 - Typical application of IRU3011 in an on board DC-DC converter providing the Core supply for microprocessor.

Part #	R5	R7	R8	R9	C4	C7	C9	C11	C12	C13	D1
HIP6004B	O	V	V	V	V	O	O	V	V	V	V
IRU3011	S	O	O	V	O	V	V	O	O	O	O

S - Short O - Open V - See IR or Harris parts list for the value

Table 2 - Components that need to be modified to make the dual layout work for IRU3011and HIP6004B.

IRU3011 and HIP6004B Dual Layout Parts List

Ref Desig	Description	Qty	Part #	Manuf
Q1	MOSFET	1	IRL3103s, TO-263 package	IR
Q2	MOSFET	1	IRL3103D1S, TO-263 package	IR
L1	Inductor	1	L=1μH, 5052 core with 4 turns of 1.0mm wire	Micro Metal
L2	Inductor	1	L=2.7μH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1	Capacitor, Electrolytic	1	10MV470GX, 470μF, 10V	Sanyo
C2, 9	Capacitor, Ceramic	2	1μF, 0603	
C3	Capacitor, Electrolytic	2	10MV1200GX, 1200μF, 10V	Sanyo
C5	Capacitor, Ceramic	1	220pF, 0603	
C6	Capacitor, Ceramic	1	1μF, 0805	
C7	Capacitor, Ceramic	1	150pF, 0603	
C8	Capacitor, Ceramic	1	1000pF, 0603	
C10	Capacitor, Electrolytic	6	6MV1500GX, 1500μF, 6.3V	Sanyo
C14	Capacitor, Ceramic	1	0.1μF, 0603	
C15	Capacitor, Ceramic	1	4.7μF, 1206	
R1	Resistor	1	3.3KΩ, 5%, 0603	
R2, 3, 4	Resistor	3	4.7Ω, 5%, 1206	
R5	Resistor	1	0Ω, 0603	
R6	Resistor	1	10KΩ, 5%, 0603	
R9	Resistor	1	100Ω, 1%, 0603	
R10	Resistor	1	220Ω, 1%, 0603	
R11	Resistor	1	330Ω, 1%, 0603	
R12	Resistor	1	22KΩ, 1%, 0603	
R13	Resistor	1	10Ω, 5%, 0603	

Note 1: R10, R11, C15, R9, and R12 set the Vcore 2% higher for level shift to reduce CPU transient voltage.

APPLICATION INFORMATION

An example of how to calculate the components for the application circuit is given below.

Assuming, two sets of output conditions that this regulator must meet,

a) Vo=2.8V, Io=14.2A, ΔVo=185mV, ΔIo=14.2A
b) Vo=2V, Io=14.2A, ΔVo=140mV, ΔIo=14.2A

the regulator design will be done such that it meets the worst case requirement of each condition.

Output Capacitor Selection

The first step is to select the output capacitor. This is done primarily by selecting the maximum ESR value that meets the transient voltage budget of the total ΔVo specification. Assuming that the regulators DC initial accuracy plus the output ripple is 2% of the output voltage, then the maximum ESR of the output capacitor is calculated as:

$$ESR \leq \frac{100}{14.2} = 7m\Omega$$

The Sanyo MVGX series is a good choice to achieve both the price and performance goals. The 6MV1500GX, 1500μF, 6.3V has an ESR of less than 36mΩ typical. Selecting 6 of these capacitors in parallel has an ESR of ≈ 6mΩ which achieves our low ESR goal.

Other type of electrolytic capacitors from other manufacturers to consider are the Panasonic FA series or the Nichicon PL series.

Reducing the Output Capacitors Using Voltage Level Shifting Technique

The trace resistance or an external resistor from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transitioning from light load to full load and vice versa. To accomplish this, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the Gnd pin of the device is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70mV or 35mV higher than the DAC voltage setting.

This intentional voltage level shifting during the load transient eases the requirement for the output capacitor ESR at the cost of load regulation. One can show that the new ESR requirement eases up by half the total trace resistance. For example, if the ESR requirement of the output capacitors without voltage level shifting must be 7mΩ then after level shifting the new ESR will only need to be 8.5mΩ if the trace resistance is 5mΩ (7 + 5/2=9.5). However, one must be careful that the combined "voltage level shifting" and the transient response is still within the maximum tolerance of the Intel specification. To insure this, the maximum trace resistance must be less than:

$$Rs \leq 2 \times (Vspec - 0.02 \times Vo - \Delta Vo) / \Delta I$$

Where :
Rs = Total maximum trace resistance allowed
Vspec = Intel total voltage spec
Vo = Output voltage
ΔVo = Output ripple voltage
ΔI = load current step

For example, assuming:
Vspec = ±140mV = ±0.1V for 2V output
Vo = 2V
ΔVo = assume 10mV = 0.01V
ΔI = 14.2A

Then the Rs is calculated to be:

$$Rs \leq 2 \times (0.140 - 0.02 \times 2 - 0.01) / 14.2 = 12.6m\Omega$$

However, if a resistor of this value is used, the maximum power dissipated in the trace (or if an external resistor is being used) must also be considered. For example if Rs=12.6mΩ, the power dissipated is:

$$Io^2 \times Rs = 14.2^2 \times 12.6 = 2.54W$$

This is a lot of power to be dissipated in a system. So, if the Rs=5mΩ, then the power dissipated is about 1W which is much more acceptable. If level shifting is not implemented, then the maximum output capacitor ESR was shown previously to be 7mΩ which translated to ≈ 6 of the 1500μF, 6MV1500GX type Sanyo capacitors. With Rs=5mΩ, the maximum ESR becomes 9.5mΩ which is equivalent to ≈ 4 caps. Another important consideration is that if a trace is being used to implement the resistor, the power dissipated by the trace increases the case temperature of the output capacitors which could seriously effect the life time of the output capacitors.

Output Inductor Selection
The output inductance must be selected such that under low line and the maximum output voltage condition, the inductor current slope times the output capacitor ESR is ramping up faster than the capacitor voltage is drooping during a load current step. However, if the inductor is too small, the output ripple current and ripple voltage become too large. One solution to bring the ripple current down is to increase the switching frequency, however, that will be at the cost of reduced efficiency and higher system cost. The following set of formulas are derived to achieve the optimum performance without many design iterations.

The maximum output inductance is calculated using the following equation:

$$L = ESR \times C \times (V_{IN(MIN)} - Vo_{(MAX)}) / (2 \times \Delta I)$$

Where:
$V_{IN(MIN)}$ = Minimum input voltage
For Vo=2.8V and ΔI=14.2A

$$L = 0.006 \times 9000 \times (4.75 - 2.8) / (2 \times 14.2) = 3.7\mu H$$

Assuming that the programmed switching frequency is set at 200KHz, an inductor is designed using the Micrometals' powder iron core material. The summary of the design is outlined below:

The selected core material is Powder Iron, the selected core is T50-52D from Micro Metal wounded with 8 turns of #16 AWG wire, resulting in 3µH inductance with ≈ 3mΩ of DC resistance.

Assuming L=3µH and Fsw=200KHz(switching frequency), the inductor ripple current and the output ripple voltage is calculated using the following set of equations:

T ≡ Switching Period
D ≡ Duty Cycle
Vsw ≡ High-side MOSFET ON Voltage
R_{DS} ≡ MOSFET On-Resistance
Vsync ≡ Synchronous MOSFET ON Voltage
ΔIr ≡ Inductor Ripple Current
ΔVo ≡ Output Ripple Voltage

$$T = 1/Fsw$$

$$Vsw = Vsync = Io \times R_{DS}$$

$$D \approx (Vo + Vsync) / (V_{IN} - Vsw + Vsync)$$

$$T_{ON} = D \times T$$

$$T_{OFF} = T - T_{ON}$$

$$\Delta Ir = (Vo + Vsync) \times T_{OFF} / L$$

$$\Delta Vo = \Delta Ir \times ESR$$

In our example for Vo=2.8V and 14.2A load, assuming IRL3103 MOSFET for both switches with maximum on resistance 0f 19mΩ, we have:

$$T = 1 / 200000 = 5\mu s$$
$$Vsw = Vsync = 14.2 \times 0.019 = 0.27V$$
$$D \cong (2.8 + 0.27) / (5 - 0.27 + 0.27) = 0.61$$
$$T_{ON} = 0.61 \times 5 = 3.1\mu s$$
$$T_{OFF} = 5 - 3.1 = 1.9\mu s$$
$$\Delta Ir = (2.8 + 0.27) \times 1.9 / 3 = 1.94A$$
$$\Delta Vo = 1.94 \times 0.006 = 0.011V = 11mV$$

Power Component Selection
Assuming IRL3103 MOSFETs as power components, we will calculate the maximum power dissipation as follows:

For high-side switch the maximum power dissipation happens at maximum Vo and maximum duty cycle.

$$D_{MAX} \cong (2.8 + 0.27) / (4.75 - 0.27 + 0.27) = 0.65$$
$$P_{DH} = D_{MAX} \times Io^2 \times R_{DS(MAX)}$$
$$P_{DH} = 0.65 \times 14.2^2 \times 0.029 = 3.8W$$

$R_{DS(MAX)}$ = Maximum $R_{DS(ON)}$ of the MOSFET at 125°C
For synch MOSFET, maximum power dissipation happens at minimum Vo and minimum duty cycle.

$$D_{MIN} \cong (2 + 0.27) / (5.25 - 0.27 + 0.27) = 0.43$$
$$P_{DS} = (1 - D_{MIN}) \times Io^2 \times R_{DS(MAX)}$$
$$P_{DS} = (1 - 0.43) \times 14.2^2 \times 0.029 = 3.33W$$

Heat Sink Selection
Selection of the heat sink is based on the maximum allowable junction temperature of the MOSFETS. Since we previously selected the maximum $R_{DS(ON)}$ at 125°C, then we must keep the junction below this temperature. Selecting TO-220 package gives θ_{JC}=1.8°C/W (From the venders' data sheet) and assuming that the selected heat sink is black anodized, the heat-sink-to-case thermal resistance is θcs=0.05°C/W, the maximum heat sink temperature is then calculated as:

$$Ts = T_J - P_D \times (\theta_{JC} + \theta cs)$$
$$Ts = 125 - 3.82 \times (1.8 + 0.05) = 118°C$$

With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance (θ_{SA}) is calculated as follows:

Assuming T_A = 35°C:

$$\Delta T = Ts - T_A = 118 - 35 = 83°C$$
Temperature Rise Above Ambient

$$\theta_{SA} = \Delta T / P_D = 83 / 3.82 = 22°C/W$$

Next, a heat sink with lower θ_{SA} than the one calculated in the previous step must be selected. One way to do this is to simply look at the graphs of the "Heat Sink Temp Rise Above the Ambient" vs. the "Power Dissipation" given in the heat sink manufacturers' catalog and select a heat sink that results in lower temperature rise than the one calculated in previous step. The following AAVID and Thermalloy heat sinks, meet this criteria.

Co.	Part #
Thermalloy	6078B
AAVID	577002

Following the same procedure for the Schottky diode results in a heatsink with θ_{SA}=25°C/W. Although it is possible to select a slightly smaller heatsink, for simplicity the same heatsink as the one for the high side MOSFET is also selected for the synchronous MOSFET.

Switcher Current Limit Protection

The PWM controller uses the MOSFET $R_{DS(ON)}$ as the sensing resistor to sense the MOSFET current and compares to a programmed voltage which is set externally via a resistor (Rcs) placed between the drain of the MOSFET and the "CS+" terminal of the IC as shown in the application circuit. For example, if the desired current limit point is set to be 22A and from our previous selection, the maximum MOSFET $R_{DS(ON)}$=19mΩ, then the current sense resistor, Rcs is calculated as:

$$Vcs = I_{CL} \times R_{DS} = 22 \times 0.019 = 0.418V$$

$$Rcs = Vcs / I_B = (0.418V) / (200\mu A) = 2.1K\Omega$$

Where:
I_B = 200μA is the internal current setting of the IRU3011

Switcher Timing Capacitor Selection

The switching frequency can be programmed using an external timing capacitor. The value of Ct can be approximated using the equation below:

$$Fsw \approx \frac{3.5 \times 10^{-5}}{Ct}$$

Where:
Ct = Timing Capacitor
F_{SW} = Switching Frequency

If, F_{SW} = 200KHz:

$$Ct \approx \frac{3.5 \times 10^{-5}}{200 \times 10^{3}} = 175pF$$

Switcher Output Voltage Adjust

As it was discussed earlier, the trace resistance from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transitioning from light load to full load and vice versa. To account for the DC drop, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the Gnd pin of the device is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70mV or 35mV higher than the DAC voltage setting. To do this, the top resistor of the resistor divider, R_{TOP} is set at 100Ω, and the bottom resistor, R_B is calculated. For example, if DAC voltage setting is for 2.8V and the desired output under light load is 2.835V, then R_B is calculated using the following formula:

$$R_B = 100 \times [V_{DAC} / (Vo - 1.004 \times V_{DAC})] \quad [\Omega]$$

$$R_B = 100 \times [2.8 / (2.835 - 1.004 \times 2.800)] = 11.76K\Omega$$

Select 11.8KΩ, 1%

Note: The value of the top resistor must not exceed 100Ω. The bottom resistor can then be adjusted to raise the output voltage.

Soft-Start Capacitor Selection

The soft-start capacitor must be selected such that during the start up when the output capacitors are charging up, the peak inductor current does not reach the current limit threshhold. A minimum of 1μF capacitor insures this for most applications. An internal 10μA current source charges the soft-start capacitor which slowly ramps up the inverting input of the PWM comparator V_{FB}3. This insures the output voltage to ramp at the same rate as the soft-start cap thereby limiting the input current. For example, with 1μF and the 10μA internal current source the ramp up rate is (ΔV/Δt)=I/C=1V/100ms. Assuming that the output capacitance is 9000μF, the maximum start up current will be:

$$I = 9000\mu F \times (1V / 100ms) = 0.09A$$

Input Filter

It is recommended to place an inductor between the system 5V supply and the input capacitors of the switching regulator to isolate the 5V supply from the switching noise that occurs during the turn on and off of the switching components. Typically an inductor in the range of 1 to 3μH will be sufficient in this type of application.

Switcher External Shutdown
The best way to shutdown the part is to pull down on the soft-start pin using an external small signal transistor such as 2N3904 or 2N7002 small signal MOSFET. This allows slow ramp up of the output, the same as the power up.

Layout Considerations
Switching regulators require careful attention to the layout of the components, specifically power components since they switch large currents. These switching components can create large amount of voltage spikes and high frequency harmonics if some of the critical components are far away from each other and are connected with inductive traces. The following is a guideline of how to place the critical components and the connections between them in order to minimize the above issues.

Start the layout by first placing the power components:

1) Place the input capacitors C3 and the high side MOSFET, Q1 as close to each other as possible

2) Place the synchronous MOSFETs, Q2 and the Q1 as close to each other as possible with the intention that the connection from the source of Q1 and the drain of the Q2 has the shortest length.

3) Place the snubber R4 & C7 between Q1 & Q2.

4) Place the output inductor, L2 and the output capacitors, C10 between the MOSFET and the load with output capacitors distributed along the slot 1 and close to it.

5) Place the bypass capacitors, C6 and C9 right next to 12V and 5V pins. C6 next to the 12V, pin 18 and C9 next to the 5V, pin 9.

6) Place the IC such that the PWM output drives, pins 14 and 17 are relatively short distance from gates of Q1 and Q2.

7) If the output voltage is to be adjusted, place resistor dividers close to the feedback pin.

   Note: Although, the device does not require resistor dividers and the feedback pin can be directly connected to the output, they can be used to set the outputs slightly higher to account for any output drop at the load due to the trace resistance. See the application note.

8) Place timing capacitor C7 close to pin 20 and soft-start capacitor C2 close to pin 3.

Component connections:

Note: It is extremely important that no data bus should be passing through the switching regulator section specifically close to the fast transition nodes such as PWM drives or the inductor voltage.

Using 4 layer board, dedicate on layer to Gnd, another layer as the power layer for the 5V, 3.3V and Vcore.

Connect all grounds to the ground plane using direct vias to the ground plane.

Use large low inductance/low impedance plane to connect the following connections either using component side or the solder side.

a) C3 to Q1 Drain
b) Q1 Source to Q2 Drain
c) Q2 drain to L2
d) L2 to the output capacitors, C10
e) C10 to the slot 1
f) Input filter L1 to the C3

Connect the rest of the components using the shortest connection possible.

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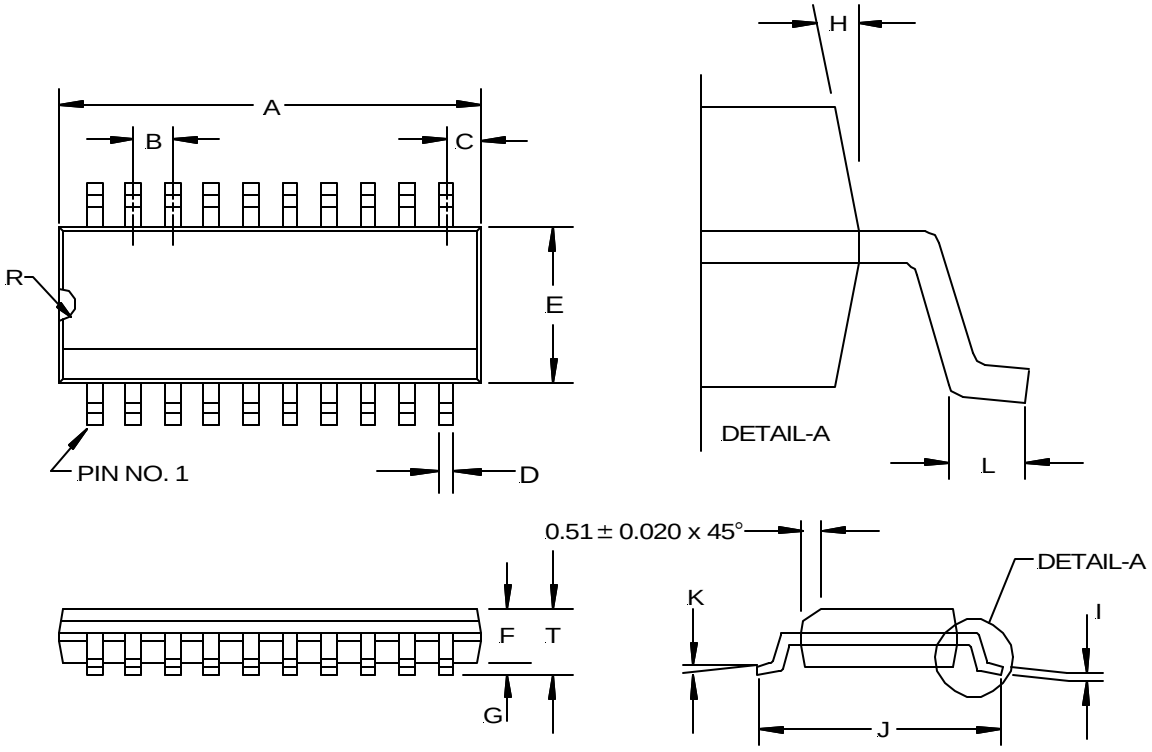
(W) SOIC Package
20-Pin Surface Mount, Wide Body

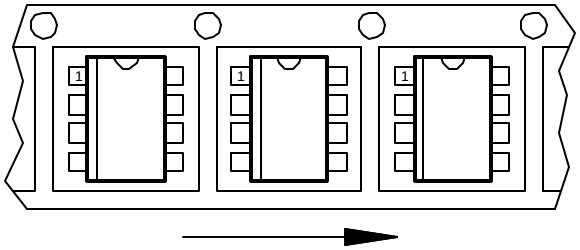


SYMBOL	20-PIN	
	MIN	MAX
A	12.598	12.979
B	1.018	1.524
C	0.66 REF	
D	0.33	0.508
E	7.40	7.60
F	2.032	2.64
G	0.10	0.30
I	0.229	0.32
J	10.008	10.654
K	0°	8°
L	0.406	1.270
R	0.63	0.89
T	2.337	2.642

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
W	SOIC, Wide Body	20	38	1000	Fig A



Feed Direction
Figure A

VRM 8.5 COMPATIBLE 5-BIT PROGRAMMABLE SYNCHRONOUS BUCK CONTROLLER IC WITH TRIPLE LDO CONTROLLER

FEATURES

- Meets Latest VRM 8.5 Specification
- Provides Single Chip Solution for Vcore, 1.2V AGTL+, 1.8V and V_{DDQ}
- On-Board 5-Bit DAC and Decoder programs the output voltage from 1.050V to 1.825V
- Loss-less Short Circuit Protection
- Synchronous operation allows maximum efficiency
- Patented architecture allows fixed frequency operation as well as 100% duty cycle when operating with a changing load
- Minimum Part Count, No External Compensation
- Soft-Start
- High current totem pole driver for directly driving an external Power MOSFET
- Power Good Function

APPLICATIONS

- Pentium III with VRM 8.5 Specification
- DC to DC Converters

DESCRIPTION

The IRU3013 controller IC is specifically designed for Intel Pentium III™ microprocessor applications as described in the VRM 8.5 specification. **The IC provides a single chip solution for the Vcore, 1.2V AGTL+, 1.8V and a third uncommitted LDO controller that can be used either as 1.2V power good detector or to provide 1.5V AGP bus in applications that this voltage is required.** The IRU3013 features a patented topology that, in combination with a few external components, (*Note: See application current in Figure 3) will provide in excess of 30A of output current for an on-board Vcore synchronous converter while automatically providing the output voltage specified in VRM 8.5 specification. The IRU3013 also features, **loss-less current sensing by using the $R_{DS(ON)}$ of the high side Power MOSFET as the sensing resistor**, a Power Good window comparator that switches its open collector output low when the output is outside of a ±10% window. Other features of the device are: Under-voltage lockout for both 5V and 12V supplies, an external programmable soft-start function, and the ability to program the oscillator frequency by connecting an external capacitor.

TYPICAL APPLICATION

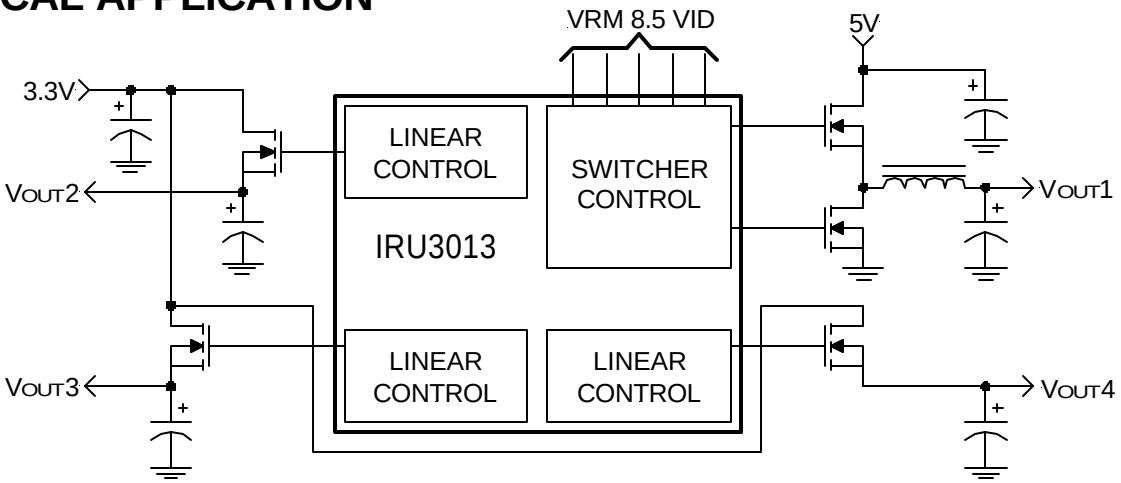


Figure 1 - Typical application of IRU3013.

Note: Pentium III is trade mark of Intel Corp.

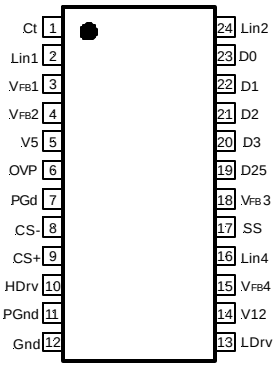
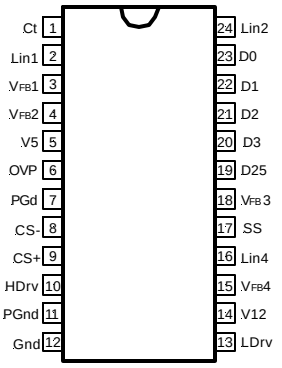
PACKAGE ORDER INFORMATION

T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3013CQ	24-Pin Plastic QSOP NB (Q)
0 To 70	IRU3013CW	24-Pin Plastic SOIC WB (W)

ABSOLUTE MAXIMUM RATINGS

V5 Supply Voltage 10V
V12 Supply Voltage 20V
All Other Pins 7V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

24-PIN PLASTIC QSOP (Q)	24-PIN WIDE BODY PLASTIC SOIC (W)
	
θ_{JA}=88°C/W	θ_{JA}=80°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V12=12V, V5=5V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
VID Section						
DAC Output Voltage (Note 1)			0.98Vs	Vs	1.02Vs	V
DAC Output Line Regulation		4.5<Vcc<5.5 10.5<V12<13V		0.2		%
DAC Output Temp Variation				0.5		%
VID Input LO					0.4	V
VID Input HI			2			V
VID Input Internal Pull-up Resistor to 5V				27		KΩ
Power Good Section						
Under-Voltage Lower Trip Point		V_{OUT} Ramping Down		0.90Vs		V
Under-Voltage Upper Trip Point		V_{OUT} Ramping Up		0.92Vs		V
UV Hysteresis				0.02Vs		V
Over-Voltage Upper Trip Point		V_{OUT} Ramping Up		1.10Vs		V
Over-Voltage Lower Trip Point		V_{OUT} Ramping Down		1.08Vs		V
OV Hysterises				0.02Vs		V
Power Good Output LO		R_L= 3mA		0.3		V
Power Good Output HI		R_L= 5K Pull-Up to 5V		4.95		V
Soft-Start Section						
Soft-Start Current		CS+ = 0V, CS- = 5V		10		µA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
UVLO Section						
UVLO Threshold - 12V		Supply Ramping Up		9		V
UVLO Hysteresis - 12V				0.5		V
UVLO Threshold - 5V		Supply Ramping Up		4		V
UVLO Hysteresis - 5V				0.3		V
Error Comparator Section						
Input Offset Voltage			-2		+2	mV
Delay to Output		V_{DIFF} = 10mV			100	ns
Current Limit Section						
CS Threshold Set Current			120	150	200	µA
CS Comp Offset Voltage			-5		+5	mV
Hiccup Duty Cycle		Css = 0.1µF			2	%
Supply Current Section						
Operating Supply Current		C_L = 3000pF				
		V5		20		
		V12		14		mA
Output Drivers Section						
Rise Time		C_L = 3000pF		70	100	ns
Fall Time		C_L = 3000pF		70	130	ns
Dead Band Time		C_L = 3000pF		200		ns
Oscillator Section						
Osc Frequency		Ct = 150pF		220		KHz
Osc Valley					0.2	V
Osc Peak				V5		V
LDO Controller Section						
V_{FB}1 and V_{FB}2 (Pins 3 and 4)				1.200		
V_{FB}4 (Pin 15)				0.800		V
Input Bias Current					2	µA
Lin 1, 2, 3 Drive Current				30		mA
OVP Section						
OVP Threshold				1.17Vs		V
OVP Source Current				5		mA

Note: Vs refers to the set point voltage given in table 1.

D25	D3	D2	D1	D0	Vs
0	1	1	1	1	1.300
0	1	1	1	0	1.350
0	1	1	0	1	1.400
0	1	1	0	0	1.450
0	1	0	1	1	1.500
0	1	0	1	0	1.550
0	1	0	0	1	1.600
0	1	0	0	0	1.650
0	0	1	1	1	1.700
0	0	1	1	0	1.750
0	0	1	0	1	1.800
0	0	1	0	0	1.050
0	0	0	1	1	1.100
0	0	0	1	0	1.150
0	0	0	0	1	2.200
0	0	0	0	0	2.250

D25	D3	D2	D1	D0	Vs
1	1	1	1	1	1.325
1	1	1	1	0	1.375
1	1	1	0	1	1.425
1	1	1	0	0	1.475
1	1	0	1	1	1.525
1	1	0	1	0	1.575
1	1	0	0	1	1.625
1	1	0	0	0	1.675
1	0	1	1	1	1.725
1	0	1	1	0	1.775
1	0	1	0	1	1.825
1	0	1	0	0	1.075
1	0	0	1	1	1.125
1	0	0	1	0	1.175
1	0	0	0	1	1.225
1	0	0	0	0	1.275

Table 1 - Set point voltage vs. VID codes.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Ct	This pin programs the oscillator frequency in the range of 50 KHz to 500KHz by means of an external capacitor connected from this pin to the ground.
2	Lin1	Controls the gate of an external MOSFET for the AGTL+ linear regulator or 1.8V supply.
3	$V_{FB}1$	This pin provides the feedback for the linear regulator that its output drive is Lin1 pin.
4	$V_{FB}2$	This pin provides the feedback for the linear regulator that its output drive is Lin2 pin.
5	V5	5V supply voltage.
6	OVP	This pin provides an over voltage flag when the feedback pin $V_{FB}3$ voltage exceeds 17%(Typical) of the set point for the Vcore output.
7	PGd	This pin is an open collector output that switches LO when the output of the converter is not within ±10% (typ) of the nominal output voltage. When PGd pin switches LO the output saturation voltage is less than 0.4V at 3mA.
8	CS-	This pin is connected to the Source of the power MOSFET for the Core supply and it is the negative input for the internal current sensing circuitry.
9	CS+	This pin is connected to the Drain of the power MOSFET of the Core supply. It provides the positive sensing input for the internal current sensing circuitry. An external resistor programs the CS threshold depending on the R_{DS} of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.
10	HDrv	Output driver for the high side power MOSFET.
11	PGnd	This is the power ground pin and must be connected directly to the gnd plane close to the source of the synchronous MOSFET. A high frequency capacitor (typically 1µF) must be connected from V12 pin to this pin for noise free operation.
12	Gnd	This pin must be connected directly to the ground plane. A high frequency capacitor (0.1 to 1µF) must be connected from V5 and V12 pins to this pin for noise free operation.
13	LDrv	Output driver for the power MOSFET, which is used as a synchronous switched rectifier.
14	V12	This pin is connected to the 12V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (0.1 to 1µF) must be connected directly from this pin to Gnd pin in order to supply large instantaneous current pulses to the power MOSFET during the transitions.
15	$V_{FB}4$	This pin provides the feedback for the linear regulator that its output drive is Lin4 pin.
16	Lin4	This pin controls the gate of an external MOSFET for either the AGP Bus linear regulator or can be used as Power good detector for 1.2V AGTL+ bus.
17	SS	This pin provides the soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to the ground which ramps up the outputs of the switching regulator, preventing the outputs from overshooting as well as limiting the inrush current. The second function of the Soft-Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting.
18	$V_{FB}3$	This pin is connected directly to the output of the Core supply to provide feedback to the Error comparator.
19	D25	This pin programs the output voltage in 25mV steps based on the VID table. 40K internal pull-up to Vcc.
20	D3	MSB input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10K resistor to either 3.3V or 5V supply. 40K internal pull-up to Vcc.
21	D2	Input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10K resistor to either 3.3V or 5V supply. 40K internal pull-up to Vcc.
22	D1	Input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10KΩ resistor to either 3.3V or 5V supply. 40K internal pull-up to Vcc.
23	D0	LSB input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10K resistor to either 3.3V or 5V supply. 40K internal pull-up to Vcc.
24	Lin2	Controls the gate of an external MOSFET for the AGTL+ linear regulator or 1.8V supply.

BLOCK DIAGRAM

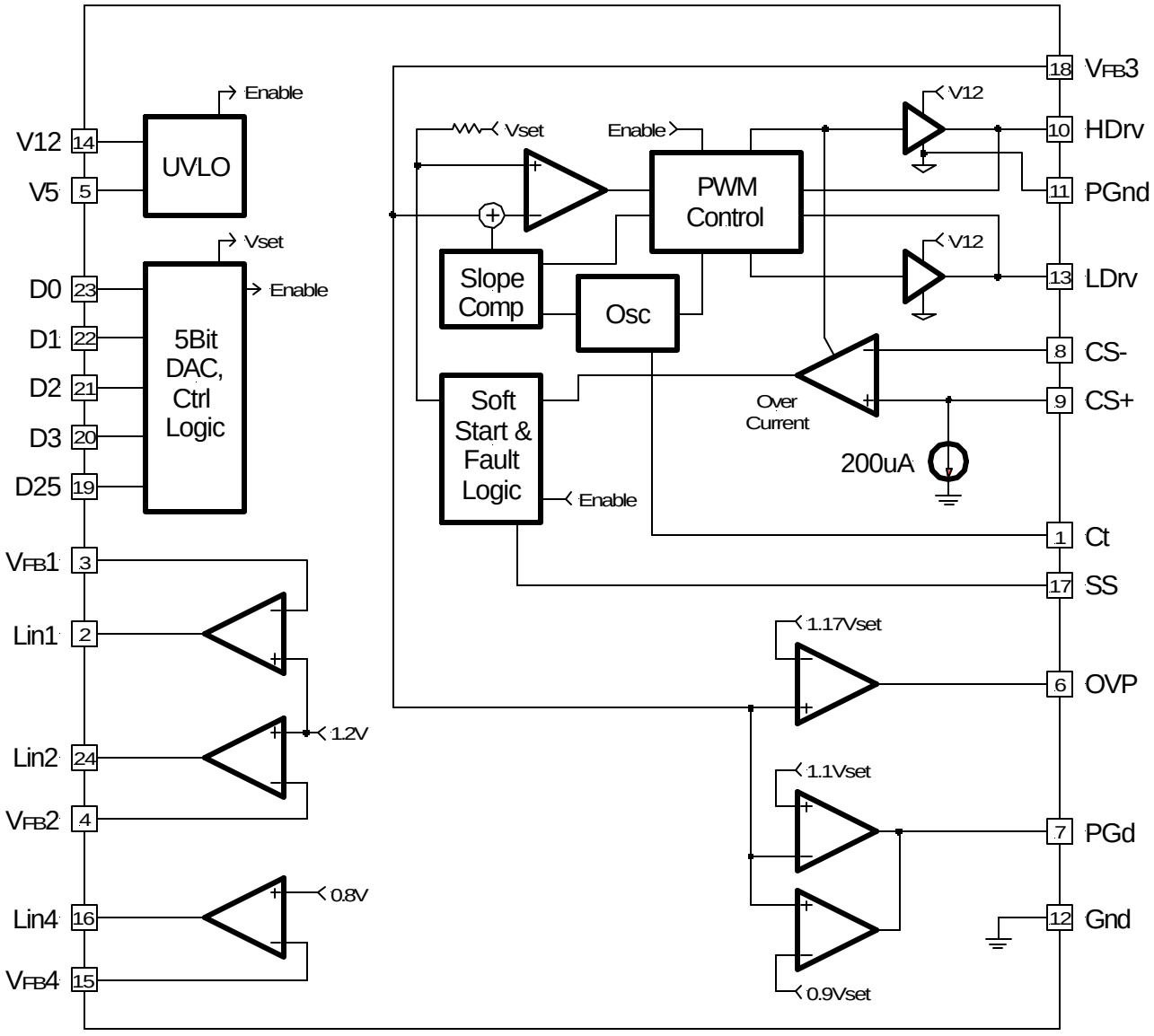
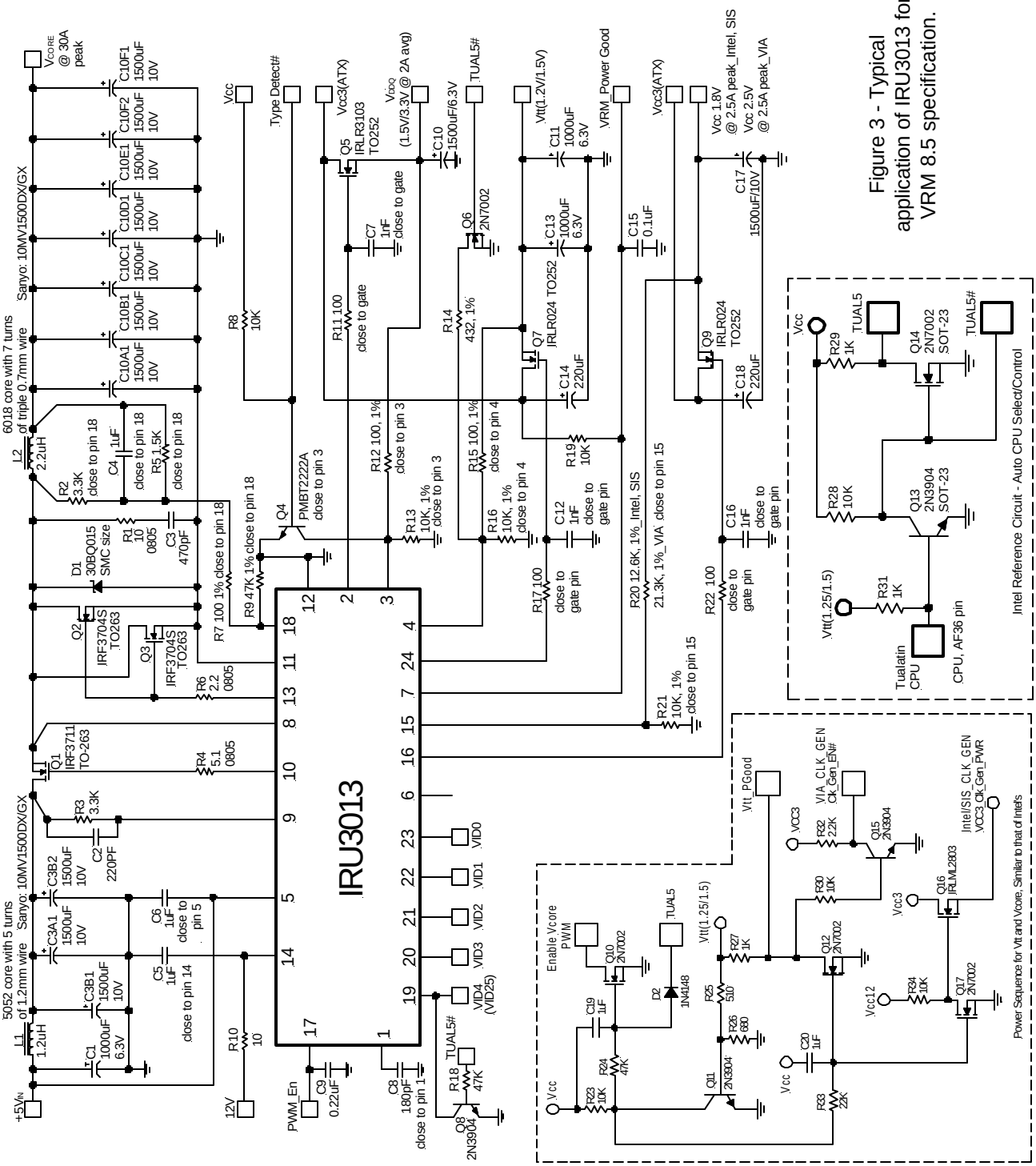


Figure 2 - Simplified block diagram of the IRU3013.

TYPICAL APPLICATION



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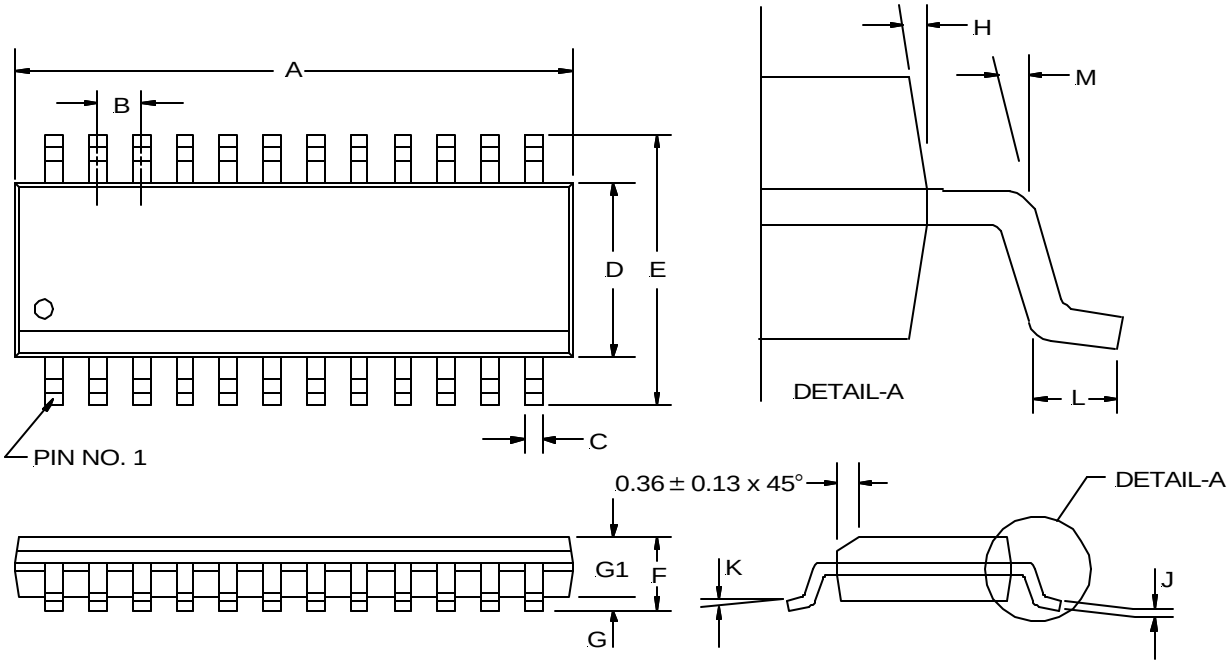
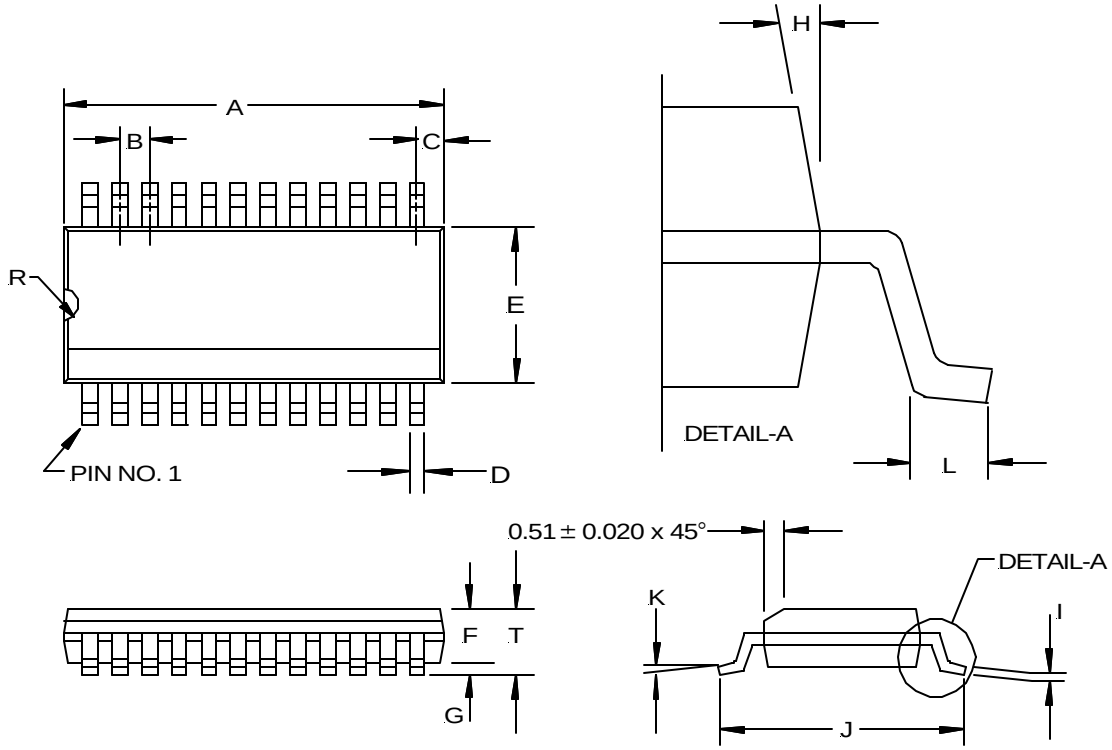
(Q) QSOP Package, Narrow Body
24-Pin



24-PIN		
SYMBOL	**MIN**	**MAX**
A	8.55	8.74
B	0.635 BSC	
C	0.20	0.30
D	3.81	3.99
E	5.79	6.20
F	1.35	1.75
G	0.10	0.25
G1	1.37	1.57
H	9° BSC	
J	0.19	0.25
K	0°	8°
L	0.40	1.27
M	7° ± 3°	

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

(W) SOIC Package
24-Pin Surface Mount, Wide Body

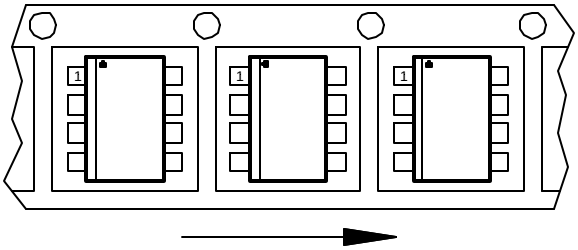


SYMBOL	24-PIN	
	MIN	MAX
A	15.20	15.40
B	1.27 BSC	
C	0.66 REF	
D	0.36	0.46
E	7.40	7.60
F	2.44	2.64
G	0.10	0.30
I	0.23	0.32
J	10.11	10.51
K	0°	8°
L	0.51	1.01
R	0.63	0.89
T	2.44	2.64

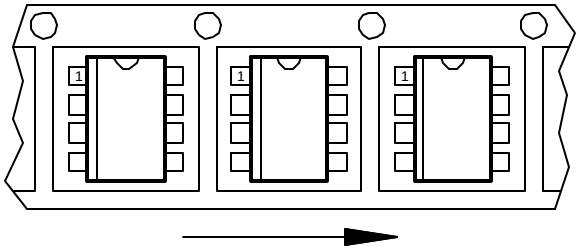
NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
Q	QSOP Plastic, Narrow Body	24	---	1500	Fig A
W	SOIC, Wide Body	24	31	1000	Fig B



Feed Direction
Figure A



Feed Direction
Figure B

International
IOR Rectifier

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5-BIT PROGRAMMABLE SYNCHRONOUS BUCK CONTROLLER IC, LDO CONTROLLER AND 200mA ON-BOARD LDO REGULATOR

FEATURES

- Provides single chip solution for Vcore, GTL+ & clock supply
- 200mA On-Board LDO Regulator
- Designed to meet the latest Intel specification for Pentium II™
- On-Board DAC programs the output voltage from 1.3V to 3.5V
- Linear regulator controller on board for 1.5V GTL+ supply
- Loss-less Short Circuit Protection with HICCUP
- Synchronous operation allows maximum efficiency patented architecture allows fixed frequency operation as well as 100% duty cycle during dynamic load
- Soft-Start
- High current totem pole driver for direct driving of the external power MOSFET
- Power Good Function monitors all outputs
- Over-Voltage Protection circuitry protects the switcher output and generates a fault signal
- Thermal Shutdown
- Logic Level Enable Input

APPLICATIONS

- Total Power Solution for Pentium II processor application

DESCRIPTION

The IRU3018 controller IC is specifically designed to meet Intel specification for Pentium II™ microprocessor applications as well as the next generation of P6 family processors. The IRU3018 provides a single chip controller IC for the Vcore, LDO controller for GTL+ and an internal 200mA regulator for clock supply which are required for the Pentium II applications. These devices feature a patented topology that in combination with a few external components as shown in the typical application circuit, will provide in excess of 18A of output current for an on-board DC-DC converter while automatically providing the right output voltage via the 5-bit internal DAC. The IRU3018 also features loss-less current sensing for both switchers by using the $R_{DS(ON)}$ of the high-side power MOSFET as the sensing resistor, internal current limiting for the clock supply, and a Power Good window comparator that switches its open collector output low when any one of the outputs is outside of a pre-programmed window. Other features of the device are: Under-voltage lockout for both 5V and 12V supplies, an external programmable soft-start function, programming the oscillator frequency via an external resistor, Over-Voltage Protection (OVP) circuitry for both switcher outputs and an internal thermal shutdown.

TYPICAL APPLICATION

Note: Pentium II is trademark of Intel Corp

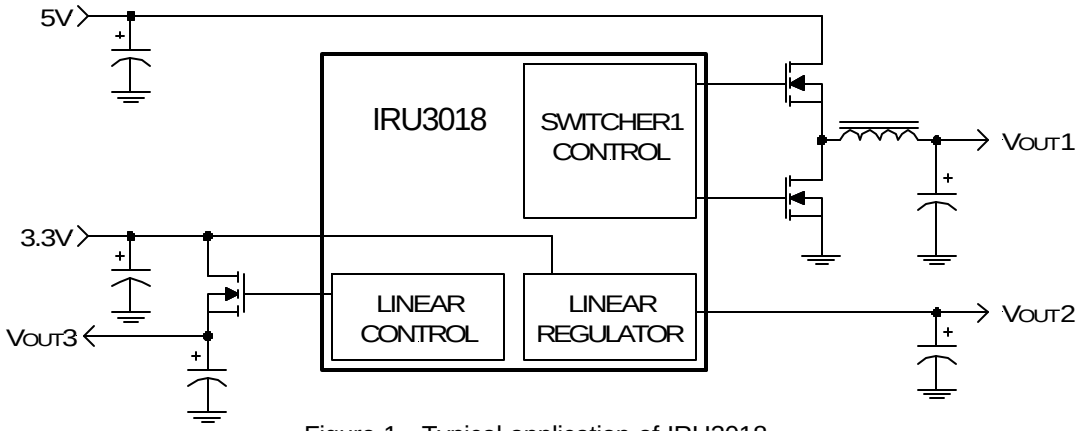


Figure 1 - Typical application of IRU3018.

PACKAGE ORDER INFORMATION

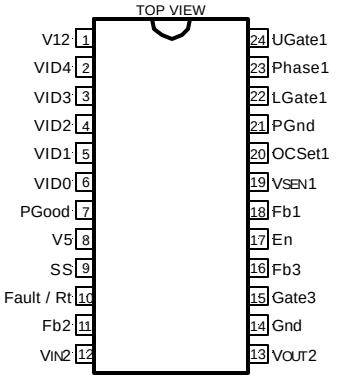
T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3018CW	24-Pin Plastic SOIC WB (W)

ABSOLUTE MAXIMUM RATINGS

V5 Supply Voltage 7V
V12 Supply Voltage 20V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

24-PIN WIDE BODY PLASTIC SOIC (W)



θ_{JA} =80°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V12=12V, V5=5V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply UVLO Section						
UVLO Threshold-12V		Supply Ramping Up		10		V
UVLO Hysteresis-12V				0.4		V
UVLO Threshold-5V		Supply Ramping Up		4.3		V
UVLO Hysteresis-5V				0.3		V
Supply Current						
Operating Supply Current	I_{12}	V12		6		mA
	I_5	V5		20		
Switching Controllers; Vcore (V_{OUT}1)						
VID Section						
DAC Output Voltage (Note 1)	V_{DAC}		0.99Vs	Vs	1.01Vs	V
DAC Output Line Regulation				0.1		%
DAC Output Temp Variation				0.5		%
VID Input LO					0.8	V
VID Input HI			2			V
VID Input Internal Pull-Up Resistor to V5				27		KΩ
Error Comparator Section						
Input Bias Current					2	µA
Input Offset Voltage			-2		+2	mV
Delay to Output		V_{DIFF}=10mV			100	ns
Oscillator Section (Internal)						
Osc Frequency				200		KHz

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Current Limit Section						
CS Threshold Set Current				200		µA
CS Comp Offset Voltage			-5		+5	mV
Hiccup Duty Cycle		Css=0.1µF		10		%
Output Drivers Section						
Rise Time		C_L=3000pF		70		ns
Fall Time		C_L=3000pF		70		ns
Dead Band Time Between High Side and Synch Drive Vcore Switcher Only		C_L=3000pF		200		ns
2.5V Regulator (V_{OUT}2)						
Reference Voltage	V_O2	T_A=25°C, V_{OUT}2=Fb2		1.260		V
Reference Voltage				1.260		V
Dropout Voltage		Io=200mA		0.6		V
Load Regulation		1mA< Io <200mA		0.5		%
Line Regulation		3.1V<V_{IN}2<4V, Vo=2.5V		0.2		%
Input Bias Current					2	µA
Output Current			200			mA
Current Limit			300			mA
Thermal Shutdown				145		°C
1.5V Regulator (V_{OUT}3)						
Reference Voltage	V_O3	T_A=25°C, Gate3=Fb3		1.260		V
Reference Voltage				1.260		V
Input Bias Current					2	µA
Output Drive Current			50			mA
Power Good Section						
Core UV Lower Trip Point		V_{SEN}1 Ramping Down		0.90Vs		V
Core UV Upper Trip Point		V_{SEN}1 Ramping Up		0.92Vs		V
Core UV Hysterises				0.02Vs		V
Core OV Upper Trip Point		V_{SEN}1 Ramping Up		1.10Vs		V
Core OV Lower Trip Point		V_{SEN}1 Ramping Down		1.08Vs		V
Core OV Hysterises				0.02Vs		V
Fb2 Lower Trip Point		Fb2 Ramping Down		0.95		V
Fb2 Upper Trip Point		Fb2 Ramping Up		1.05		V
Fb3 Lower Trip Point		Fb3 Ramping Down		0.95		V
Fb3 Upper Trip Point		Fb3 Ramping Up		1.05		V
Power Good Output LO		R_L=3mA		0.4		V
Power Good Output HI		R_L=5K, Pull-Up to 5V		4.8		V
Fault (Overvoltage) Section						
Core OV Upper Trip Point		V_{SEN}1 Ramping Up		1.17Vs		V
Core OV Lower Trip Point		V_{SEN}1 Ramping Down		1.15Vs		V
V_{IN}2 Upper Trip Point		V_{IN}2 Ramping Up		4.3		V
V_{IN}2 Lower Trip Point		V_{IN}2 Ramping Down		4.2		V
Fault Output HI		Io=3mA		10		V
Soft-Start Section						
Pull-Up Resistor to 5V		OCSet=0V, Phase=5V		23		KΩ
Enable Section						
En Pin Input LO Voltage	$V_{EN(L)}$	Regulator OFF			0.8	V
En Pin Input HI Voltage	$V_{EN(H)}$	Regulator ON	2			V
En Pin Input LO Current		V_{EN}=0V to 0.8V		0.01		µA
En Pin Input HI Current		V_{EN}=2V to 5V		20		µA

Note 1: Vs refers to the set point voltage given in Table 1

D4	D3	D2	D1	D0	Vs
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05

D4	D3	D2	D1	D0	Vs
1	1	1	1	1	2.0
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

Table 1 - Set point voltage vs. VID codes

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	V12	This pin is connected to the 12V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (typically 1μF) must be placed close to this pin and PGnd pin and be connected directly from this pin to the ground plane for noise free operation.
2	VID4	This pin selects a range of output voltages for the DAC. When in the Low state, the range is 1.3V to 2.05V and when it switches to Hi state, the range is 2V to 3.5V. This pin is TTL compatible that realizes a logic “1” as either Hi or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
3	VID3	MSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either Hi or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
4	VID2	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either Hi or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
5	VID1	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either Hi or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
6	VID0	LSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either Hi or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
7	PGood	This pin is an open collector output that switches Low when any of the outputs are outside of the specified under-voltage trip point. It also switches Low when $V_{SEN}1$ pin is more than 10% above DAC voltage setting.
8	V5	5V supply voltage. A high frequency capacitor (0.1 to 1μF) must be placed close to this pin and connected from this pin to the ground plane for noise free operation.
9	SS	This pin provides the soft-start for the switching regulator. An internal resistor charges an external capacitor that is connected from 5V supply to this pin which ramps up the outputs of the switching regulators, preventing the outputs from overshooting as well as limiting the input current. The second function of the soft-start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting.

PIN#	PIN SYMBOL	PIN DESCRIPTION
10	Fault / Rt	This pin has dual function. It acts as an output of the OVP circuitry or it can be used to program the frequency using an external resistor. When used as a fault detector, if the switcher output exceeds the OVP trip point, the Fault pin switches to 12V and the soft-start cap is discharged. If the Fault pin is to be connected to any external circuitry, it needs to be buffered as shown in the application circuit.
11	Fb2	This pin provides the feedback for the internal LDO regulator which its output is $V_{OUT}4$.
12	$V_{IN}2$	This pin is the input that provides power for the internal LDO regulator. It is also monitored for the under-voltage and over-voltage conditions.
13	$V_{OUT}2$	This pin is the output of the internal LDO regulator.
14	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane.
15	Gate3	This pin controls the gate of an external transistor for the 1.5V GTL+ linear regulator.
16	Fb3	This pin provides the feedback for the linear regulator which its output drive is Gate3.
17	En	This pin is a TTL compatible Enable pin. When this pin is left open or pulled high, the device is enabled and when it is pulled low, it will disable the switcher and the LDO controller ($V_{OUT}3$) leaving the internal 200mA regulator operational. When signal is given to enable the device, both switcher and $V_{OUT}3$ will go through soft-start, the same as during start-up.
18	Fb1	This pin provides the feedback for the synchronous switching regulator. Typically this pin can be connected directly to the output of the switching regulator. However, a resistor divider is recommended to be connected from this pin to $V_{OUT}1$ and Gnd to adjust the output voltage for any drop in the output voltage that is caused by the trace resistance. The value of the resistor connected from $V_{OUT}1$ to Fb1 must be less than 100Ω.
19	$V_{SEN}1$	This pin is internally connected to the under-voltage and over-voltage comparators sensing the Vcore status. It must be connected directly to the Vcore supply.
20	OCSet1	This pin is connected to the Drain of the power MOSFET of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the CS threshold depending on the R_{DS} of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.
21	PGnd	This pin serves as the Power ground pin and must be connected directly to the ground plane close to the source of the synchronous MOSFET. A high frequency capacitor (typically 1μF) must be connected from V12 pin to this pin for noise free operation.
22	LGate1	Output driver for the synchronous power MOSFET for the Core supply.
23	Phase1	This pin is connected to the Source of the power MOSFET for the Core supply and it provides the negative sensing for the internal current sensing circuitry.
24	UGate1	Output driver for the high side power MOSFET for the Core supply.

BLOCK DIAGRAM

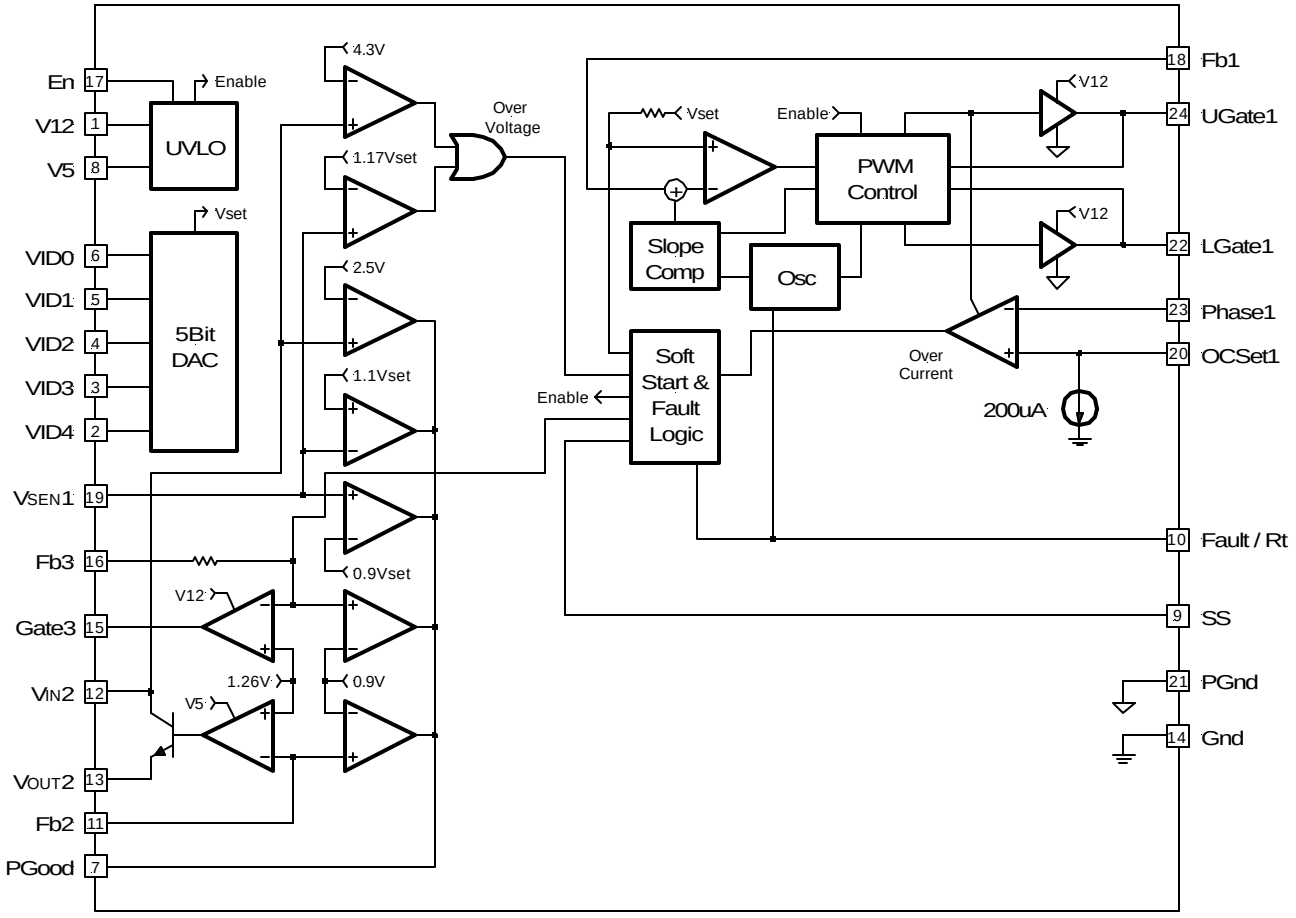


Figure 2 - Simplified block diagram of the IRU3018.

TYPICAL APPLICATION

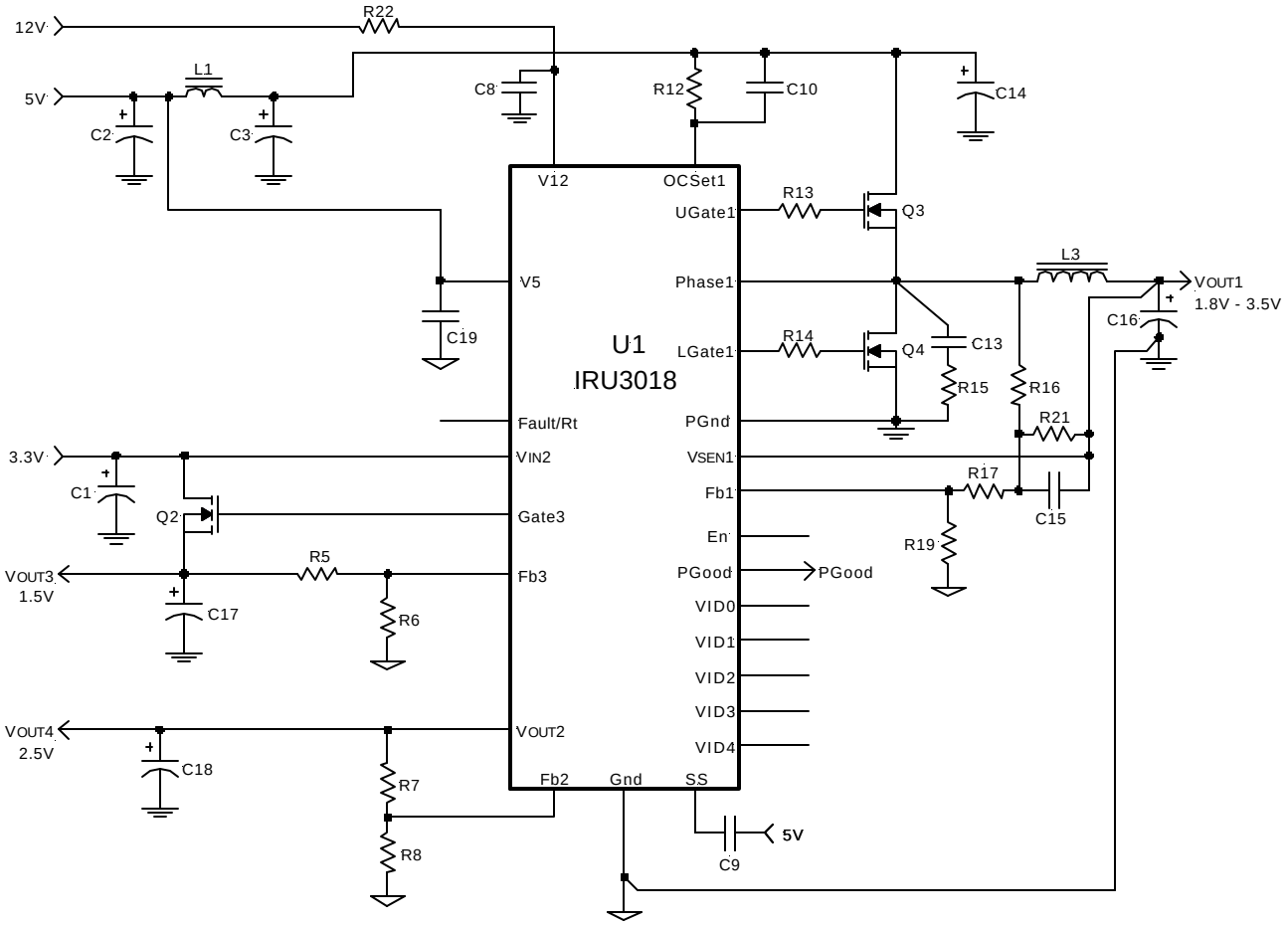


Figure 3 - Typical application of IRU3018 for an on board DC-DC converter providing power for the Vcore, GTL+ & Clock supply for the Deschutes and the next generation processor applications.

IRU3018 APPLICATION PARTS LIST

Ref Desig	Description	Qty	Part #	Manuf
Q2	MOSFET	1	IRLR024, TO-252 package	IR
Q3	MOSFET	1	IRL3103S, TO-263 package	IR
Q4	MOSFET with Schottky	1	IRL3103D1S, TO-263 package	IR
L1	Inductor	1	L=1μH, 5052 core with 4 turns of 1.0mm wire	Micro Metal
L3	Inductor	1	L=2.7μH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1,17	Capacitor, Electrolytic	2	6MV1000GX, 1000μF, 6.3V	Sanyo
C2	Capacitor, Electrolytic	1	10MV470GX, 470μF, 10V	Sanyo
C3	Capacitor, Electrolytic	1	10MV1200GX, 1200μF, 10V	Sanyo
C8	Capacitor, Ceramic	1	1μF, 0805	
C9,15,19	Capacitor, Ceramic	3	1μF, 0603	
C10	Capacitor, Ceramic	1	220pF, 0603	
C13	Capacitor, Ceramic	1	1000pF, 0603	
C14	Capacitor, Electrolytic	2	10MV1200GX, 1200μF, 10V	Sanyo
C16	Capacitor, Electrolytic	6	6MV1500GX, 1500μF, 6.3V	Sanyo
C18	Capacitor, Electrolytic	1	6MV150GX, 150μF, 6.3V	Sanyo
R5	Resistor	1	19.1Ω, 1%, 0603	
R6,7,8	Resistor	3	100Ω, 1%, 0603	
R12	Resistor	1	3.3KΩ, 5%, 0603	
R13,14,15	Resistor	3	4.7Ω, 5%, 1206	
R16,17,21	Resistor	3	2.2KΩ, 1%, 0603	
R22	Resistor	1	10Ω, 5%, 0603	

TYPICAL APPLICATION

(Dual Layout with HIP6018)

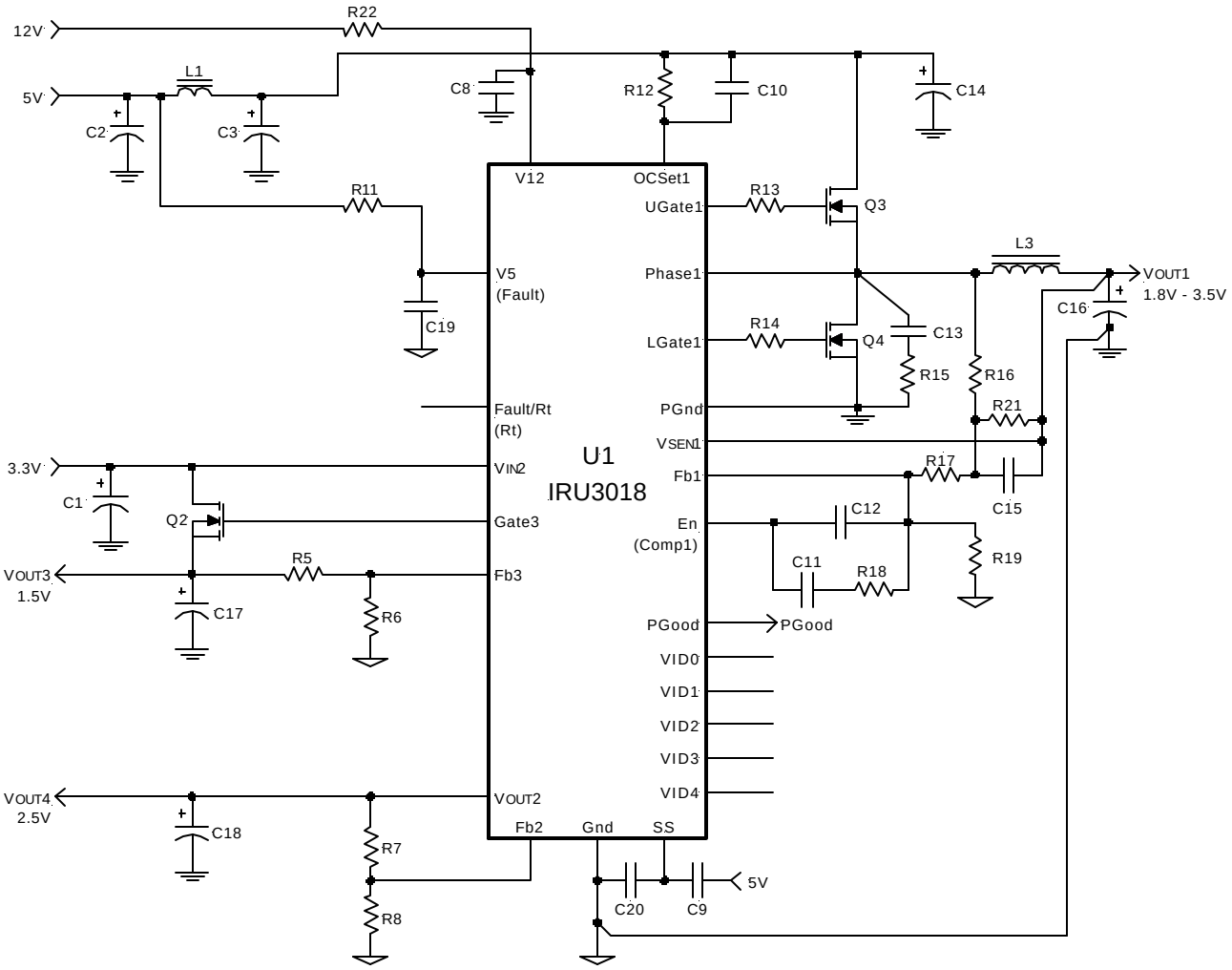


Figure 4 - Typical application of IRU3018 in a dual layout with HIP6018 for an on-board DC-DC converter providing power for the Vcore, GTL+ & Clock supply for the Deschutes and the next generation processor applications.

Part #	R11	R18	C9	C11	C12	C19	C20
HIP6018	O	V	O	V	V	O	V
IRU3018	S	O	V	O	O	V	O

S - Short O - Open V - See IR or Harris parts list for the value

Table 2 - Dual layout component table. Components that need to be modified to make the dual layout work for IRU3018 and HIP6018.

IRU3018 APPLICATION PARTS LIST

Dual Layout with HIP6018

Ref Desig	Description	Qty	Part #	Manuf
Q2	MOSFET	1	IRLR024, TO-252 package	IR
Q3	MOSFET	1	IRL3103S, TO-263 package	IR
Q4	MOSFET with Schottky	1	IRL3103D1S, TO-263 package	IR
L1	Inductor	1	L=1μH, 5052 core with 4 turns of 1.0mm wire	Micro Metal
L3	Inductor	1	L=2.7μH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1,17	Capacitor, Electrolytic	2	6MV1000GX, 1000uF, 6.3V	Sanyo
C2	Capacitor, Electrolytic	1	10MV470GX, 470μF, 10V	Sanyo
C3	Capacitor, Electrolytic	1	10MV1200GX, 1200μF, 10V	Sanyo
C8	Capacitor, Ceramic	1	1μF, 0805	
C9,15,19	Capacitor, Ceramic	3	1μF, 0603	
C10	Capacitor, Ceramic	1	220pF, 0603	
C11,12,20	Capacitor, Ceramic	3	See Table 2, dual layout component 0603 × 3	
C13	Capacitor, Ceramic	1	1000pF, 0603	
C14	Capacitor, Electrolytic	2	10MV1200GX, 1200μF, 10V	Sanyo
C16	Capacitor, Electrolytic	6	6MV1500GX, 1500μF, 6.3V	Sanyo
C18	Capacitor, Electrolytic	1	6MV150GX, 150μF, 6.3V	Sanyo
R5	Resistor	1	19.1Ω, 1%, 0603	
R6,7,8	Resistor	3	100Ω, 1%, 0603	
R11	Resistor	1	0Ω, 0603	
R12	Resistor	1	3.3KΩ, 5%, 0603	
R13,14,15	Resistor	3	4.7Ω, 5%, 1206	
R16,17,21	Resistor	3	2.2KΩ, 1%, 0603	
R18	Resistor	1	See Table 2, dual layout component 0603 × 1	
R19	Resistor	1	220KΩ, 1%, 0603	
R22	Resistor	1	10Ω, 5%, 0603	

APPLICATION INFORMATION

An example of how to calculate the components for the application circuit is given below.

Assuming, two set of output conditions that this regulator must meet for Vcore:

a) Vo=2.8V, Io=14.2A, ΔVo=185mV, ΔIo=14.2A
b) Vo=2V, Io=14.2A, ΔVo=140mV, ΔIo=14.2A

The regulator design will be done such that it meets the worst case requirement of each condition.

Output Capacitor Selection

The first step is to select the output capacitor. This is done primarily by selecting the maximum ESR value that meets the transient voltage budget of the total ΔVo specification. Assuming that the regulators DC initial accuracy plus the output ripple is 2% of the output voltage, then the maximum ESR of the output capacitor is calculated as:

$$ESR \leq \frac{100}{14.2} = 7m\Omega$$

The Sanyo MVGX series is a good choice to achieve both the price and performance goals. The 6MV1500GX, 1500μF, 6.3V has an ESR of less than 36mΩ typical. Selecting 6 of these capacitors in parallel has an ESR of ≈ 6mΩ which achieves our low ESR goal.

Other type of Electrolytic capacitors from other manufacturers to consider are the Panasonic FA series or the Nichicon PL series.

Reducing the Output Capacitors Using Voltage Level Shifting Technique

The trace resistance or an external resistor from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transitioning from light load to full load and vice versa. To accomplish this, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the Gnd pin of the IRU3018 is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70mV or 35mV higher than the DAC voltage setting. This intentional voltage level shifting during the load transient eases the requirement for the output capacitor ESR at the cost of load regulation. One can show that the new ESR requirement eases up by half the total trace resistance. For example, if the ESR requirement of the output capacitors without voltage level shifting must be 7mΩ then after level shifting the new ESR will only need to be 8.5mΩ if the trace resistance is 5mΩ (7+5/2=9.5). However, one must be careful that the combined "voltage level shifting" and the transient response is still within the maximum tolerance of the Intel specification. To insure this, the maximum trace resistance must be less than:

$$Rs \leq 2 \times (Vspec - 0.02 \times Vo - \Delta Vo) / \Delta I$$

Where:
Rs = Total maximum trace resistance allowed
Vspec = Intel total voltage spec
Vo = Output voltage
ΔVo = Output ripple voltage
ΔI = load current step

For example, assuming:
Vspec = ±140mV = ±0.1V for 2V output
Vo = 2V
ΔVo = assume 10mV = 0.01V
ΔI = 14.2A

Then the Rs is calculated to be:

$$Rs \leq 2 \times (0.140 - 0.02 \times 2 - 0.01) / 14.2 = 12.6m\Omega$$

However, if a resistor of this value is used, the maximum power dissipated in the trace (or if an external resistor is being used) must also be considered. For example if Rs=12.6mΩ, the power dissipated is:

$$Io^2 \times Rs = 14.2^2 \times 12.6 = 2.54W$$

This is a lot of power to be dissipated in a system. So, if the Rs=5mΩ, then the power dissipated is about 1W which is much more acceptable. If level shifting is not implemented, then the maximum output capacitor ESR was shown previously to be 7mΩ which translated to ≈ 6 of the 1500μF, 6MV1500GX type Sanyo capacitors. With Rs=5mΩ, the maximum ESR becomes 9.5mΩ which is equivalent to ≈ 4 caps. Another important consideration is that if a trace is being used to implement the resistor, the power dissipated by the trace increases the case temperature of the output capacitors which could seriously effect the life time of the output capacitors.

Output Inductor Selection

The output inductance must be selected such that under low line and the maximum output voltage condition, the inductor current slope times the output capacitor ESR is ramping up faster than the capacitor voltage is drooping during a load current step.

However, if the inductor is too small, the output ripple current and ripple voltage become too large. One solution to bring the ripple current down is to increase the switching frequency, however that will be at the cost of reduced efficiency and higher system cost. The following set of formulas are derived to achieve the optimum performance without many design iterations.

The maximum output inductance is calculated using the following equation:

$$L = ESR \times C \times (V_{IN(MIN)} - Vo_{(MAX)}) / (2 \times \Delta I)$$

Where:
$V_{IN(MIN)}$ = Minimum input voltage
For Vo=2.8V, ΔI=14.2A:

$$L = 0.006 \times 9000 \times (4.75 - 2.8) / (2 \times 14.2) = 3.7\mu H$$

Assuming that the programmed switching frequency is set at 200KHz, an inductor is designed using the Micrometals' Powder Iron core material. The summary of the design is outlined below:

The selected core material is Powder Iron, the selected core is T50-52D from Micro Metal wound with 8 turns of #16 AWG wire, resulting in 3μH inductance with ≈ 3mΩ of DC resistance.

Assuming L=3μH and Fsw=200KHz (switching frequency), the inductor ripple current and the output ripple voltage is calculated using the following set of equations:

T ≡ Switching Period
D ≡ Duty Cycle
Vsw ≡ High-side MOSFET ON Voltage
R_{DS} ≡ MOSFET On-resistance
Vsync ≡ Synchronous MOSFET ON Voltage
ΔIr ≡ Inductor Ripple Current
ΔVo ≡Output Ripple Voltage

$$T = 1 / Fsw$$

$$Vsw = Vsync = Io \times R_{DS}$$

$$D \approx (Vo + Vsync) / (V_{IN} - Vsw + Vsync)$$

$$T_{ON} = D \times T$$

$$T_{OFF} = T - T_{ON}$$

$$\Delta Ir = (Vo + Vsync) \times T_{OFF} / L$$

$$\Delta Vo = \Delta Ir \times ESR$$

In our example for Vo=2.8V and 14.2 A load, assuming IRL3103 MOSFET for both switches with maximum on resistance of 19mΩ, we have:

$$T = 1 / 200000 = 5\mu s$$
$$Vsw = Vsync = 14.2 \times 0.019 = 0.27V$$
$$D \approx (2.8 + 0.27) / (5 - 0.27 + 0.27) = 0.61$$
$$T_{ON} = 0.61 \times 5 = 3.1\mu s$$
$$T_{OFF} = 5 - 3.1 = 1.9\mu s$$
$$\Delta Ir = (2.8 + 0.27) \times 1.9 / 3 = 1.94A$$
$$\Delta Vo = 1.94 \times 0.006 = 0.011V = 11mV$$

Power Component Selection

Assuming IRL3103 MOSFETs as power components, we will calculate the maximum power dissipation as follows:

For high-side switch the maximum power dissipation happens at maximum Vo and maximum duty cycle.

$$D_{MAX} \approx (2.8 + 0.27) / (4.75 - 0.27 + 0.27) = 0.65$$
$$P_{DH} = D_{MAX} \times Io^2 \times R_{DS(MAX)}$$
$$P_{DH} = 0.65 \times 14.2^2 \times 0.029 = 3.8W$$

$R_{DS(MAX)}$ = Maximum $R_{DS(ON)}$ of the MOSFET at 125°C

For synch MOSFET, maximum power dissipation happens at minimum Vo and minimum duty cycle.

$$D_{MIN} \approx (2 + 0.27) / (5.25 - 0.27 + 0.27) = 0.43$$
$$P_{DS} = (1-D_{MIN}) \times Io^2 \times R_{DS(MAX)}$$
$$P_{DS} = (1 - 0.43) \times 14.2^2 \times 0.029 = 3.33\ W$$

Heat Sink Selection

Selection of the heat sink is based on the maximum allowable junction temperature of the MOSFETS. Since we previously selected the maximum $R_{DS(ON)}$ at 125°C, then we must keep the junction below this temperature. Selecting TO-220 package gives θ_{JC}=1.8°C/W (from the venders' data sheet) and assuming that the selected heat sink is black anodized, the heat-sink-to-case thermal resistance is: θcs=0.05°C/W, the maximum heat sink temperature is then calculated as:

$$Ts = T_J - P_D \times (\theta_{JC} + \theta cs)$$

$$Ts = 125 - 3.82 \times (1.8 + 0.05) = 118°C$$

With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance (θ_{SA}) is calculated as follows:

Assuming T_A = 35°C:

$$\Delta T = Ts - T_A = 118 - 35 = 83°C$$

Temperature Rise Above Ambient

$$\theta_{SA} = \Delta T / P_D = 83 / 3.82 = 22°C/W$$

Next, a heat sink with lower θ_{SA} than the one calculated in the previous step must be selected. One way to do this is to look at the graphs of the "Heat Sink Temp Rise Above the Ambient" vs. the "Power Dissipation" given in the heat sink manufacturers' catalog and select a heat sink that results in lower temperature rise than the one calculated in previous step. The following heat sinks from AAVID and Thermalloy meet this criteria.

Co.	Part #
Thermalloy	6078B
AAVID	577002

Following the same procedure for the Schottky diode results in a heat sink with θ_{SA}=25°C/W. Although it is possible to select a slightly smaller heat sink, for simplicity the same heat sink as the one for the high side MOSFET is also selected for the synchronous MOSFET.

Switcher Current Limit Protection

The IRU3018 uses the MOSFET $R_{DS(ON)}$ as the sensing resistor to sense the MOSFET current and compares to a programmed voltage which is set externally via a resistor (Rcs) placed between the drain of the MOSFET and the "OCSet1" terminal of the IC as shown in the application circuit. For example, if the desired current limit point is set to be 22A, for the synchronous and 16A for the non-synchronous, and from our previous selection, the maximum MOSFET $R_{DS(ON)}$=19mΩ, then the current sense resistor Rcs is calculated as:

$$Vcs = I_{CL} \times R_{DS} = 22 \times 0.019 = 0.418V$$
$$Rcs = Vcs / I_B = (0.418V) / (200\mu A) = 2.1K\Omega$$

Where:
I_B = 200μA is the internal current setting of the IRU3018

Switcher Frequency Selection

The IRU3018 frequency is internally set at 200KHz with no external timing resistor. However, it can be adjusted up by using an external resistor from Rt pin to Gnd or can be adjusted down if the resistor is connected to the 12V supply.

1.5V, GTL+ Supply LDO Power MOSFET Selection

The first step in selecting the power MOSFET for the 1.5V linear regulator is to select its maximum $R_{DS(ON)}$ of the pass transistor based on the input to output Dropout voltage and the maximum load current.

$$R_{DS(MAX)} = (V_{IN} - Vo) / I_L$$

For Vo = 1.5V, V_{IN} = 3.3V and, I_L = 2A:

$$R_{DS(MAX)} = (3.3 - 1.5) / 2 = 0.9\Omega$$

Note that since the MOSFETs $R_{DS(ON)}$ increases with temperature, this number must be divided by ≈ 1.5, in order to find the $R_{DS(ON)}$ max at room temperature. The Motorola MTP3055VL has a maximum of 0.18Ω $R_{DS(ON)}$ at room temperature, which meets our requirement.

To select the heat sink for the LDO MOSFET, first calculate the maximum power dissipation of the device and then follow the same procedure as for the switcher.

$$P_D = (V_{IN} - Vo) \times I_L$$

Where:
P_D = Power Dissipation of the Linear Regulator
I_L = Linear Regulator Load Current

For the 1.5V and 2A load:

$$P_D = (3.3 - 1.5) \times 2 = 3.6W$$

Assuming $T_{J(MAX)}$ = 125°C:

$$Ts = T_J - P_D \times (\theta_{JC} + \theta cs)$$
$$Ts = 125 - 3.6 \times (1.8 + 0.05) = 118°C$$

With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance (θ_{SA}) is calculated as follows:

Assuming T_A = 35°C:

$$\Delta T = Ts - Ta = 118 - 35 = 83\ °C$$
Temperature Rise Above Ambient

$$\theta_{SA} = \Delta T / P_D = 83 / 3.6 = 23°C/W$$

The same heat sink as the one selected for the switcher MOSFETs is also suitable for the 1.5V regulator.

2.5V, Clock Supply

The IRU3018 provides an internal ultra low dropout regulator with a minimum of 200mA current capability that converts 3.3V supply to a programmable regulated 2.5V supply to power the clock chip. The internal regulator has short circuit protection with internal thermal shutdown.

1.5V and 2.5V Supply Resistor Divider Selection

Since the internal voltage reference for the linear regulators is set at 1.26V for IRU3018, there is a need to use external resistor dividers to step up the voltage. The resistor dividers are selected using the following equations:

$$Vo = (1 + Rt/R_B) \times V_{REF}$$

Where:
Rt = Top resistor divider
R_B = Bottom resistor divider
V_{REF} = 1.26V typical

For 1.5V supply
Assuming R_B=100Ω:

$Rt = R_B \times [(Vo/V_{REF}) - 1]$
$Rt = 100 \times [(1.5/1.26) - 1] = 19.1\Omega$

For 2.5V supply
Assuming R_B=200Ω:

$Rt = R_B \times [(Vo/V_{REF}) - 1]$
$Rt = 200 \times [(2.5/1.26) - 1] = 197\Omega$

Select Rt=200Ω

Switcher Output Voltage Adjust
As it was discussed earlier, the trace resistance from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transitioning from light load to full load and vice versa. To account for the DC drop, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the Gnd pin of the IRU3018 is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70mV or 35mV higher than the DAC voltage setting. To do this, the top resistor of the resistor divider (R17 in the application circuit) is set at 100Ω, and the R19 is calculated. For example, if DAC voltage setting is for 2.8V and the desired output under light load is 2.835V, then R19 is calculated using the following formula:

$R19 = 100 \times [V_{DAC}/(Vo - 1.004 \times V_{DAC})]$ (Ω)
$R19 = 100 \times [2.8/(2.835 - 1.004 \times 2.800)] = 11.76K\Omega$

Select 11.8KΩ, 1%

Note: The value of the top resistor must not exceed 100Ω. The bottom resistor can then be adjusted to raise the output voltage.

Soft-Start Capacitor Selection
The soft-start capacitor must be selected such that during the start-up when the output capacitors are charging up, the peak inductor current does not reach the current limit threshold. A minimum of 1μF capacitor insures this for most applications. An internal resistor charges the soft-start capacitor which slowly ramps up the inverting input of the PWM comparator V_{FB}3. This insures the output voltage to ramp at the same rate as the soft-start cap thereby limiting the input current. For example, with 1μF of soft-start capacitor, the ramp up rate is approximated to be 1V/20ms. For example if the output capacitance is 9000μF, the maximum start up current will be:

$I = 9000\mu F \times (1V/20ms) = 0.45A$

The other function of the soft-start cap is to provide an off time between the current limit cycles(HICCUP) in order for the synchronous MOSFET to cool off and survive the short circuit condition. The off time between the current limit cycles is approximated as:

$T_{HICCUP} = 60 \times Css$ (ms)
For example if Css=1μF, $T_{HICCUP} = 60 \times 1 = 60ms$

Input Filter
It is recommended to place an inductor between the system 5V supply and the input capacitors of the switching regulator to isolate the 5V supply from the switching noise that occurs during the turn on and off of the switching components. Typically an inductor in the range of 1 to 3μH will be sufficient in this type of application.

External Shutdown
The best way to shutdown the IRU3018 is to pull down on the soft-start pin using an external small signal transistor such as 2N3904 or 2N7002 small signal MOSFET. This allows slow ramp up of the output, the same as the power up.

Layout Considerations
Switching regulators require careful attention to the layout of the components, specifically power components since they switch large currents. These switching components can create large amount of voltage spikes and high frequency harmonics if some of the critical components are far away from each other and are connected with inductive traces. The following is a guideline of how to place the critical components and the connections between them in order to minimize the above issues.

Start the layout by first placing the power components:

1) Place the input capacitor C14 and the high-side MOSFET, Q3 as close to each other as possible.

2) Place the synchronous MOSFET, Q4 and the Q3 as close to each other as possible with the intention that the source of Q3 and drain of the Q4 has the shortest length.

3) Place the snubber R15 & C13 between Q4 & Q3.

4) Place the output inductor, L3 and the output capacitors, C16 between the mosfet and the load with output capacitors distributed along the slot 1 and close to it.

5) Place the bypass capacitors, C8 and C19 right next to 12V and 5V pins. C8 next to the 12V, pin 1 and C19 next to the 5V, pin 8.

6) Place the IRU3018 such that the PWM output drives, pins 24 and 22 are relatively short distance from gates of Q3 and Q4.

7) Place all resistor dividers close to their respective feedback pins.

8) Place the 2.5V output capacitor, C18 close to the pin 13 of the IC and the 1.5V output capacitor, C17 close to the Q2 MOSFET.

   Note: It is better to place the 1.5V linear regulator components close to the 3018 and then run a trace from the output of the regulator to the load. However, if this is not possible then the trace from the linear drive output pin, pin 16 must be run away from any high frequency data signals.

   It is critical, to place high frequency ceramic capacitors close to the clock chip and termination resistors to provide local bypassing.

9) Place R12 and C10 close to pin 20

10) Place C9 close to pin 9

Component connections:

Note: It is extremely important that no data bus should be passing through the switching regulator section specifically close to the fast transition nodes such as PWM drives or the inductor voltage.

Using the 4 layer board, dedicate on layer to ground, another layer as the power layer for the 5V, 3.3V, Vcore, 1.5V and if it is possible for the 2.5V.

Connect all grounds to the ground plane using direct vias to the ground plane.

Use large low inductance/low impedance plane to connect the following connections either using component side or the solder side.

a) C14 to Q3 Drain
b) Q3 Source to Q4 Drain
c) Q4 Drain to L3
d) L3 to the output capacitors, C16
e) C16 to the load, slot 1
f) Input filter L1 to the C16 and C3
g) C1 to Q2 Drain
h) C17 to the Q2 Source
I) A minimum of 0.2 inch width trace from the C18 capacitor to pin 13

Connect the rest of the components using the shortest connection possible.

IRU3018 APPLICATION PARTS LIST

Dual Layout with HIP6016

Ref Desig	Description	Qty	Part #	Manuf
Q3,4	MOSFET	2	IRL3103 IRL3103S (Note 1)	 IR
Q5	MOSFET, GP	1	2N7002	Motorola
Q2	MOSFET	1	MTP3055VL, TO-263 package	Motorola
L1	Inductor	1	L=1μH	Micro Metal
L3	Inductor	1	Core: L=2μH, R=2mΩ	Micro Metal
C16	Capacitor, Electrolytic	6	6MV1500GX, 1500μF, 6.3V,	Sanyo
C14	Capacitor, Electrolytic	2	6MV1500GX, 1500μF, 6.3V,	Sanyo
C3	Capacitor, Electrolytic	1	6MV1500GX, 1500μF, 6.3V,	Sanyo
C18	Capacitor, Electrolytic	1	220μF, 6.3V, ECAOJFQ221	Panasonic
C17,C1	Capacitor, Electrolytic	2	680μF, 10V, EEUFA1A681L	Panasonic
C2	Capacitor, Electrolytic	1	680μF, 10V, EEUFA1A681L	Panasonic
C8,19	Capacitor, Ceramic	2	0805Z105P250NT 1μF, 25V, Z5U, 0805 SMT	Novacap
C9	Capacitor , Ceramic	1	0805Z105P250NT 1μF, 25V, Z5U, 0805 SMT See Table 2, Dual layout component	Novacap
C10	Capacitor, Ceramic	1	220pF, SMT 0805 size	
C13	Capacitor, Ceramic	1	470pF, SMT 0805 size	
C9,11, 12,15,20			See Table 2, Dual layout component	
R12	Resistor	1	2.21KΩ, 1%, SMT 0805 size	
R13,14	Resistor	2	10Ω, 5%, SMT 1206 size	
R15	Resistor	1	10Ω, 5%, SMT 1206 size	
R20	Resistor	1	10KΩ, 5%, SMT 0805 size	
R6	Resistor	1	100Ω, 1%, SMT 0805 size	
R8	Resistor	1	200Ω, 1%, SMT 0805 size	
R5	Resistor	1	19.1Ω, 1%, SMT 0805 size	
R7	Resistor	1	200Ω, 1%, SMT 0805 size	
R17	Resistor	1	100Ω, 1%, SMT 0805 size	
R19	Resistor	1	10KΩ, 1%, SMT 0805 size	
HS3,4	Q1,3,4 Heatsink	2	6270	Thermalloy
R11,16,18, 21, 22			See Table 2, Dual layout component	

Note 1: For the applications where it is desirable not to use the Heat sink, the IRL3103S MOSFET in the TO-263 SMT package with 1" square of pad area using top and bottom layers of the board as a minimum is required.

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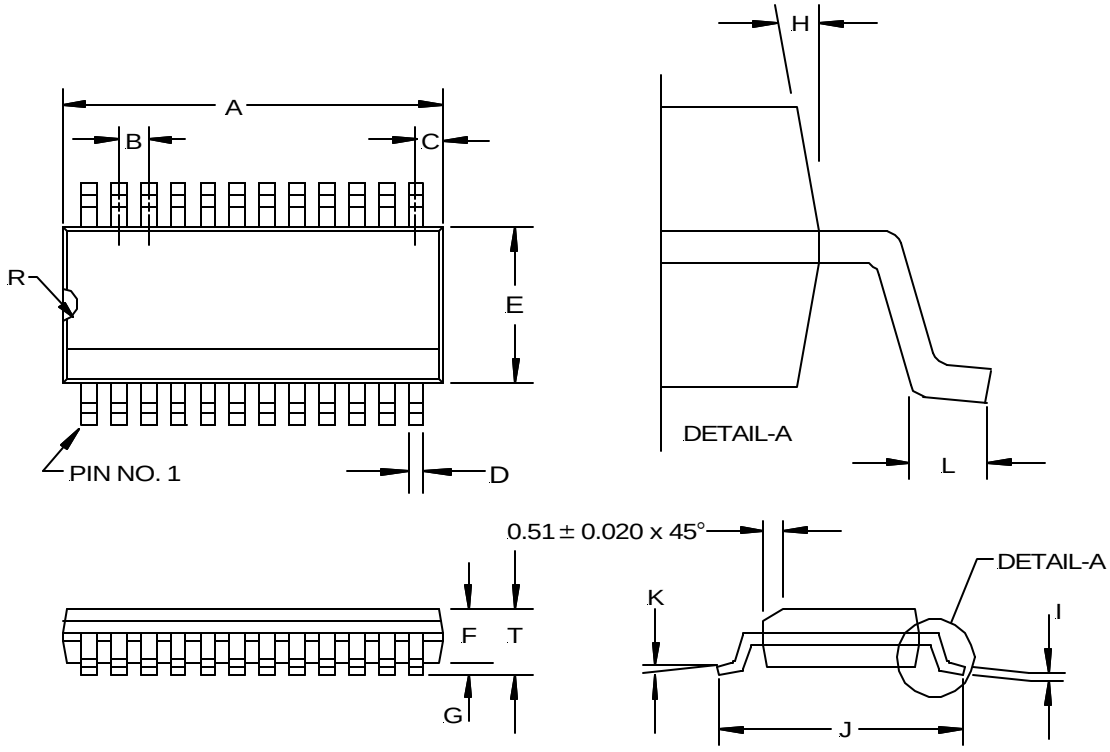
(W) SOIC Package
24-Pin Surface Mount, Wide Body

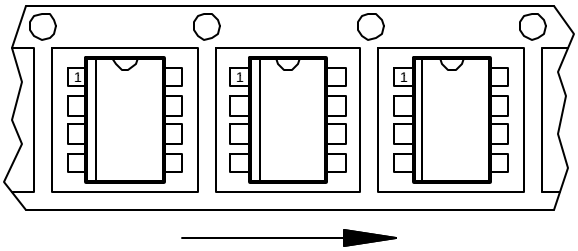


SYMBOL	24-PIN	
	MIN	MAX
A	15.20	15.40
B	1.27 BSC	
C	0.66 REF	
D	0.36	0.46
E	7.40	7.60
F	2.44	2.64
G	0.10	0.30
I	0.23	0.32
J	10.11	10.51
K	0°	8°
L	0.51	1.01
R	0.63	0.89
T	2.44	2.64

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
W	SOIC, Wide Body	24	31	1000	Fig A



Feed Direction
Figure A

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5-BIT PROGRAMMABLE SYNCHRONOUS BUCK CONTROLLER IC WITH TRIPLE LDO CONTROLLER

FEATURES

- Provides single chip solution for Vcore, GTL+, AGP bus, and 1.8V
- Automatic voltage selection for AGP slot V_{DDQ} supply
- Linear Regulator Controller On-Board for 1.8V
- Designed to meet Intel latest VRM specification for next generation microprocessors
- On-Board DAC programs the output voltage from 1.3V to 3.5V
- Linear Regulator Controller On-Board for 1.5V GTL+ Supply
- Loss-less Short Circuit Protection for all Outputs
- Synchronous operation allows maximum efficiency
- Patented architecture allows fixed frequency operation as well as 100% duty cycle during dynamic load
- Minimum Part Count
- Soft-Start
- High current totem pole driver for direct driving of the external Power MOSFET
- Power Good function monitors all outputs
- Over-Voltage Protection Circuitry Protects the switcher output and generates a Fault output

APPLICATIONS

- Total Power Solution for next generation Intel processor application

DESCRIPTION

The IRU3021M controller IC is specifically designed to meet Intel specification for next generation microprocessor applications requiring multiple on-board regulators. The IRU3021M provides a single chip controller IC for the Vcore, three LDO controllers, one with an automatic select pin that connects to the Type Detect pin of the AGP slot for the AGP V_{DDQ} supply, one for GTL+ and the other for the 1.8V chip set regulator as required for the next generation PC applications. The IRU3021M uses N-channel MOSFET as pass transistor for $V_{OUT}2(V_{DDQ})$, $V_{OUT}3(1.5V)$ and $V_{OUT}4(1.8V)$. No external resistor divider is necessary for any of the regulators. The switching regulator feature a patented topology that in combination with a few external components as shown in the typical application circuit, will provide well in excess of 20A of output current for an on-board DC/DC converter while automatically providing the right output voltage via the 5-bit internal DAC .The IRU3021M also features, loss-less current sensing for both switcher by using the $R_{DS(ON)}$ of the high-side power MOSFET as the sensing resistor, an output under-voltage shutdown that detects short circuit condition for the linear outputs and latches the system off, and a Power Good window comparator that switches its open collector output low when any one of the outputs is outside of a pre-programmed window.

TYPICAL APPLICATION

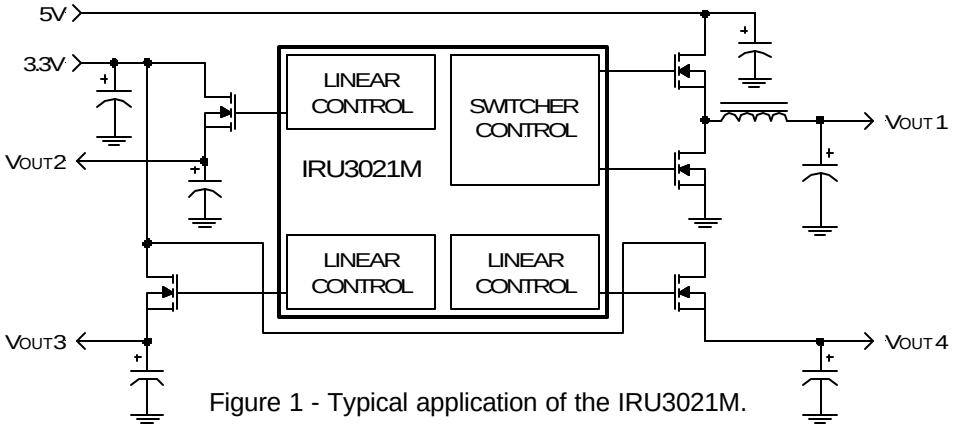


Figure 1 - Typical application of the IRU3021M.

PACKAGE ORDER INFORMATION

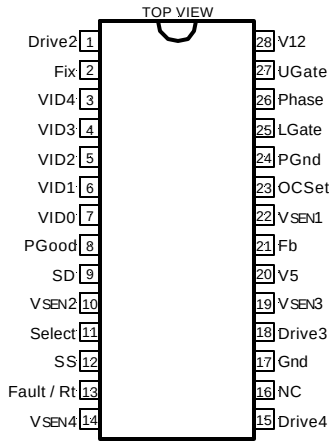
T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3021MCW	28-Pin Plastic SOIC WB (W)

ABSOLUTE MAXIMUM RATINGS

V5 Supply Voltage 7V
V12 Supply Voltage 20V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

28-PIN WIDE BODY PLASTIC SOIC (W)



θ_{JA} =80°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V12=12V, V5=5V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply UVLO Section						
UVLO Threshold-12V		Supply Ramping Up		10		V
UVLO Hysteresis-12V				0.6		V
UVLO Threshold-5V		Supply Ramping Up		4.4		V
UVLO Hysteresis-5V				0.3		V
Supply Current						
Operating Supply Current		V12 V5		6 30		mA
Switching Controllers; Vcore (V_{SEN}1) and AGP (V_{SEN}2)						
VID Section (Vcore only)						
DAC Output Voltage (Note 1)			0.99Vs	Vs	1.01Vs	V
DAC Output Line Regulation				0.1		%
DAC Output Temp Variation				0.5		%
VID Input LO					0.8	V
VID Input HI			2			V
VID Input Internal Pull-Up Resistor to V5				27		KΩ
V_{SEN}2 Voltage		Select <0.8V Select >2V		1.5 3.3		V

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Comparator Section						
Input Bias Current					2	µA
Input Offset Voltage			-2		+2	mV
Delay to Outout		V_{DIFF}=10mV			100	ns
Current Limit Section						
CS Threshold Set Current				200		µA
CS Comp Offset Voltage			-5		+5	mV
Hiccup Duty Cycle		Css=0.1µF		10		%
Output Drivers Section						
Rise Time		C_L=3000pF		70		ns
Fall Time		C_L=3000pF		70		ns
Dead Band Time Between High Side and Synch Drive (Vcore Switcher Only)		C_L=3000pF		200		ns
Oscillator Section (Internal)						
Osc Frequency		Rt=Open		217		KHz
1.8V Regulator (V_{SEN}4)						
V_{SEN} Voltage	V_O4	T_A=25°C, Drive4=V_{SEN}4		1.800		V
V_{SEN} Voltage				1.800		V
Input Bias Current					2	µA
Output Drive Current		V_{AUX} - V_{DRIVE}>0.6V	50			mA
1.5V Regulator (V_{SEN}3)						
V_{SEN} Voltage	V_O3	T_A=25°C, Drive3=V_{SEN}3		1.500		V
V_{SEN} Voltage				1.500		V
Input Bias Current					2	µA
Output Drive Current		V_{AUX} - V_{DRIVE}>0.6V	50			mA
Power Good Section						
V_{SEN}1 UV Lower Trip Point		V_{SEN}1 Ramping Down		0.90Vs		V
V_{SEN}1 UV Upper Trip Point		V_{SEN}1 Ramping Up		0.92Vs		V
V_{SEN}1 UV Hysterises				0.02Vs		V
V_{SEN}1 HV Upper Trip Point		V_{SEN}1 Ramping Up		1.10Vs		V
V_{SEN}1 HV Lower Trip Point		V_{SEN}1 Ramping Down		1.08Vs		V
V_{SEN}1 HV Hysterises				0.02Vs		V
V_{SEN}2 Trip Point		Select <0.8V Select >2V		1.100 2.560		V
V_{SEN}3 Trip Point		Fix=Gnd Fix=Open		0.920 1.320		V
V_{SEN}4 Trip Point		Fix=Gnd Fix=Open		0.920 1.140		V
Power Good Output LO		R_L=3mA		0.4		V
Power Good Output HI		R_L=5K, Pull-Up to 5V		4.8		V
Fault (Overvoltage) Section						
Core OV Upper Trip Point		V_{SEN}1 Ramping Up		1.17Vs		V
Core OV Lower Trip Point		V_{SEN}1 Ramping Down		1.15Vs		V
Fault Output HI		Io=3mA		10		V
Soft-Start Section						
Pull-Up Resistor to 5V		OCSet=0V, Phase=5V		20		µA

Note 1: Vs refers to the set point voltage given in Table 1.

D4	D3	D2	D1	D0	Vs
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05

D4	D3	D2	D1	D0	Vs
1	1	1	1	1	2.0
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

Table 1 - Set point voltage vs. VID codes.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Drive2	This pin controls the gate of an external MOSFET for the AGP linear regulator.
2	Fix	Leaving this pin open provides fixed output voltages of the 1.5V and 1.8V for the #3 and #4 linear regulators. When this pin is grounded the reference to the linear regulators are set to 1.26V and therefore the output of the regulators can be programmed to any voltages above the 1.26V using: $V_{OUT}=1.26 \times (1 + R_{TOP}/R_{BOT})$ Where: R_{TOP} = Top resistor connected from the output to the V_{SENSE} pin. R_{BOT} = Bottom resistor connected from the V_{SENSE} pin to ground.
3	VID4	This pin selects a range of output voltages for the DAC. When in the LOW state the range is 1.3V to 2.05V and when it switches to HI state the range is 2.0V to 3.5V. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
4	VID3	MSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
5	VID2	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
6	VID1	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
7	VID0	LSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
8	PGood	This pin is an open collector output that switches LO when any of the outputs are outside of the specified under-voltage trip point. It also switches low when $V_{SEN}1$ pin is more than 10% above the DAC voltage setting.

PIN#	PIN SYMBOL	PIN DESCRIPTION
9	SD	This pin provides shutdown for all the regulators. A TTL compatible, logic level high applied to this pin disables all the outputs and discharges the soft-start capacitor. The SD signal turns off the synchronous MOSFET allowing body diode to conduct and discharge the output capacitor.
10	$V_{SEN}2$	This pin provides the feedback for the AGP linear regulator. The Select pin when connected to the "Type Detect" pin of the AGP slot automatically selects the right voltage for the AGP V_{DDQ}.
11	Select	This pin provides automatic voltage selection for the AGP switching regulator. When it is pulled LO, the voltage is 1.5V and when left open or pulled to HI, the voltage is 3.3V.
12	SS	This pin provides the soft-start for all the regulators. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the outputs of the regulators, preventing the outputs from overshooting as well as limiting the input current. The second function of the Soft-Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting.
13	Fault / Rt	This pin has dual function. It acts as an output of the over-voltage protection circuitry or it can be used to program the frequency using an external resistor. When used as a fault detector, if any of the switcher outputs exceed the OVP trip point, the Fault pin switches to 12V and the soft-start cap is discharged. If the Fault pin is to be connected to any external circuitry, it needs to be buffered.
14	$V_{SEN}4$	This pin provides the feedback for the linear regulator that its output drive is Drive4.
15	Drive4	This pin controls the gate of an external MOSFET for the 1.8V chip set linear regulator.
16	NC	This pin is not connected internally.
17	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane.
18	Drive3	This pin controls the gate of an external transistor for the 1.5V GTL+ linear regulator.
19	$V_{SEN}3$	This pin provides the feedback for the linear regulator that its output drive is Drive3.
20	V5	5V supply voltage. A high frequency capacitor (0.1 to 1µF) must be placed close to this pin and connected from this pin to the ground plane for noise free operation.
21	Fb	This pin provides the feedback for the synchronous switching regulator. Typically this pin can be connected directly to the output of the switching regulator. However, a resistor divider is recommended to be connected from this pin to $V_{OUT}1$ and ground to adjust the output voltage for any drop in the output voltage that is caused by the trace resistance. The value of the resistor connected from $V_{OUT}1$ to Fb1 must be less than 1000Ω.
22	$V_{SEN}1$	This pin is internally connected to the under-voltage and over-voltage comparators sensing the Vcore status. It must be connected directly to the Vcore supply.
23	OCSet	This pin is connected to the Drain of the power MOSFET of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the current sense threshold depending on the R_{DS} of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.
24	PGnd	This pin serves as the Power ground pin and must be connected directly to the ground plane close to the source of the synchronous MOSFET. A high frequency capacitor (typically 1µF) must be connected from V12 pin to this pin for noise free operation.
25	LGate	Output driver for the synchronous power MOSFET for the Core supply.
26	Phase	This pin is connected to the source of the power MOSFET for the Core supply and it provides the negative sensing for the internal current sensing circuitry.
27	UGate	Output driver for the high side power MOSFET for the Core supply.
28	V12	This pin is connected to the 12V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (typically 1µF) must be placed close to this pin and PGnd pin and be connected directly from this pin to the ground plane for the noise free operation.

BLOCK DIAGRAM

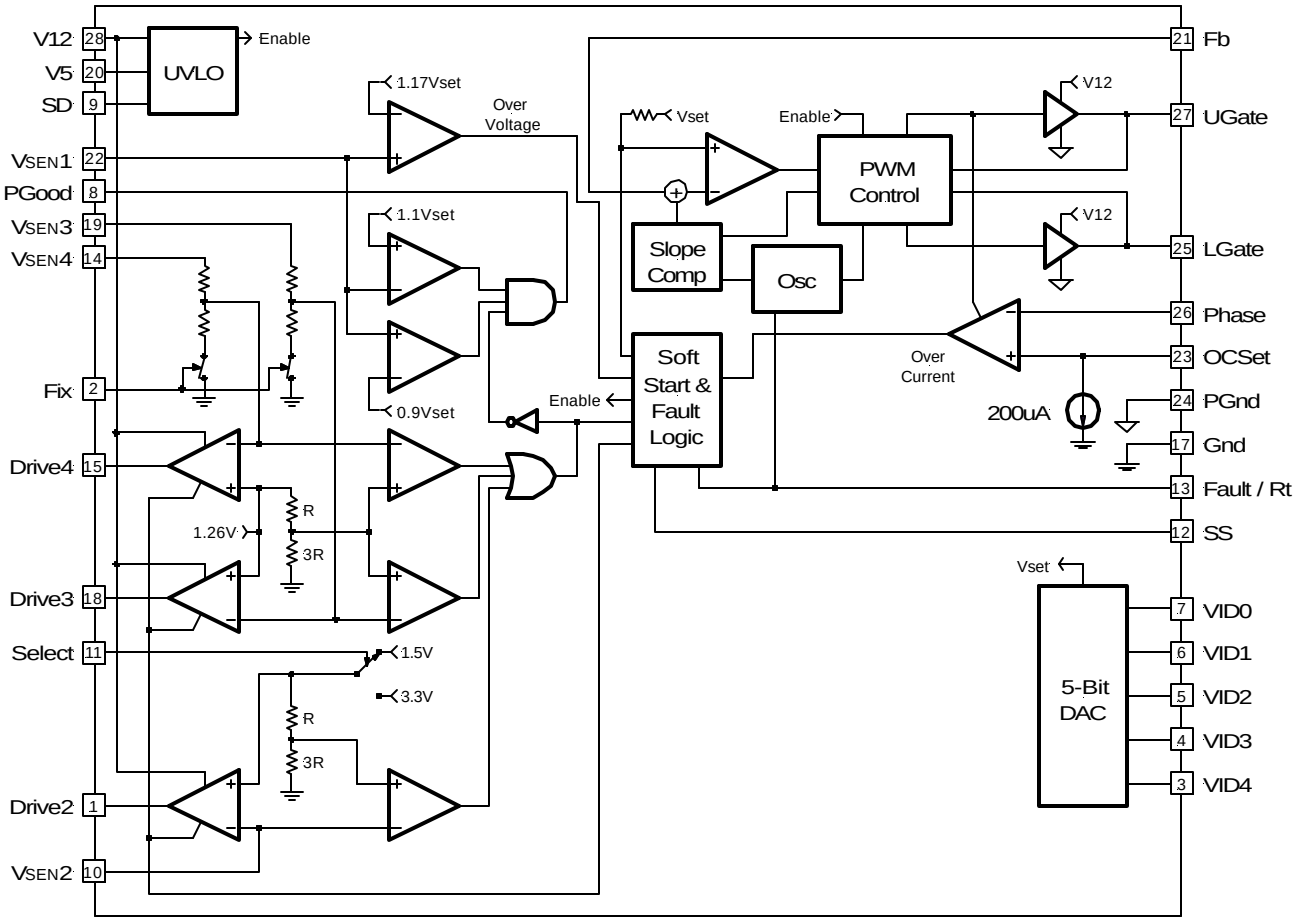


Figure 2 - Simplified block diagram of the IRU3021M.

TYPICAL APPLICATION

(Dual Layout with HIP6021)

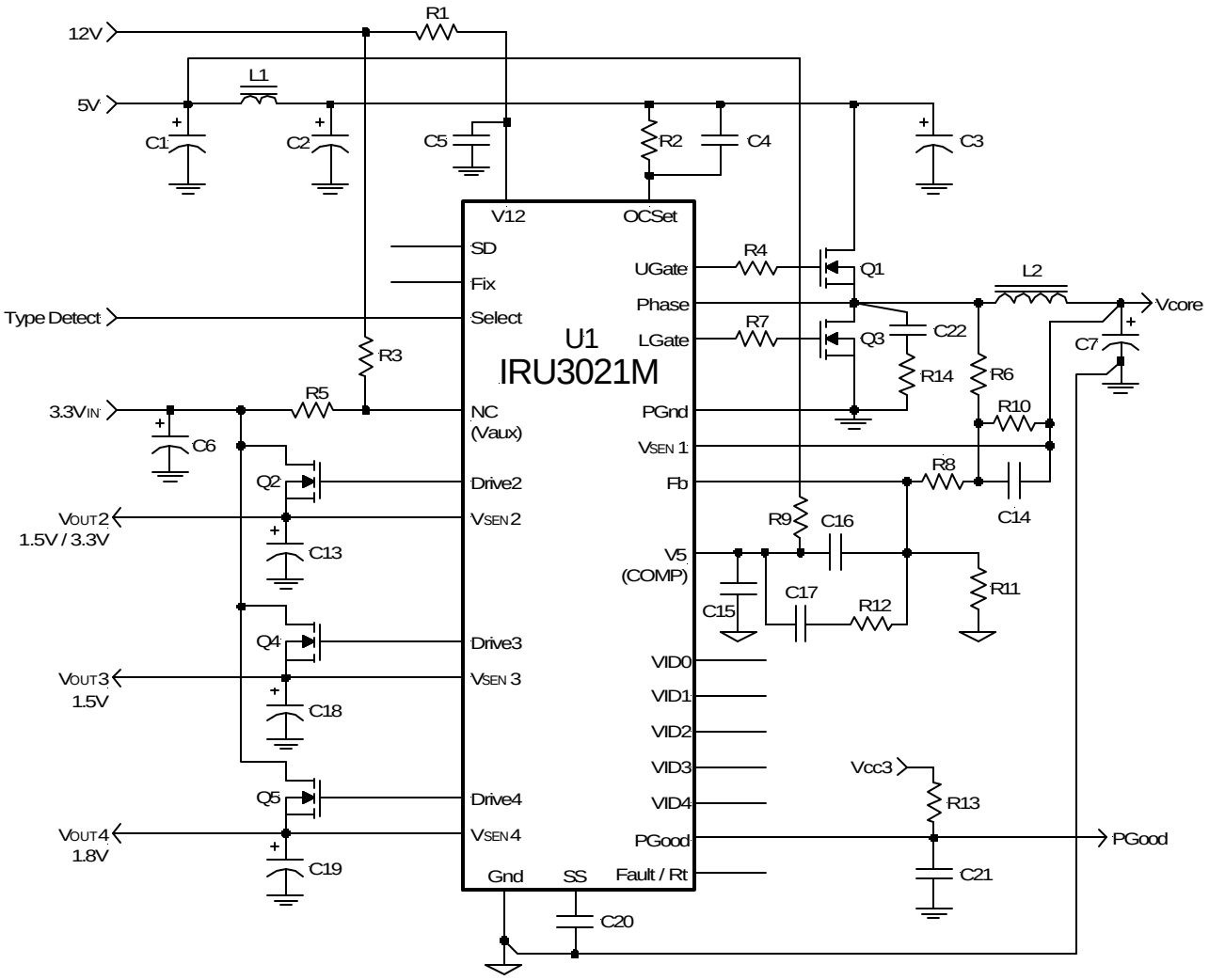


Figure 3 - Typical application of IRU3021M in a dual layout with HIP6021 for an on-board DC-DC converter providing power for the Vcore, GTL+, 1.8V chip set supply as well as auto select AGP supply for the next generation PC applications.

Part#	R3	R5	R9	R12	C15	C16	C17
HIP6021	O	S	O	V	O	V	V
IRU3021M	S	O	S	O	V	O	O

S - Short O - Open V - See IR or Harris parts list for the value

Table 2 - Dual layout component table.

IRU3021M APPLICATION PARTS LIST

Dual Layout with HIP6021

Ref Desig	Description	Qty	Part #	Manuf
Q1	MOSFET	1	IRL3103S, TO-263 package	IR
Q2	MOSFET	1	IRLR3103, TO-252 package	IR
Q3	MOSFET with Schottky	1	IRL3103D1S, TO-263 package	IR
Q4,5	MOSFET	2	IRLR024, TO-252 package	IR
L1	Inductor	1	L=1μH, 5052 core with 4 turns of 1.0mm wire	Micro Metal
L2	Inductor	1	L=2.7μH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1	Capacitor, Electrolytic	1	10MV470GX, 470μF, 10V	Sanyo
C2,3	Capacitor, Electrolytic	2	10MV1200GX, 1200μF, 10V	Sanyo
C4	Capacitor, Ceramic	1	220pF, 0603	
C5	Capacitor, Ceramic	1	1μF, 0805	
C6,18	Capacitor, Electrolytic	2	6MV1000GX, 1000μF, 6.3V	Sanyo
C7	Capacitor, Electrolytic	6	6MV1500GX, 1500μF, 6.3V	Sanyo
C13,19	Capacitor, Electrolytic	1	6MV1500GX, 1500μF, 6.3V	Sanyo
C14,15	Capacitor, Ceramic	2	1μF, 0603	
C16,17	Capacitor, Ceramic	2	See Table 2, dual layout component 0603 × 2	
C20,21	Capacitor, Ceramic	2	0.1μF, 0603	
C22	Capacitor, Ceramic	1	1000pF, 0603	
R1	Resistor	1	10Ω, 5%, 0603	
R2	Resistor	1	3.3KΩ, 5%, 0603	
R3,5,12	Resistor	3	See Table 2, dual layout component 0603 × 3	
R4,7,14	Resistor	3	4.7Ω, 5%, 1206	
R6,8,10	Resistor	3	2.2KΩ, 1%, 0603	
R9	Resistor	1	0Ω, 0603	
R11	Resistor	1	220KΩ, 1%, 0603	
R13	Resistor	1	10KΩ, 5%, 0603	

International
IOR Rectifier

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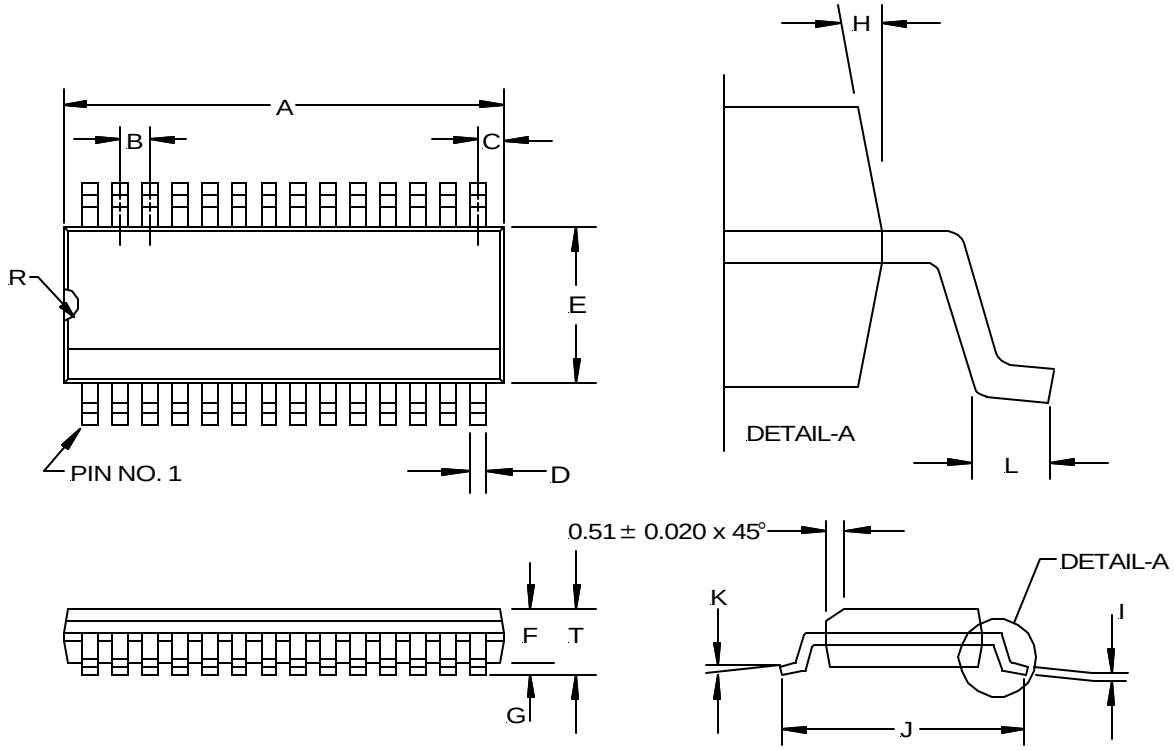
(W) SOIC Package
28-Pin Surface Mount, Wide Body

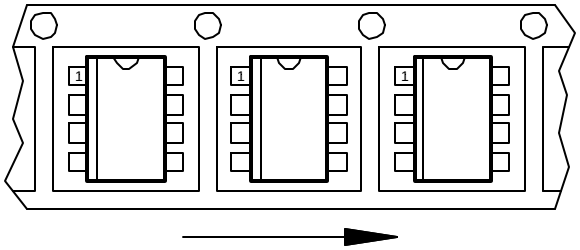


SYMBOL	28-PIN	
	MIN	MAX
A	17.73	17.93
B	1.27 BSC	
C	0.66 REF	
D	0.36	0.46
E	7.40	7.60
F	2.44	2.64
G	0.10	0.30
I	0.23	0.32
J	10.11	10.51
K	0°	8°
L	0.51	1.01
R	0.63	0.89
T	2.44	2.64

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
W	SOIC, Wide Body	28	27	1000	Fig A



Feed Direction
Figure A

International
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5-BIT PROGRAMMABLE SYNCHRONOUS BUCK CONTROLLER IC WITH TRIPLE LDO CONTROLLER

FEATURES

- Designed to meet VRM 9.0 specification for next generation microprocessors
- On-Board 5-Bit DAC programs the output voltage from 1.075V to 1.850V in 25mV steps
- Linear Regulator Controller On-Board for 1.8V
- Provides single chip solution for Vcore, GTL+, AGP bus, and 1.8V
- Automatic Voltage Selection for AGP Slot V_{DDQ} Supply
- Linear Regulator Controller On-Board for 1.5V GTL+ Supply
- Loss-less Short Circuit Protection for all Outputs
- Synchronous operation allows maximum efficiency
- Patented architecture allows fixed frequency operation as well as 100% duty cycle during dynamic load
- Minimum Part Count
- Soft-Start
- High current totem pole driver for direct driving of the external power MOSFET
- Power Good function monitors all outputs
- Over-Voltage Protection Circuitry protects the switcher output and generates a fault output

APPLICATIONS

- Total power solution for next generation Intel processor application
- AMD K7 Low Cost Solution

DESCRIPTION

The IRU3027 controller IC is specifically designed to meet VRM 9.0 specification for next generation microprocessor applications requiring multiple on-board regulators. The IRU3027 provides a single chip controller IC for the Vcore, three LDO controllers, one with an automatic select pin that connects to the Type Detect pin of the AGP slot for the AGP V_{DDQ} supply, one for GTL+ and the other for the 1.8V chip set regulator as required for the next generation PC applications. The IRU3027 is designed to use either bipolar transistors for $V_{OUT}3$(1.5V) and $V_{OUT}4$(1.8V). No external resistor divider is necessary for any of the regulators. The switching regulator features a patented topology that in combination with a few external components as shown in the typical application circuit, will provide well in excess of 20A of output current for an on-board DC-DC converter while automatically providing the right output voltage via the 5-bit internal DAC. The IRU3027 also features loss-less current sensing for both switchers by using the $R_{DS(ON)}$ of the high side power MOSFET as the sensing resistor, an output under-voltage shutdown that detects short circuit condition for the linear outputs and latches the system off, and a Power Good window comparator that switches its open collector output low when any one of the outputs is outside of a pre-programmed window.

TYPICAL APPLICATION

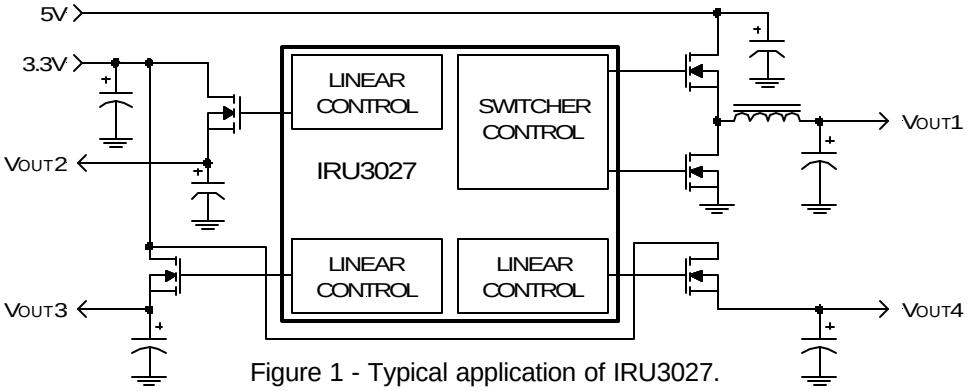


Figure 1 - Typical application of IRU3027.

PACKAGE ORDER INFORMATION

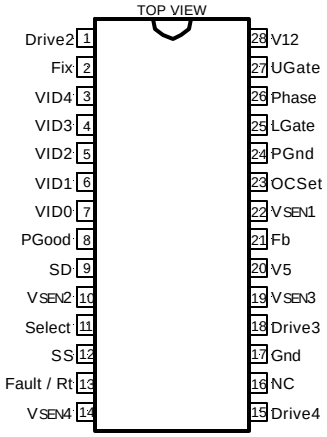
T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3027CW	28-Pin Plastic SOIC WB (W)

ABSOLUTE MAXIMUM RATINGS

V5 Supply Voltage 7V
V12 Supply Voltage 20V
Storage Temperature Range ..... -65 To 150°C
Operating Junction Temperature Range ..... 0 To 125°C

PACKAGE INFORMATION

28 PIN WIDE BODY PLASTIC SOIC (W)



θ_{JA} =80°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V12=12V, V5=5V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply UVLO Section						
UVLO Threshold-12V		Supply Ramping Up		10		V
UVLO Hysteresis-12V				0.6		V
UVLO Threshold-5V		Supply Ramping Up		4.4		V
UVLO Hysteresis-5V				0.3		V
Supply Current						
Operating Supply Current		V12 V5		6 30		mA
Switching Controllers; Vcore (V_{SEN}1) and AGP (V_{SEN}2)						
VID Section (Vcore only)						
DAC Output Voltage (Note 1)			0.99Vs	Vs	1.01Vs	V
DAC Output Line Regulation				0.1		%
DAC Output Temp Variation				0.5		%
VID Input LO					0.8	V
VID Input HI			2			V
VID Input Internal Pull-Up Resistor to V5				27		KΩ
V_{SEN}2 Voltage		Select <0.8V Select >2V		1.5 3.3		V

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Comparator Section						
Input Bias Current					2	µA
Input Offset Voltage			-2		+2	mV
Delay to Outout		V_{DIFF}=10mV			100	ns
Current Limit Section						
CS Threshold Set Current				200		µA
CS Comp Offset Voltage			-5		+5	mV
Hiccup Duty Cycle		Css=0.1µF		10		%
Output Drivers Section						
Rise Time		C_L=3000pF		70		ns
Fall Time		C_L=3000pF		70		ns
Dead Band Time Between High Side and Synch Drive (Vcore Switcher Only)		C_L=3000pF		200		ns
Oscillator Section (Internal)						
Osc Frequency		Rt=Open		217		KHz
1.8V Regulator (V_{SEN}4)						
V_{SEN} Voltage	V_O4	T_A=25°C, Drive4=V_{SEN}4		1.800		V
V_{SEN} Voltage				1.800		V
Input Bias Current					2	µA
Output Drive Current			50			mA
1.5V Regulator (V_{SEN}3)						
V_{SEN} Voltage	V_O3	T_A=25°C, Drive3=V_{SEN}3		1.500		V
V_{SEN} Voltage				1.500		V
Input Bias Current					2	µA
Output Drive Current			50			mA
Power Good Section						
V_{SEN}1 UV Lower Trip Point		V_{SEN}1 Ramping Down		0.90Vs		V
V_{SEN}1 UV Upper Trip Point		V_{SEN}1 Ramping Up		0.92Vs		V
V_{SEN}1 UV Hysterises				0.02Vs		V
V_{SEN}1 HV Upper Trip Point		V_{SEN}1 Ramping Up		1.10Vs		V
V_{SEN}1 HV Lower Trip Point		V_{SEN}1 Ramping Down		1.08Vs		V
V_{SEN}1 HV Hysterises				0.02Vs		V
V_{SEN}2 Trip Point		Select <0.8V Select >2V		1.100 2.560		V
V_{SEN}3 Trip Point		Fix=Gnd Fix=Open		0.920 1.320		V
V_{SEN}4 Trip Point		Fix=Gnd Fix=Open		0.920 1.140		V
Power Good Output LO		R_L=3mA		0.4		V
Power Good Output HI		R_L=5K, Pull-Up to 5V		4.8		V
Fault (Overvoltage) Section						
Core OV Upper Trip Point		V_{SEN}1 Ramping Up		1.17Vs		V
Core OV Lower Trip Point		V_{SEN}1 Ramping Down		1.15Vs		V
Fault Output HI		Io=3mA		10		V
Soft-Start Section						
Pull-Up Resistor to 5V		OCSet=0V, Phase=5V		20		µA

Note 1: Vs refers to the set point voltage given in Table 1.

D4	D3	D2	D1	D0	Vs
1	1	1	1	1	1.075
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450

D4	D3	D2	D1	D0	Vs
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

Table 1 - Set point voltage vs. VID codes.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Drive2	This pin controls the gate of an external MOSFET for the AGP linear regulator.
2	Fix	Leaving this pin open provides fixed output voltages of the 1.5V and 1.8V for the #3 and #4 linear regulators. When this pin is grounded the reference to the linear regulators are set to 1.26V and therefore the output of the regulators can be programmed to any voltages above the 1.26V using: $V_{OUT} = 1.26 \times (1 + R_{TOP}/R_{BOT})$ Where: R_{TOP}=Top resistor connected from the output to the V_{SENSE} pin R_{BOT}=Bottom resistor connected from the V_{SENSE} pin to ground.
3	VID4	This pin selects a range of output voltages for the DAC. When in the LOW state the range is 1.3V to 2.05V and when it switches to HI state the range is 2V to 3.5V. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
4	VID3	MSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
5	VID2	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
6	VID1	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
7	VID0	LSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
8	PGood	This pin is an open collector output that switches LO when any of the outputs are outside of the specified under-voltage trip point. It also switches low when $V_{SEN}1$ pin is more than 10% above the DAC voltage setting.

PIN#	PIN SYMBOL	PIN DESCRIPTION
9	SD	This pin provides shutdown for all the regulators. A TTL compatible, logic level high applied to this pin disables all the outputs and discharges the soft-start capacitor. The SD signal turns off the synchronous allowing the body diode to conduct and discharge the output capacitor.
10	$V_{SEN}2$	This pin provides the feedback for the AGP linear regulator. The Select pin when connected to the "Type Detect" pin of the AGP slot automatically selects the right voltage for the AGP V_{DDQ}.
11	Select	This pin provides automatic voltage selection for the AGP switching regulator. When it is pulled LO, the voltage is 1.5V and when left open or pulled to HI, the voltage is 3.3V.
12	SS	This pin provides the soft-start for all the regulators. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the outputs of the regulators, preventing the outputs from overshooting as well as limiting the input current. The second function of the Soft-Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting.
13	Fault / Rt	This pin has dual function. It acts as an output of the over-voltage protection circuitry or it can be used to program the frequency using an external resistor . When used as a fault detector, if any of the switcher outputs exceed the OVP trip point, the Fault pin switches to 12V and the soft-start cap is discharged. If the Fault pin is to be connected to any external circuitry, it needs to be buffered.
14	$V_{SEN}4$	This pin provides the feedback for the linear regulator that its output drive is Drive4.
15	Drive4	This pin controls the gate of an external MOSFET for the 1.8V chip set linear regulator.
16	NC	This pin has no connection.
17	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane.
18	Drive3	This pin controls the gate of an external transistor for the 1.5V GTL+ linear regulator.
19	$V_{SEN}3$	This pin provides the feedback for the linear regulator that its output drive is Drive3.
20	V5	5V supply voltage. A high frequency capacitor (0.1 to 1μF) must be placed close to this pin and connected from this pin to the ground plane for noise free operation.
21	Fb	This pin provides the feedback for the synchronous switching regulator. Typically this pin can be connected directly to the output of the switching regulator. However, a resistor divider is recommended to be connected from this pin to $V_{OUT}1$ and ground to adjust the output voltage for any drop in the output voltage that is caused by the trace resistance. The value of the resistor connected from $V_{OUT}1$ to Fb1 must be less than 1000Ω.
22	$V_{SEN}1$	This pin is internally connected to the under-voltage and over-voltage comparators sensing the Vcore status. It must be connected directly to the Vcore supply.
23	OCSet	This pin is connected to the Drain of the power MOSFET of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the current sense threshold depending on the R_{DS} of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.
24	PGnd	This pin serves as the Power ground pin and must be connected directly to the ground plane close to the source of the synchronous MOSFET. A high frequency capacitor (typically 1μF) must be connected from V12 pin to this pin for noise free operation.
25	LGate	Output driver for the synchronous power MOSFET for the Core supply.
26	Phase	This pin is connected to the Source of the power MOSFET for the Core supply and it provides the negative sensing for the internal current sensing circuitry.
27	UGate	Output driver for the high side power MOSFET for the Core supply.
28	V12	This pin is connected to the 12V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (typically 1μF) must be placed close to this pin and PGnd pin and be connected directly from this pin to the ground plane for the noise free operation.

BLOCK DIAGRAM

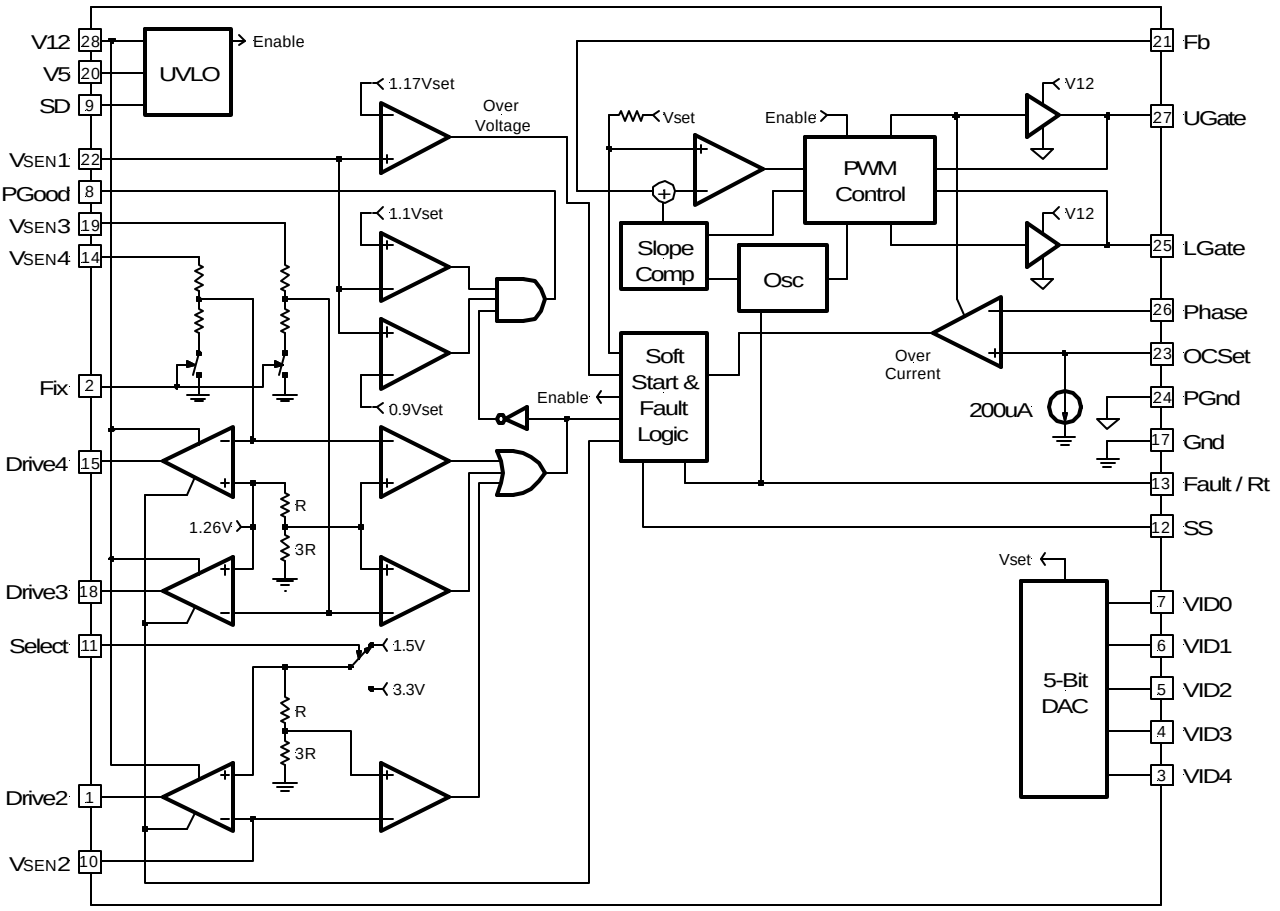


Figure 2 - Simplified block diagram of the IRU3027.

TYPICAL APPLICATION

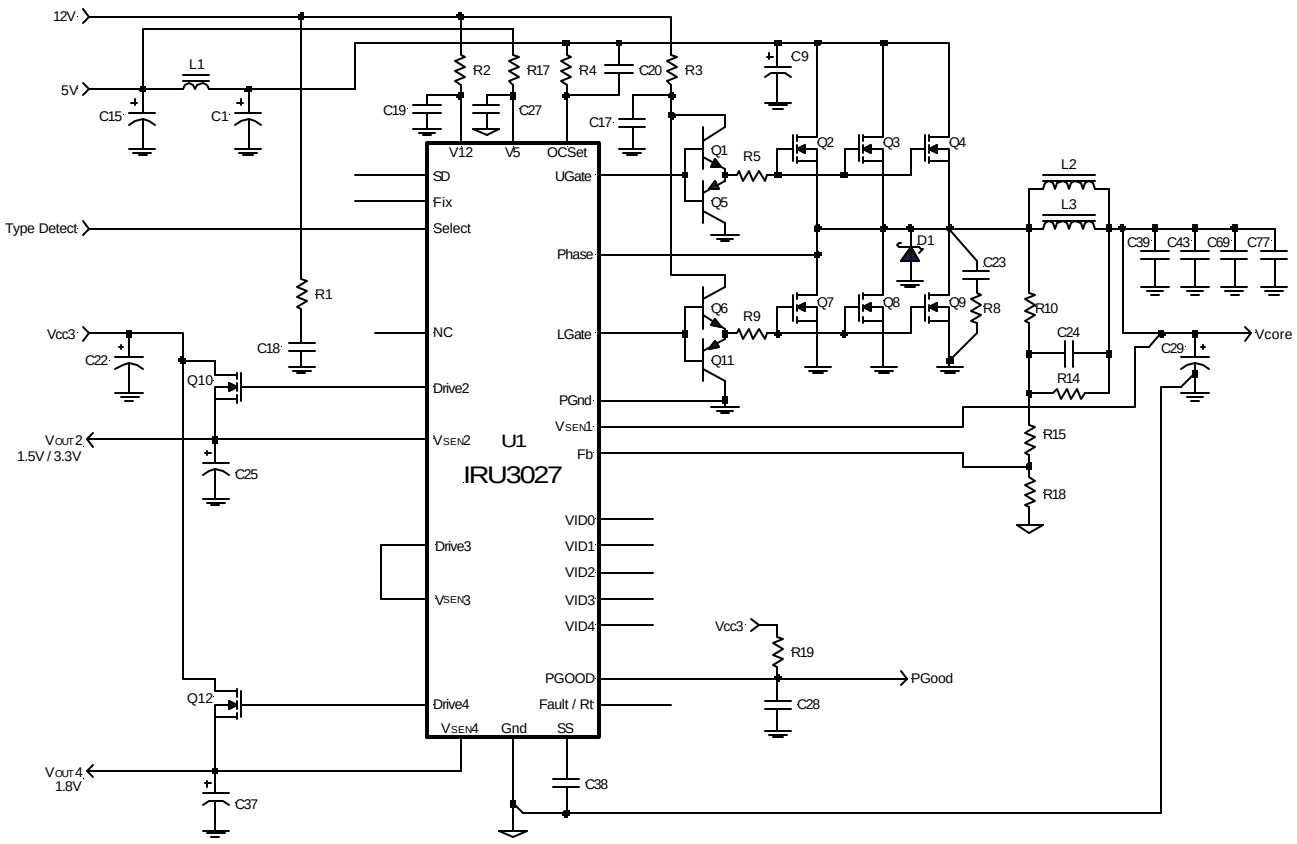


Figure 3 - Typical application of IRU3027 for the AMD Slot A socket.

IRU3027 APPLICATION PARTS LIST

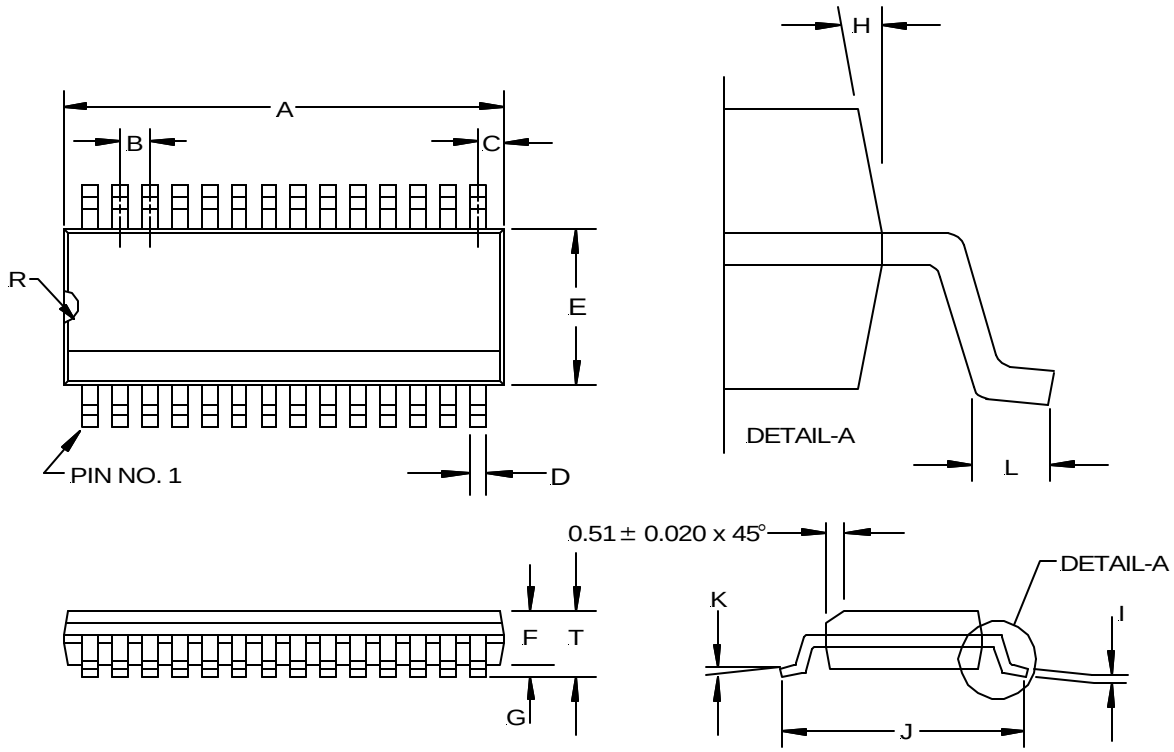
Dual Layout with HIP6019

Ref Desig	Description	Qty	Part #	Manuf
Q1, 6	Transistor	2	2SD882, TO-226 package	Fairchild
Q2, 3, 4	MOSFET	3	IRF3706S, TO-263 package	IR
Q5, 11	Transistor	2	2SB772, TO-226 package	Fairchild
Q7, 8, 9	MOSFET	3	IRL2203NS, TO-263 package	IR
Q10	MOSFET	1	IRLR3103S, TO-252 package	IR
Q12	MOSFET	1	IRLR024, TO-252 package	IR
D1	Diode	1	MBR1535CT, TO-220 package	IR
L1	Inductor	1	L=1μH, 5052B core with 5 turns of triple 0.8mm wire	Micro Metal
L2, 3	Inductor	2	L=1.8μH, 6018 core with 6 turns of triple 0.8mm wire	Micro Metal
C1	Capacitor, Ceramic	8	1μF, 0603	
C9	Capacitor, Electrolytic	6	10MV1500GX, 1500μF, 10V	Sanyo
C15	Capacitor, Electrolytic	1	10MV1500GX, 1500μF, 10V	Sanyo
C16	Capacitor, Ceramic	1	1μF, 0603	
C17, 18, 19, 21	Capacitor, Ceramic	4	1μF, 0805	
C20	Capacitor, Ceramic	1	220pF, 0603	
C22, 26	Capacitor, Electrolytic	2	6MV1000GX, 1000μF, 6.3V	Sanyo
C23	Capacitor, Ceramic	1	1000pF, 0805	
C24, 27	Capacitor, Ceramic	2	1μF, 0603	
C25, 37	Capacitor, Electrolytic	2	6MV1500GX, 1500μF, 6.3V	Sanyo
C28, 38	Capacitor, Ceramic	2	0.1μF, 0603	
C29	Capacitor, Electrolytic	8	6MV2200GX, 2200μF, 6.3V	Sanyo
C39	Capacitor, Ceramic	4	4.7μF, 0805	
C43	Capacitor, Ceramic	26	1μF, 0603	
C69	Capacitor, Ceramic	8	0.01μF, 0603	
C77	Capacitor, Ceramic	8	39pF, 0603	
R1, 2, 3, 7, 16, 21	Resistor	6	10Ω, 5%, 0603	
R4	Resistor	1	2KΩ, 5%, 0603	
R5, 9	Resistor	4	1Ω, 5%, 0805	
R8	Resistor	1	4.7Ω, 5%, 0805	
R10, 14	Resistor	2	3.3KΩ, 1%, 0603	
R11, 20	Resistor	2	0Ω, 0603	
R12	Resistor	1	47KΩ, 5%, 0603	
R15	Resistor	1	2.2KΩ, 1%, 0603	
R17	Resistor	1	1Ω, 0603	
R18	Resistor	1	100KΩ, 1%, 0603	
R19	Resistor	1	10KΩ, 5%, 0603	

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information

(W) SOIC Package
28-Pin Surface Mount, Wide Body

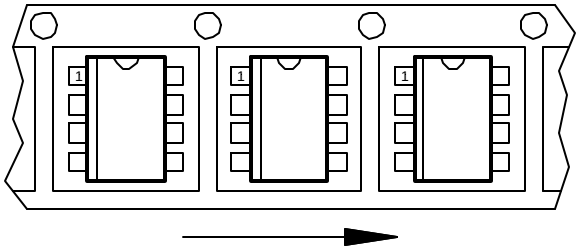


SYMBOL	28-PIN	
	MIN	MAX
A	17.73	17.93
B	1.27 BSC	
C	0.66 REF	
D	0.36	0.46
E	7.40	7.60
F	2.44	2.64
G	0.10	0.30
I	0.23	0.32
J	10.11	10.51
K	0°	8°
L	0.51	1.01
R	0.63	0.89
T	2.44	2.64

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
W	SOIC, Wide Body	28	27	1000	Fig A



Feed Direction
Figure A

International
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TAC Fax: (310) 252-7903
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IRU3033

8-PIN PWM SWITCHER AND LINEAR CONTROLLER IC

FEATURES

- LDO Controller allows the use of a low cost pass transistor for the I/O supply
- 8-Pin SOIC combines switching and linear controller
- Internal pre-regulator eliminates cross talk between switching and linear regulators
- Automatic shut down of the linear regulator when connected to the Vcc2 detect pin
- On-Board MOSFET Driver
- Fastest transient response of any controller method (0 to 100% Duty Cycle in 100ns)
- 1% Internal Voltage Reference
- Internal Under-Voltage Lockout protects MOSFET during start-up

APPLICATIONS

- Dual supply low voltage processor applications, such as: P55C™, CYRIX M2™, POWER PC™ and AMD K6™
- Simple 5V to 3.3V switcher for Pentium with AGP or Pentium II™ applications

DESCRIPTION

The IRU3033 IC combines a switching controller and a linear regulator controller all in a compact 8-pin surface mount package, providing a total solution for dual supply processor applications such as an Intel P55C™, AMD K6™, as well as Cyrix 6X86L™ and the M2™ processors. Typically in these applications a dual supply regulator converts 5V to 3.3V for I/O supply and a jumper programmable supply of 1.25V to 3.5V for Core supply. The linear regulator controller portion in the IRU3033 is a programmable controller allowing flexibility for the I/O regulator and has a minimum of 50mA drive current capability designed to provide ample current for an external pass transistor. The IC uses an internal regulator generated from the 12V supply to power the controller as well as the 12V supply to drive the power MOSFET, allowing a low cost N-channel MOSFET switch to be used. The IC also includes an error comparator for fast transient response, a precise voltage reference for setting the output voltage as well as a direct drive of the MOSFET for the minimum part count.

TYPICAL APPLICATION

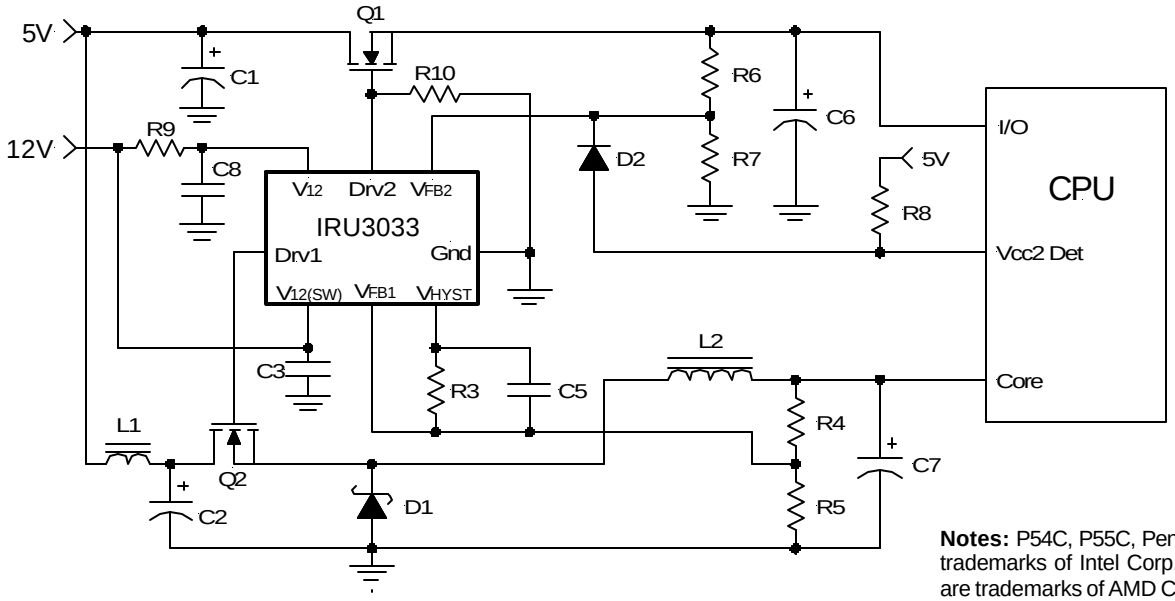


Figure 1 - Typical application of IRU3033 in a flexible mother board designed for Intel P55™, P54™, AMD K5, K6™ as well as Cyrix M1™ and M2™ applications.

Notes: P54C, P55C, Pentium II are trademarks of Intel Corp. K5 & K6 are trademarks of AMD Corp. Cyrix 6X86L, M1, M2 are trademarks of Cyrix Corp. Power PC is trademark of IBM Corp.

PACKAGE ORDER INFORMATION

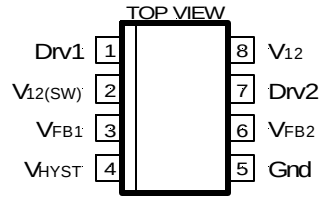
T_A (°C)	8-PIN PLASTIC SOIC (S)
0 To 70	IRU3033CS

ABSOLUTE MAXIMUM RATINGS

V_{12},$V_{12(SW)}$ Supply Voltages 20V
Fb Pin Voltages ..... -0.3V To 5V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature ..... 0°C To 150°C

PACKAGE INFORMATION

8-PIN PLASTIC SOIC (S)



θ_{JA} =160°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the following specification applies over V_{12}=$V_{12(SW)}$=12V and T_A=0 to 70°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Linear Controller Section	V_{FB2}					
Fb Voltage Initial Accuracy		T_J=25°C, Drv2=V_{FB2}, C_L=100µF	1.237	1.250	1.262	V
Fb Voltage Total Variation		Drv2=V_{FB2}, C_L=100µF	1.225	1.250	1.275	V
Fb Voltage Line Regulation		10<V_{12}<14V, Drv2=V_{FB2}, C_L=100µF		0.2		%
Fb Input Bias Current	I_{FB2}	V_{FB2}=1.25V	-1		+1	µA
Maximum Drive Current	$I_{DRV(max)}$	V_{FB2}=1V, V_{FB1}=1.5V		50		mA
V_{12} Supply Current	I_{12}	V_{FB2}=1V, V_{FB1}=1.5V, I_{DRV2}=0		5		mA
Switching Controller Section						
Fb Voltage Initial Accuracy	V_{FB1}	T_J=25°C	1.237	1.250	1.262	V
Fb Voltage Total Variation			1.225	1.250	1.275	V
Fb Voltage Line Regulation				0.2		%
Fb Input Bias Current	I_{FB1}	V_{FB1}=1.25V	-1		+1	µA
Min On Time		V_{FB1} is sq wave with 300ns on time and 2µs off time		800		ns
Min Off Time		V_{FB1} is sq wave with 300ns off time and 2µs on time		800		ns
V_{HYST} Pin Output-HI		I_{SOURCE}=500µA, V_{FB1}=1.5V	11			V
V_{HYST} Pin Output-LO		I_{SINK}=500µA, V_{FB1}=1V			1	V
Supply Current	$I_{12(SW)}$	V_{FB1}=1V, V_{FB2}=1.5V		10		mA
Maximum Duty Cycle	D_{MAX}	V_{FB1}=1V			100	%
Minimum Duty Cycle	D_{MIN}	V_{FB1}=1.5V	0			%
Gate Drive Rise/Fall Time	V_{GATE}	Load=IRL3303		70		ns

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	Drv1	The PWM output of the switching controller. This pin is a totem pole drive that is connected to the gate of the power MOSFET. A resistor may be placed from this pin to the gate in order to reduce switching noise.
2	$V_{12(SW)}$	This pin supplies the voltage to the PWM drive and hysteresis circuitry and it is connected to the 12V supply. A 1µF, high frequency capacitor must be connected from this pin to ground to provide the peak current for charging and discharging of the MOSFET.
3	V_{FB1}	A resistor divider from this pin to the output of the switching regulator and ground sets the Core supply voltage.
4	V_{HYST}	A resistor and a 10pF capacitor is connected from this pin to the V_{FB1} pin to set the output ripple voltage for the switching regulator.
5	Gnd	This pin is connected to the IC substrate and must be connected to the lowest potential in the system.
6	V_{FB2}	The feedback pin of the linear regulator. A resistor divider from this pin to the output of the linear regulator and ground sets the I/O supply voltage.
7	Drv2	The drive pin of the linear regulator. This pin controls the base of a transistor or the gate of a MOSFET acting as the series pass element for the linear regulator.
8	V_{12}	This pin provides the biasing for the chip and drive for the linear regulator controller. It is connected to 12V supply. A 10Ω resistor in series from this pin to the 12V supply and a 1µF, high frequency capacitor connected from this pin to ground is required to filter the switching noise of the switching regulator.

BLOCK DIAGRAM

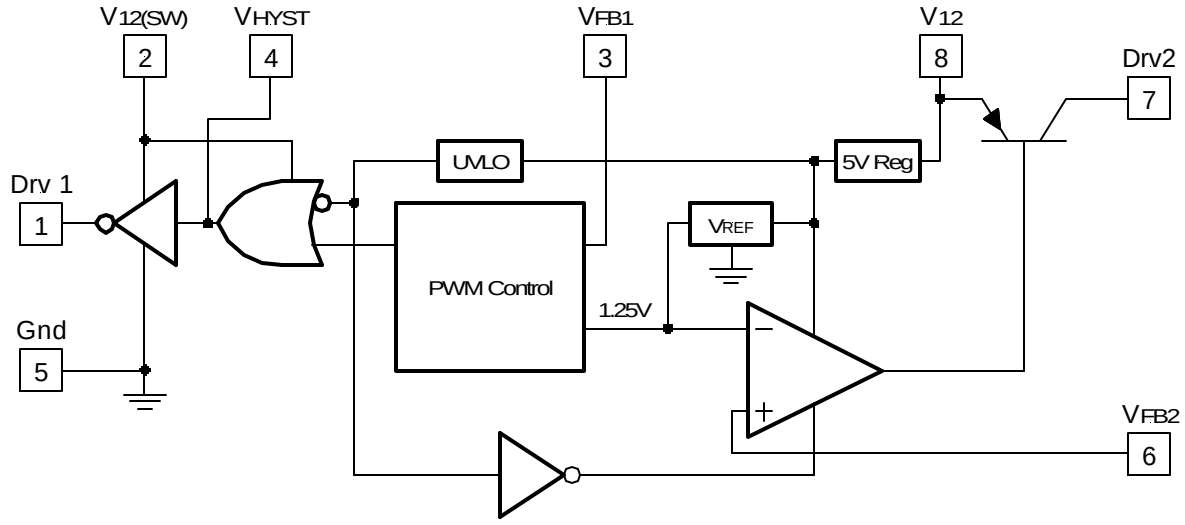


Figure 2 - Simplified block diagram of the IRU3033.

TYPICAL APPLICATION

Pentium Dual Supply Application

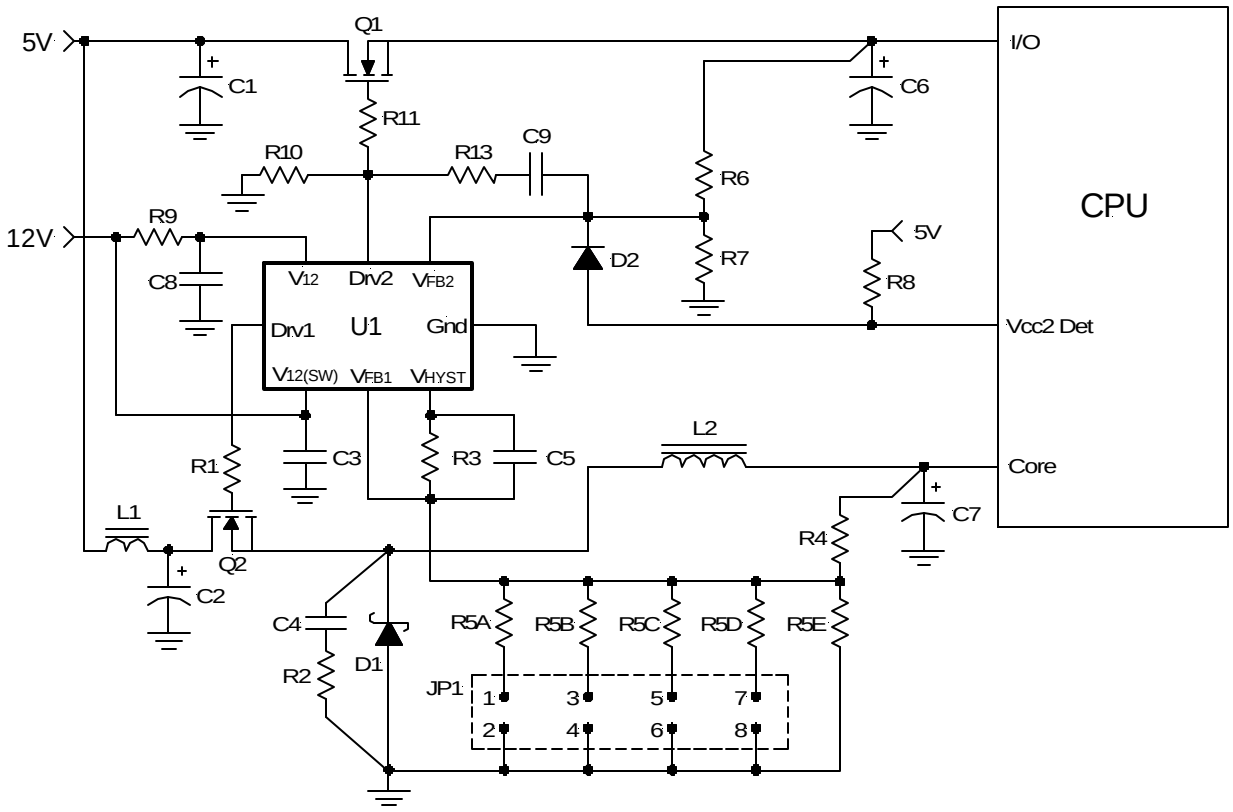


Figure 3 - Typical application of IRU3033 in a flexible motherboard with the 4-bit VID output voltage selection. This circuit uses a single jumper that programs the output voltage in 16 steps with 0.1V steps from 2V to 3.5V, designed for Intel P55™,P54™, AMD K5 & K6™ as well as Cyrix M1™ and M2™ applications. The Vcc2 Det pin automatically shuts down the I/O regulator when a single plane processor is dropped in the socket.

JP1 1-2	JP1 3-4	JP1 5-6	JP1 7-8	Output Voltage
0	0	0	0	3.5
0	0	0	1	3.4
0	0	1	0	3.3
0	0	1	1	3.2
0	1	0	0	3.1
0	1	0	1	3.0
0	1	1	0	2.9
0	1	1	1	2.8
1	0	0	0	2.7
1	0	0	1	2.6
1	0	1	0	2.5
1	0	1	1	2.4
1	1	0	0	2.3
1	1	0	1	2.2
1	1	1	0	2.1
1	1	1	1	2.0

0 = Jumper block is installed.
1 = Jumper block is not installed.

APPLICATION PARTS LIST

Pentium Dual Supply

Ref Desig	Description	Qty	Part #	Manuf
U1	LDO/Switcher IC	1	IRU3033CS (8-Pin SOIC)	IR
Q1	MOSFET	1	MTP3055 (TO-220)	Motorola
Q2	MOSFET	1	IRL3303 (TO-220) IRL3103S (TO-263) (Note 1)	IR
D2	Diode, GP	1	1N4148	
D1	Schottky Diode	1	MBR1045CT (TO-220) MBRB1545CT (TO-263) (Note1)	Motorola
L2	Inductor	1	Core: T50-18, L=4μH Turns: 10T, 18 AWG	Micro Metal (core)
L1	Inductor	1	L=2μH	
R1	Resistor	1	22Ω, 5%, SMT 1206 size	
R2	Resistor	1	10Ω, 5%, SMT 1206 size	
R3	Resistor	1	324KΩ, 1%, SMT 0805 size	
R4A*	Resistor	1	806Ω, 1%, SMT 0805 size	
R4B*	Resistor	1	90.9KΩ, 1%, SMT 0805 size	
R5A	Resistor	1	1.24KΩ, 1%, SMT 0805 size	
R5B	Resistor	1	2.49KΩ, 1%, SMT 0805 size	
R5C	Resistor	1	4.99KΩ, 1%, SMT 0805 size	
R5D	Resistor	1	1KΩ, 1%, SMT 0805 size	
R5E	Resistor	1	1.30KΩ, 1%, SMT 0805 size	
R6	Resistor	1	2 KΩ, 1%, SMT 0805 size	
R7	Resistor	1	1.21KΩ,1%, SMT 0805 size	
R8	Resistor	1	1 KΩ, 5%, SMT 0805 size	
R9	Resistor	1	10Ω, 5%, SMT 0805 size	
R10	Resistor	1	1KΩ, 5%, SMT 0805 size	
R11	Resistor	1	2.4KΩ, 5%, SMT 0805 size	
R13	Resistor	1	7.5KΩ, 5%, SMT 0805 size	
C1	Capacitor	1	6MV1500GX, 1500μF, 6.3V, Elect	
C2	Capacitor	1	6MV1500GX, 1500μF, 6.3V, Elect	Sanyo
C3	Capacitor	1	1μF, Ceramic, SMT 0805 size	
C4	Capacitor	1	470pF, Ceramic, SMT 0805 size	Sanyo
C5	Capacitor	1	10pF, Ceramic, SMT 0805 size	Sanyo
C6	Capacitor	1	6MV1500GX, 1500μF, 6.3V, Elect	Sanyo
C7	Capacitor	4	6MV1500GX, 1500μF, 6.3V, Elect	Sanyo
C8	Capacitor	1	1μF, Ceramic, SMT 0805 size	
C9	Capacitor	1	470p, Ceramic, SMT 0805 size	
HS1	Heat Sink	1	For MOSFET, 577002	Aavid
HS2	Heat Sink	1	For Schottky Diode , 577002	Aavid
HS3	Heat Sink	1	For Q1, 507222 (I/O curren<5A) 576602 (I/O current< 3.5A)	Aavid

*R4 is a parallel combination of R4A and R4B.

Note 1: For the applications where it is desirable to eliminate the heat sink, the IRL3103S for Q2 and MBR1545CT for D2 in TO-263 packages with minimum of 1" square copper pad can be used.

TYPICAL APPLICATION

5V to 3.3V for Pentium Application with AGP or Pentium II Application without ATX power supply Dual mode Operation between Switching or Linear mode.

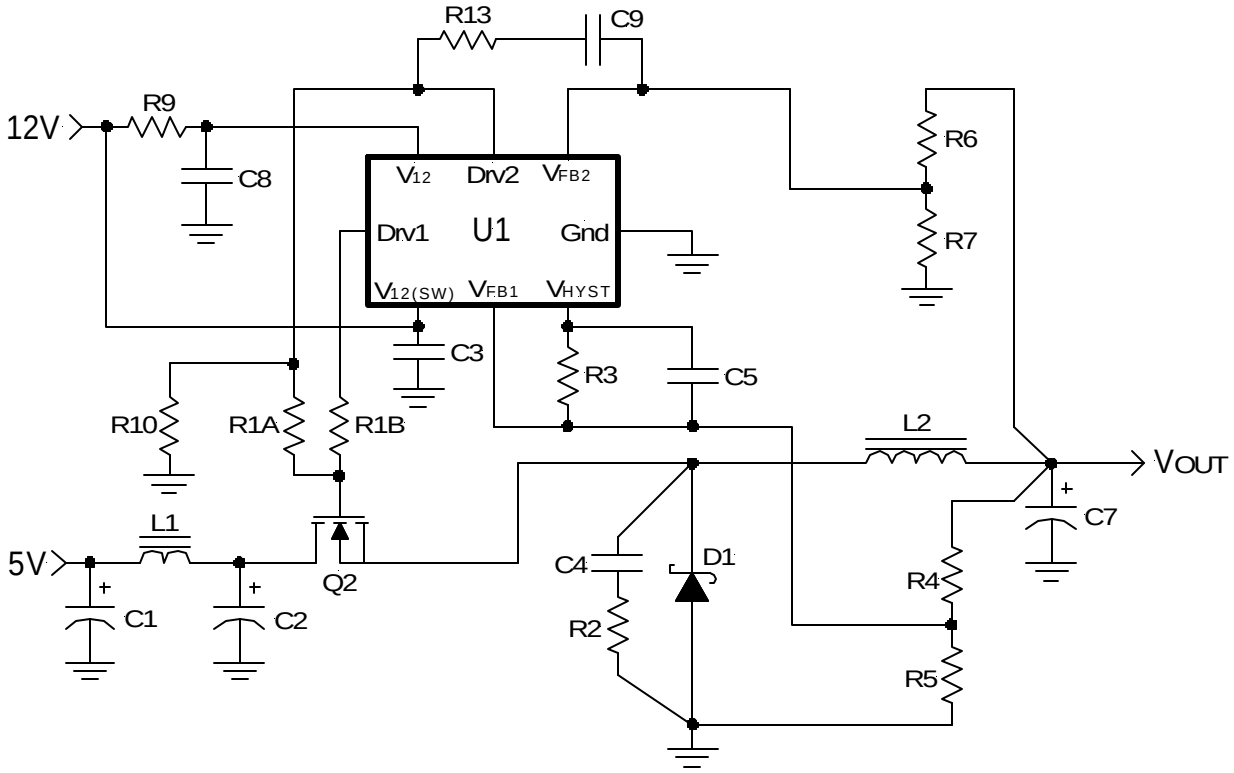


Figure 4 - This unique application of IRU3033 allows the designer to switch between Linear or Switching mode of operation using a single IC. This circuit has the flexibility to be used for low current operation in Linear mode for cost reasons and yet be able to operate in the Switching mode if the load current increases and the heat generated by the Linear operation will be an issue.

The table below describes the components that will be effected for the two modes of operation.

Mode of Operation	L1	L2	D1	C4	C5	R1A	R1B	R2	R3	R4	R5	R6	R7
Switching	V	V	V	V	V	O	V	V	V	V	V	V	O
Linear	S	S	O	O	O	V	O	O	O	V	O	V	V

V = See parts list for value S = Short O = Open

APPLICATION PARTS LIST

5V to 3.3V for Pentium Application with AGP or Pentium II Application without ATX power supply Dual mode Operation between Switching or Linear mode.

Ref Desig	Description	Qty	Part #	Manuf
U1	LDO/Switcher IC	1	IRU3033CS (8-Pin SOIC)	IR
Q2	MOSFET	1	IRL3303 (TO-220) IRL3103S (TO-263) (Note 1)	IR
D1	Schottky Diode	1	MBR1045CT (TO-220) MBRB1545CT (TO-263) (Note1)	Motorola
L2	Inductor	1	Core: T50-18,L=4μH Turns: 10T, 18 AWG	Micro Metal (core)
L1	Inductor	1	L=2μH	
R1A	Resistor	1	2.4KΩ, 5%, SMT 1206 size	
R1B	Resistor	1	22Ω, 5%, SMT 1206 size	
R2	Resistor	1	10Ω, 5%, SMT 1206 size	
R3	Resistor	1	249KΩ, 1%, SMT 0805 size	
R4	Resistor	1	1KΩ, 1%, SMT 0805 size	
R5	Resistor	1	576Ω, 1%, SMT 0805 size	
R6	Resistor	1	180Ω, 1%, SMT 0805 size	
R7	Resistor	1	100Ω, 1%, SMT 0805 size	
R9	Resistor	1	10Ω, 5%, SMT 1206 size	
R10	Resistor	1	1KΩ, 5%, SMT 1206 size	
R13	Resistor	1	7.5KΩ, 5%, SMT 1206 size	
C1, 2	Capacitor	2	6MV1500GX, 1500μF, 6.3V, Elect	Sanyo
C3	Capacitor	1	1μF, Ceramic, SMT 0805 size	
C4	Capacitor	1	470pF, Ceramic, SMT 0805 size	Sanyo
C5	Capacitor	1	10pF, Ceramic, SMT 0805 size	Sanyo
C7	Capacitor	1	6MV1500GX, 1500uF, 6.3V, Elect	Sanyo
C8	Capacitor	1	1μF, Ceramic, SMT 0805 size	
C9	Capacitor	1	470pF, Ceramic, SMT 0805 size	
HS1	Heat Sink	1	For MOSFET in Switching mode, 577002 For MOSFET in Linear mode: 507222 (3.3V current<5A), 576602 (3.3V current< 3.5A)	Aavid
HS2	Heat Sink	1	For Schottky Diode, 577002	Aavid

Note 1: For the applications where it is desirable to eliminate the heat sink, the IRL3103S for Q2 and MBR1545CT for D2 in TO-263 packages with minimum of 1" square copper pad can be used.

TYPICAL APPLICATION

5V to 3.3V for Pentium application with AGP or Pentium II application without ATX power supply switching mode operation.

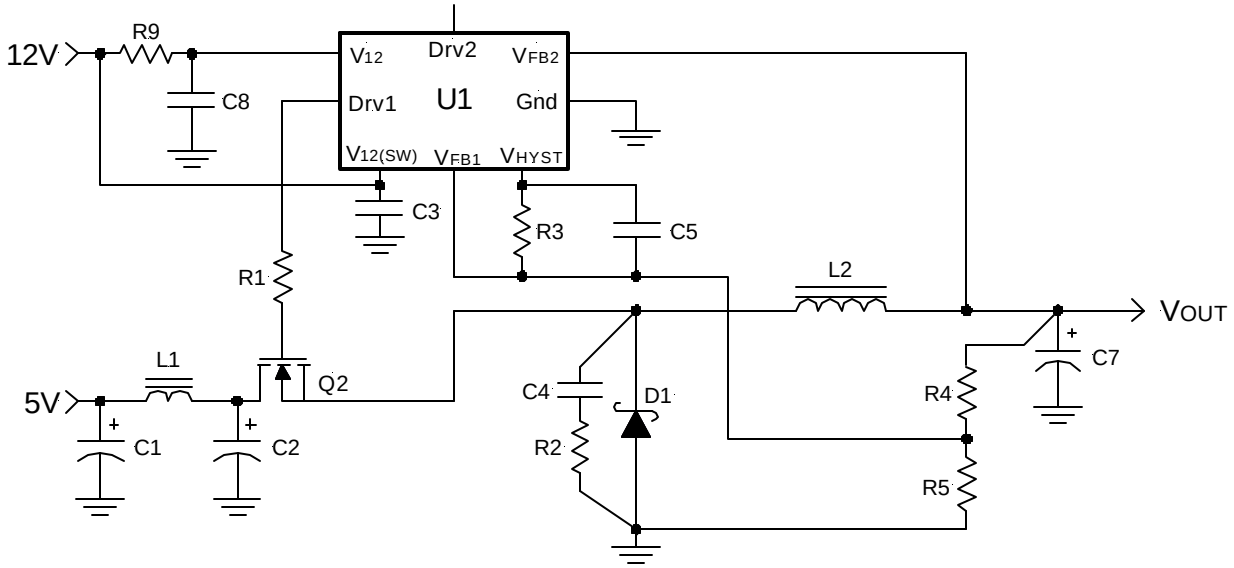


Figure 5 - The circuit in figure 4 is the application of the IRU3033 in a switching mode only. This circuit can be used to generate a low cost 5V to 3.3V for either Pentium application with AGP socket or in Pentium II applications where it is desirable to generate an accurate on board 3.3V supply.

Ref Desig	Description	Qty	Part #	Manuf
U1	LDO/Switcher IC	1	IRU3033CS (8-Pin SOIC)	IR
Q2	MOSFET	1	IRL3303 (TO-220) IRL3103S (TO-263) (Note 1)	IR
D1	Schottky Diode	1	MBR1045CT (TO-220) MBRB1545CT (TO-263) (Note 1)	Motorola
L2	Inductor	1	Core: T50-18, L=4μH Turns: 10T, 18 AWG	Micro Metal (core)
L1	Inductor	1	L=2μH	
R1	Resistor	1	22Ω, 5%, SMT 1206 size	
R9	Resistor	1	10Ω, 5%, SMT 0805 size	
R2	Resistor	1	10Ω, 5%, SMT 1206 size	
R3	Resistor	1	249KΩ, 1%, SMT 0805 size	
R4	Resistor	1	1KΩ, 1%, SMT 0805 size	
R5	Resistor	1	576Ω, 1%, SMT 0805 size	
C1, 2	Capacitor	2	6MV1500GX, 1500μF, 6.3V, Elect	Sanyo
C3	Capacitor	1	1μF, Ceramic, SMT 0805 size	
C4	Capacitor	1	470pF, Ceramic, SMT 0805 size	Sanyo
C5	Capacitor	1	10pF, Ceramic, SMT 0805 size	Sanyo
C7	Capacitor	1	6MV1500GX, 1500μF, 6.3V, Elect	Sanyo
C8	Capacitor	1	1μF, Ceramic, SMT 0805 size	
HS1	Heat Sink	1	For MOSFET, 577002	Aavid
HS2	Heat Sink	1	For Schottky Diode, 577002	Aavid

Note 1: For the applications where it is desirable to eliminate the heat sink, the IRL3103S for Q2 and MBR1545CT for D2 in TO-263 packages with minimum of 1" square copper pad can be used.

APPLICATION INFORMATION

Introduction

The IRU3033 device is an application specific product designed to provide an on board dual supply for the new generation of microprocessors requiring separate Core and I/O supplies. One of the processors fitting this requirement is the new Intel P55C™ multimedia microprocessor. Intel specifies a Core voltage of 2.8V nominal (±100mV max) with maximum Core supply current of 6A while the I/O supply is set for 3.3V with a maximum I/O current of 0.65A. However, in most applications the I/O regulator also provides the voltage for other IC functions such as the chip set, cache, etc. Typically a low cost solution such as a Low Dropout (LDO) Linear Regulator is selected to provide the I/O supply with the maximum designed current of 3A, keeping the power dissipation and the heat sink to a reasonable size. The Core supply regulator, however, if also selected to be a linear regulator, will be dissipating a maximum of 12.6W [(5V-2.8V)X5.7A] of power, which requires a substantial amount of heat sinking and perhaps forced air cooling in order to keep it operational. Some manufacturers suggest using two regulators to current share and therefore distribute the power dissipation equally between the regulators. The problem is that, in order to equally current share you need to sense both currents and force the slave regulator to match the master regulator. This can be done, but at the cost of the circuit complexity and much higher system cost and the total power dissipation is still the same. In fact, if the task is to design a flexible motherboard to accommodate the Cyrix 6X86L or their future MMX processors, then the power dissipation could easily reach 20W or more. At this power dissipation level the choice for a switching regulator approach becomes evident. However, the main reason that designers have always shied away from the switching regulators is their higher price tag and more complex circuit design that is associated with this kind of technique.

The IRU3033 device is designed to take advantage of the high efficiency of the switching regulator technique for the Core supply while maintaining the low cost LDO regulator for the I/O supply by offering both control functions in a single 8-pin surface mount package. In fact, as the typical application circuit shows, one can design a complete flexible motherboard using the IRU3033 and a few external components yielding a very low component count switching regulator and with an addition of a low cost pass transistor for the I/O supply provide a complete dual supply power solution.

LDO Section

The output voltage of the LDO regulator is externally programmable via 2 external resistors from 1.25V to 5V. The internal voltage reference of the LDO regulator is set to 1.25V and the output of the regulator can be programmed using the following formula:

$$V_{OUT} = (1 + R1/R2) \times V_{REF}$$

Where:
V_{REF} = 1.25V Typical
R1 = Resistor connected from V_{OUT} to the V_{FB2} pin of IRU3033.
R2 = Resistor connected from V_{FB2} pin to Gnd.

The IRU3033 requires the use of an output capacitor as part of the frequency compensation in order to be stable. Typical designs for the microprocessor applications use standard electrolytic capacitors with typical ESR in the range of 50 to 100mΩ and an output capacitance of 500 to 1000μF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU3033 takes advantage of this phenomena in making the overall regulator loop stable. For most applications a minimum of 100μF aluminum electrolytic capacitor such as Sanyo, MVGX series, Panasonic FA series or Nichicon PL series insures both stability and good transient response.

An external filtering is suggested as shown in the application circuit that reduces the switching ripple that might show in the output of the LDO regulator.

Switching Controller Operation

The operation of the switching controller is as follows:

After the power is applied, the output drive (Drv1) goes to 100% duty cycle and the current in the inductor charges the output capacitor causing the output voltage to increase. When output reaches a pre-programmed set point the feedback pin (V_{FB1}) exceeds 1.25V causing the output drive to switch low and the V_{HYST} pin to switch high which jumps the feedback pin higher than 1.25V resulting in a fixed output ripple which is given by the following equation:

$$\Delta Vo = (Rt/R_B) \times 11$$

Where:
Rt = Top resistor of the output divider, resistor connected from V_{OUT} to the V_{FB1} pin of IRU3033.
R_B = Bottom resistor of the divider, resistor connected from V_{FB1} pin to V_{HYST} pin.

For example, if Rt=1K and R_B=422K, then the output ripple is:

$$\Delta Vo = (1/422) \times 11 = 26mV$$

The advantage of fixed output ripple is that when the output voltage changes from 2V to 3.5V, the ripple voltage remains the same which is important in meeting the Intel maximum tolerance specification.

Switcher Output Voltage Setting

The output voltage of the switcher can be set using the following equations:

Assuming, Vo=3.38V and the selected output ripple is ≈ 1.3%(44mV) of the output voltage, a set of equations are derived that selects the resistor divider and the hysteresis resistor.

Assuming, Rt=1KΩ, 1%:

$$R_H = (11 \times Rt) / \Delta V$$

Where:
Rt = Top resistor of the resistor divider.
R_H = Hysteresis resistor connected between pins 3 and 4 of the IRU3033.
ΔVo = Selected output ripple (typically 1% to 2% of output voltage).

Assuming, ΔVo=44mV:

$$R_H = (11 \times 1000) / 0.044 = 250K\Omega$$

Select R_H = 249KΩ, 1%

The bottom resistor of the divider is then calculated using the following equations:

$$R_B = Rt / X$$

Where:
R_B = Bottom resistor of the divider
V_{REF} = 1.25V typical

$$X = [(Vo + \frac{\Delta Vo}{2})/V_{REF}] - 1$$

$$X = [(3.38 + \frac{0.044}{2})/1.25] - 1 = 1.72$$

$$R_B = 1000 / 1.72 = 580\Omega$$

Select R_B = 576Ω, 1%

Frequency Calculation

The IRU3033 frequency of operation is calculated using the following formula:

$$Fs = [(Vo \times (1 - D) \times ESR)] / (L \times \Delta Vo) \quad (MHz)$$

Where:
Vo = Output voltage (V)
D = Duty cycle
ESR = Output capacitor ESR (V)
L = Output inductance (μH)
ΔVo = Output ripple voltage (V)

For our example:

$$D \approx (Vo + Vf) / V_{IN}$$

Where:
Vf = Forward voltage drop of the Schottky diode.

$$D = (3.38 + 0.5) / 5 = 0.78$$

The ESR=18mΩ for 2 of the Sanyo 1500μF, 6MV1500GX caps. If L=3.5μH then, Fs is calculated as follows:

$$Fs = \frac{[(3.38 \times (1 - 0.78) \times 0.018)]}{(3.5 \times 0.044)} = 0.087MHz$$

Fs = 87KHz

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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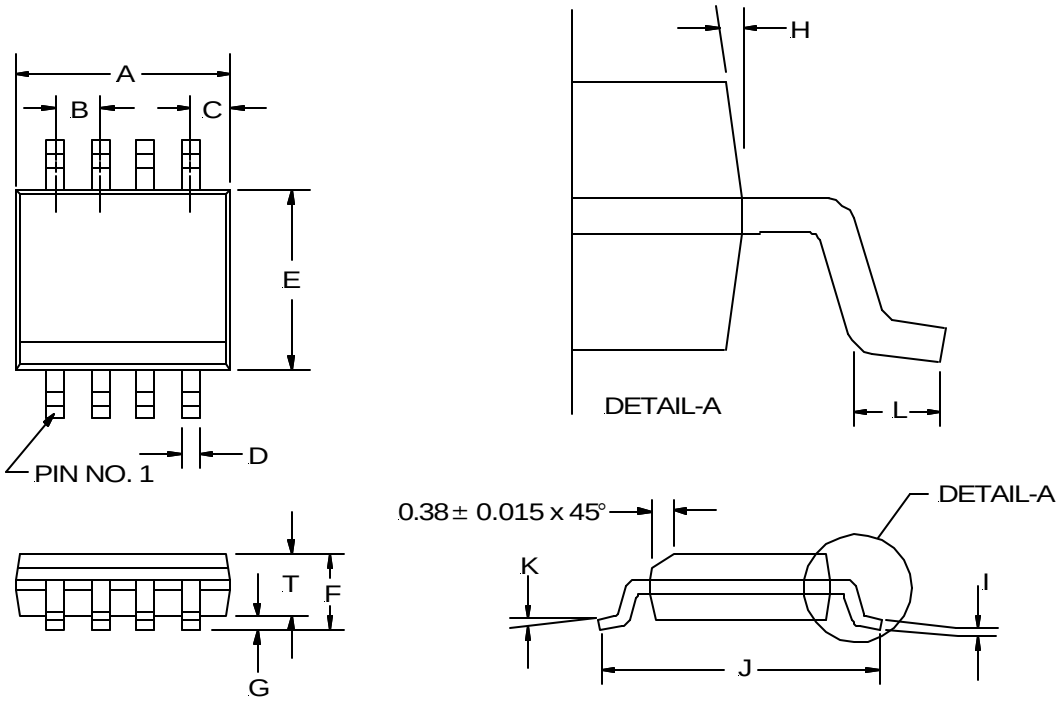
(S) SOIC Package
8-Pin Surface Mount, Narrow Body

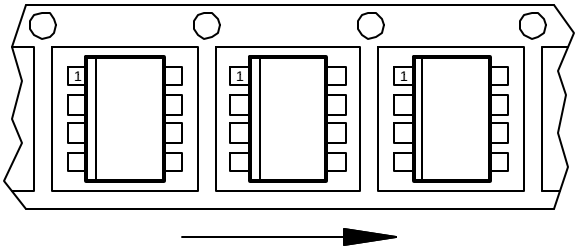


8-PIN		
SYMBOL	**MIN**	**MAX**
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
S	SOIC, Narrow Body	8	95	2500	Fig A



Feed Direction
Figure A

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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IRU3034

8-PIN PWM SWITCHER CONTROLLER IC WITH CURRENT LIMITING

FEATURES

- 8-Pin SOIC switching controller with HICCUP current limiting reduces diode power dissipation to less than 1% of normal operation
- Soft-Start capacitor allows for smooth output voltage ramp up
- On-Board MOSFET Driver
- Fastest transient response of any controller method. (0 to 100% Duty Cycle in 100ns)
- 1% Internal Voltage Reference
- Internal Under-Voltage Lockout protects MOSFET during start-up

APPLICATIONS

- Dual supply low voltage processor applications, such as: P55C™, CYRIX M2™, POWER PC™ and AMD K6™
- Simple 5V to 3.3V switcher for Pentium with AGP or Pentium II™ applications

DESCRIPTION

The IRU3034 IC provides a low cost switching controller with true short circuit protection all in a compact 8-pin surface mount package, providing a low cost switching solution for dual supply processor applications that require switching regulator for the 3.3V supply such as the applications with AGP on-board. Typically in these applications, a dual supply regulator converts 5V to 3.3V for I/O supply and a jumper programmable supply of 1.25V to 3.5V for Core supply. The IC uses an internal regulator generated from the 12V supply to power the controller as well as the 12V supply to drive the power MOSFET, allowing a low cost N-channel MOSFET to be used. The IC also includes an error comparator for fast transient response, a precise voltage reference for setting the output voltage as well as a direct drive of the MOSFET for the minimum part count.

TYPICAL APPLICATION

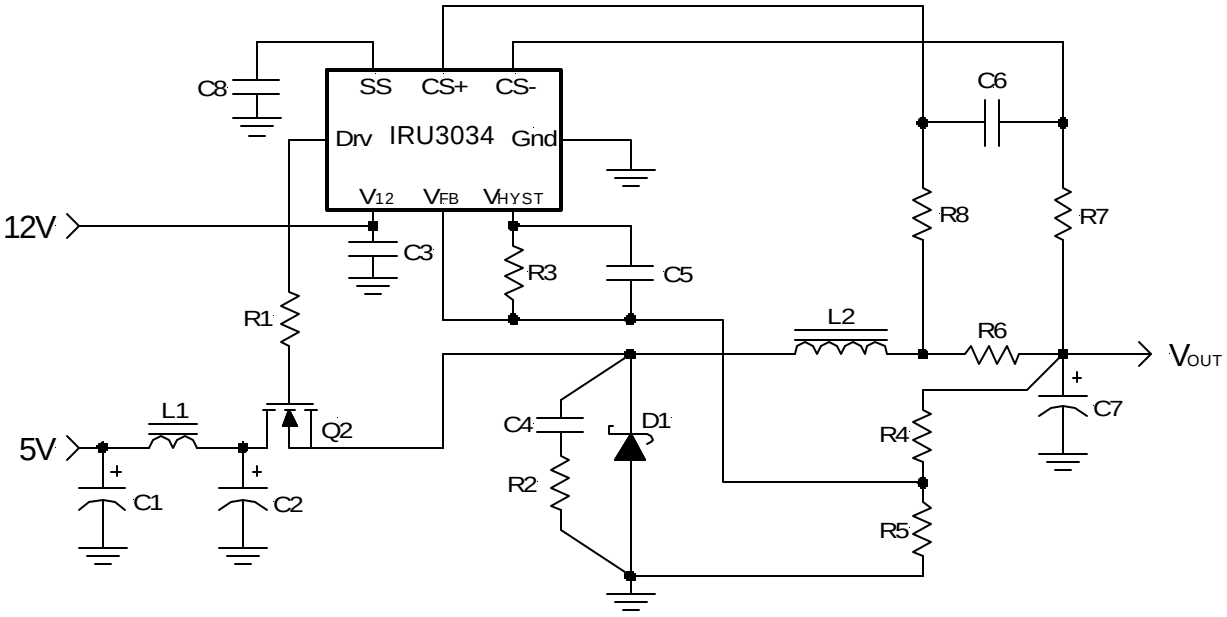


Figure 1 - Typical application of IRU3034.

Notes: P55C, Pentium II are trademarks of Intel Corp. K5 & K6 are trademarks of AMD corp. Cyrix 6X86L, M1, M2 are trademarks of Cyrix Corp. Power PC is trademark of IBM Corp.

PACKAGE ORDER INFORMATION

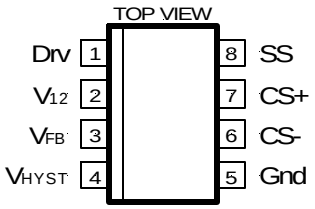
T_A (°C)	8-PIN PLASTIC SOIC (S)
0 To 70	IRU3034CS

ABSOLUTE MAXIMUM RATINGS

V_{12} Supply Voltages 20V
Fb Pin Voltages ..... -0.3V To 5V
Storage Temperature Range ..... -65 To 150°C
Operating Junction Temperature ..... 0 To 150°C

PACKAGE INFORMATION

8-PIN PLASTIC SOIC (S)



θ_{JA} =160°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the following specification applies over V_{12}=12V and T_A=0 to 70°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Fb Voltage Initial Accuracy	V_{FB}	T_J=25°C	1.237	1.250	1.262	V
Fb Voltage Total Variation			1.225	1.250	1.275	V
Fb Voltage Line Regulation				0.2		%
Fb Input Bias Current	I_{FB}	V_{FB}=1.25V	-1		+1	µA
Minimum On Time		V_{FB} is sq wave with 300ns on time and 2µs off time		800		ns
Minimum Off Time		V_{FB} is sq wave with 300ns off time and 2µs on time		800		ns
V_{HYST} Pin Output-HI		I_{SOURCE}=500µA, V_{FB}=1.5V	11			V
V_{HYST} Pin Output-LO		I_{SINK}=500µA, V_{FB}=1V			1	V
Supply Current	$I_{12(SW)}$	V_{FB}=1V		10		mA
Maximum Duty Cycle	D_{MAX}	V_{FB}=1V			100	%
Minimum Duty Cycle	D_{MIN}	V_{FB}=1.5V	0			%
Gate Drive Rise/Fall Time	V_{GATE}	Load=IRL3303		70		ns
CL Threshold Current	I_{CL}	CS+, CS- from 1.3V to 3.7V		20		µA
CS Comp Common Mode		V_{CS+}=V_{CS-}	0		4.5	V
Soft-Start Current				10		µA

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	Drv	The PWM output of the switching controller. This pin is a totem pole drive that is connected to the gate of the power MOSFET. A resistor may be placed from this pin to the gate in order to reduce switching noise.
2	V_{12}	This pin supplies the voltage to the PWM drive and hysteresis circuitry and it is connected to the 12V supply. A 1µF, high frequency capacitor must be connected from this pin to ground to provide the peak current for charging and discharging of the MOSFET.
3	V_{FB}	A resistor divider from this pin to the output of the switching regulator and ground sets the Core supply voltage.
4	V_{HYST}	A resistor and a 10pF capacitor is connected from this pin to the V_{FB} pin to set the output ripple voltage for the switching regulator.
5	Gnd	This pin is connected to the IC substrate and must be connected to the lowest potential in the system.
6	CS-	This pin is connected to the minus side of the external current sense resistor. An internal current source together with an external resistor in series with this pin programs the current limit threshold voltage. This voltage divided by the external current sense resistor sets the current limit threshold.
7	CS+	This pin is connected to the plus side of the external current sense resistor. A resistor in series with this pin and a capacitor connected between this pin and pin 6 provides a high frequency filtering for the noise spikes of turn on and turn off switching.
8	SS	This pin provides the soft-start for the regulator during power up. It also sets a long off time when the converter goes into current limiting, providing low duty cycle for the catch diode allowing it to survive during short circuit.

BLOCK DIAGRAM

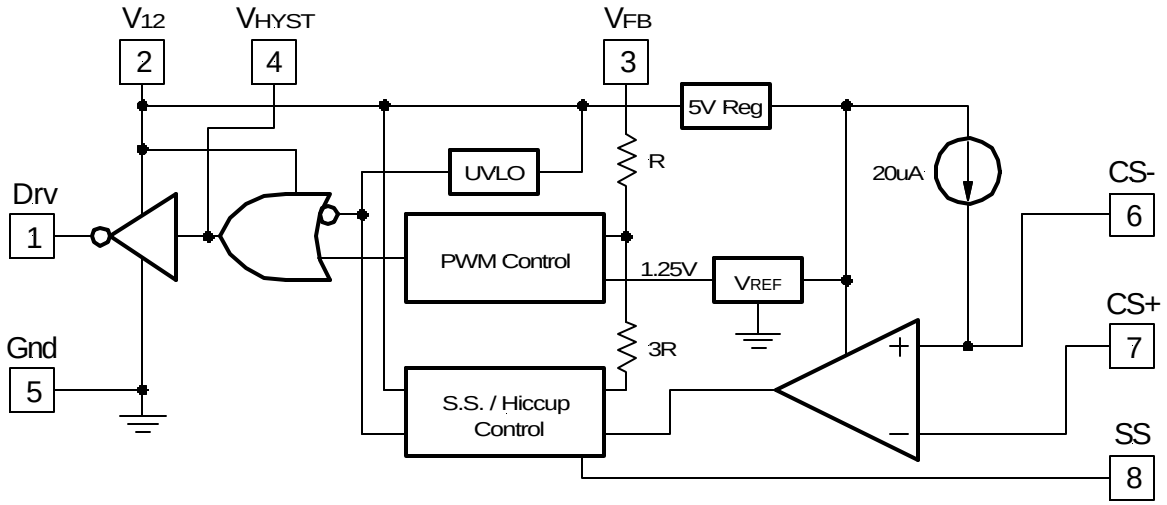


Figure 2 - Simplified block diagram of the IRU3034.

TYPICAL APPLICATION

Pentium Core Supply Application (IRU3034 and IRU3033 Dual Layout)
Low Cost 4-Bit VID

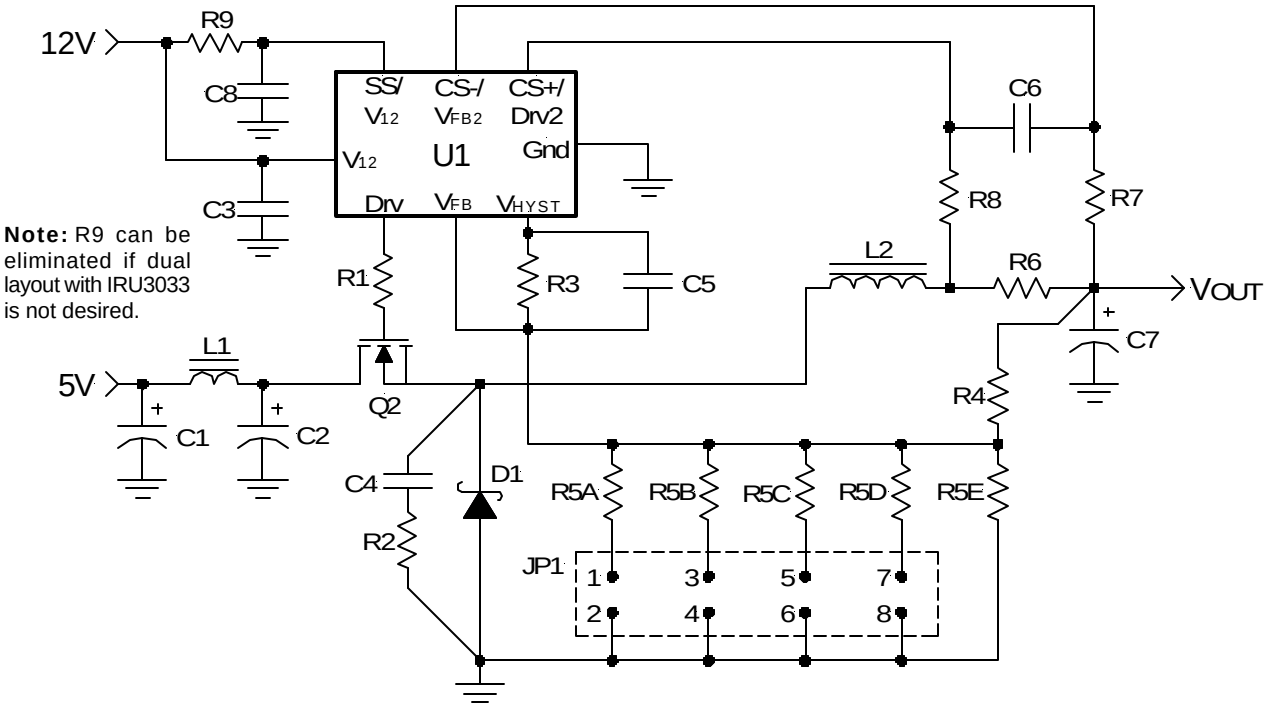


Figure 3 - Typical application of IRU3034 in a flexible motherboard with the 4-bit VID output voltage selection. This circuit is done using a dual layout with the IRU3033 part. The advantage of this circuit is that it uses a single jumper that programs the output voltage in 16 steps with 0.1V steps from 2V to 3.5V, designed for Intel P55, P54, AMD K5 & K6 as well as Cyrix M1 and M2 applications.

JP1 1-2	**JP1** 3-4	**JP1** 5-6	**JP1** 7-8	**Output Voltage**
0	0	0	0	3.5
0	0	0	1	3.4
0	0	1	0	3.3
0	0	1	1	3.2
0	1	0	0	3.1
0	1	0	1	3.0
0	1	1	0	2.9
0	1	1	1	2.8
1	0	0	0	2.7
1	0	0	1	2.6
1	0	1	0	2.5
1	0	1	1	2.4
1	1	0	0	2.3
1	1	0	1	2.2
1	1	1	0	2.1
1	1	1	1	2.0

0 = Jumper block is installed.
1 = Jumper block is not installed.

PENTIUM CORE SUPPLY APPLICATION PARTS LIST

(IRU3034 and IRU3033 Dual Layout) Low Cost 4-Bit VID

Ref Desig	Description	Qty	Part #	Manuf
U1	LDO/Switcher IC	1	IRU3034CS (8-Pin SOIC)	IR
Q2	MOSFET	1	IRL3303 (TO-220) IRL3103S (TO-263) (Note 1)	IR
D1	Schottky Diode	1	MBR1045CT (TO-220) MBRB1545CT (TO-263) (Note1)	Motorola
L2	Inductor	1	Core: T50-18, L=4μH Turns: 10T, 18 AWG	Micro Metal (core)
L1	Inductor	1	L=2μH	
R1	Resistor	1	22Ω, 5%, SMT 1206 size	
R2	Resistor	1	10Ω, 5%, SMT 1206 size	
R3	Resistor	1	324KΩ, 1%, SMT 0805 size	
R4A *	Resistor	1	806Ω, 1%, SMT 0805 size	
R4B *	Resistor	1	90.9KΩ, 1%, SMT 0805 size	
R5A	Resistor	1	1.24KΩ, 1%, SMT 0805 size	
R5B	Resistor	1	2.49KΩ, 1%, SMT 0805 size	
R5C	Resistor	1	4.99KΩ, 1%, SMT 0805 size	
R5D	Resistor	1	10KΩ, 1%, SMT 0805 size	
R5E	Resistor	1	1.30Ω, 1%, SMT 0805 size	
R6	Resistor	1	5mΩ, 5%, 2W	
R7	Resistor	1	4.99KΩ, 1%, SMT 0805 size	
R8	Resistor	1	4.7KΩ, 5% for IRU3034, open for 3033	
R9	Resistor	1	Open for IRU3034, 10Ω for IRU3033	
C1	Capacitor	1	6MV1500GX, 1500μF, 6.3V, Elect	
C2	Capacitor	1	6MV1500GX, 1500μF, 6.3V, Elect	Sanyo
C3	Capacitor	1	1μF, Ceramic, SMT 0805 size	
C4	Capacitor	1	470pF, Ceramic, SMT 0805 size	Sanyo
C5	Capacitor	1	10pF, Ceramic, SMT 0805 size	Sanyo
C7	Capacitor	4	6MV1500GX, 1500μF, 6.3V, Elect	Sanyo
C8	Capacitor	1	0.047μF for 3034 , 0.1μF for IRU3033	
C6	Capacitor	1	4700pF for IRU3034, open for IRU3033	
HS1	Heat Sink	1	For MOSFET, 577002	Aavid
HS2	Heat Sink	1	For Schottky Diode, 577002	Aavid

*R4 is a parallel combination of R4A and R4B.

Note: For the applications where it is desirable to eliminate the heat sink, the IRL3103S for Q2 and MBR1545CT for D2 in TO-263 packages with minimum of 1" square copper pad can be used.

TYPICAL APPLICATION

5V to 3.3V for Pentium Application with AGP or Pentium II Application without ATX power supply Switching mode Operation. (IRU3034 and IRU3033 Dual Layout)

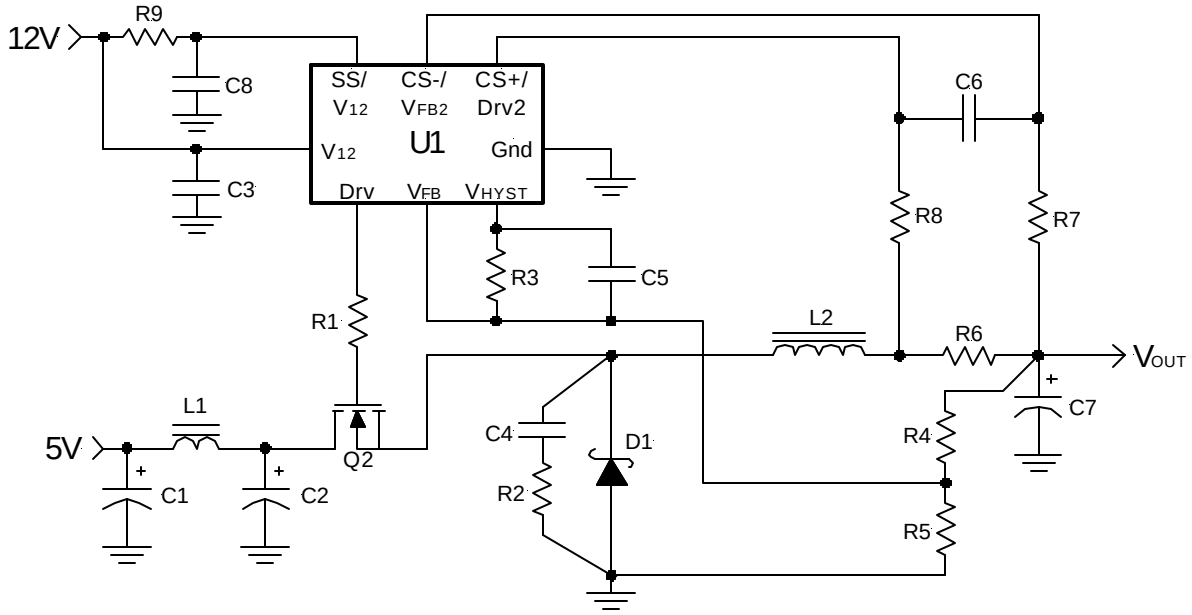


Figure 4 - The circuit in figure 4 is the application of the IRU3034 which is done using a dual layout with IRU3033 in a switching mode only. This circuit can be used to generate a low cost 5V to 3.3V for either Pentium application with AGP socket or in Pentium II applications where it is desirable to generate an accurate on-board 3.3V supply.

Ref Desig	Description	Qty	Part #	Manuf
U1	LDO/Switcher IC	1	IRU3034CS (8-Pin SOIC)	IR
Q2	MOSFET	1	IRL3303 (TO-220) IRL3103S (TO-263) (Note 1)	IR
D1	Schottky Diode	1	MBR1045CT (TO-220) MBRB1545CT (TO-263) (Note1)	Motorola
L2	Inductor	1	Core: T50-18, L=4μH Turns: 10T, 18 AWG	Micro Metal (core)
L1	Inductor	1	L=2μH	
R1	Resistor	1	22Ω, 5%, SMT 1206 size	
R9	Resistor	1	Open for IRU3034, 10Ω for IRU3033	
R2	Resistor	1	10Ω, 5%, SMT 1206 size	
R3	Resistor	1	249KΩ, 1%, SMT 0805 size	
R4	Resistor	1	1KΩ, 1%, SMT 0805 size	
R5	Resistor	1	576Ω, 1%, SMT 0805 size	
R6	Resistor	1	5mΩ, 5%, 2W	
R7	Resistor	1	4.99KΩ, 1%, SMT 0805 size	
R8	Resistor	1	4.7KΩ, 5% for IRU3034, Open for IRU3033	
C1, 2	Capacitor	2	6MV1500GX, 1500μF, 6.3V, Elect	Sanyo
C3	Capacitor	1	1μF, Ceramic, SMT 0805 size	
C4	Capacitor	1	470pF, Ceramic, SMT 0805 size	Sanyo
C5	Capacitor	1	10pF, Ceramic, SMT 0805 size	Sanyo
C6	Capacitor	1	4700pF for IRU3034, Open for IRU3033	
C7	Capacitor	2	6MV1500GX, 1500μF, 6.3V, Elect	Sanyo
C8	Capacitor	1	0.047μF for IRU3034 , 0.1μF for 3033	
HS1	Heat Sink	1	For MOSFET, 577002	Aavid
HS2	Heat Sink	1	For Schottky Diode, 577002	Aavid

Note: For the applications where it is desirable to eliminate the heat sink, the IRL3103S for Q2 and MBR1545CT for D2 in TO-263 packages with minimum of 1" square copper pad can be used.

TYPICAL APPLICATION

5V to 3.3V with loss-less short circuit protection (Output UVLO detection)

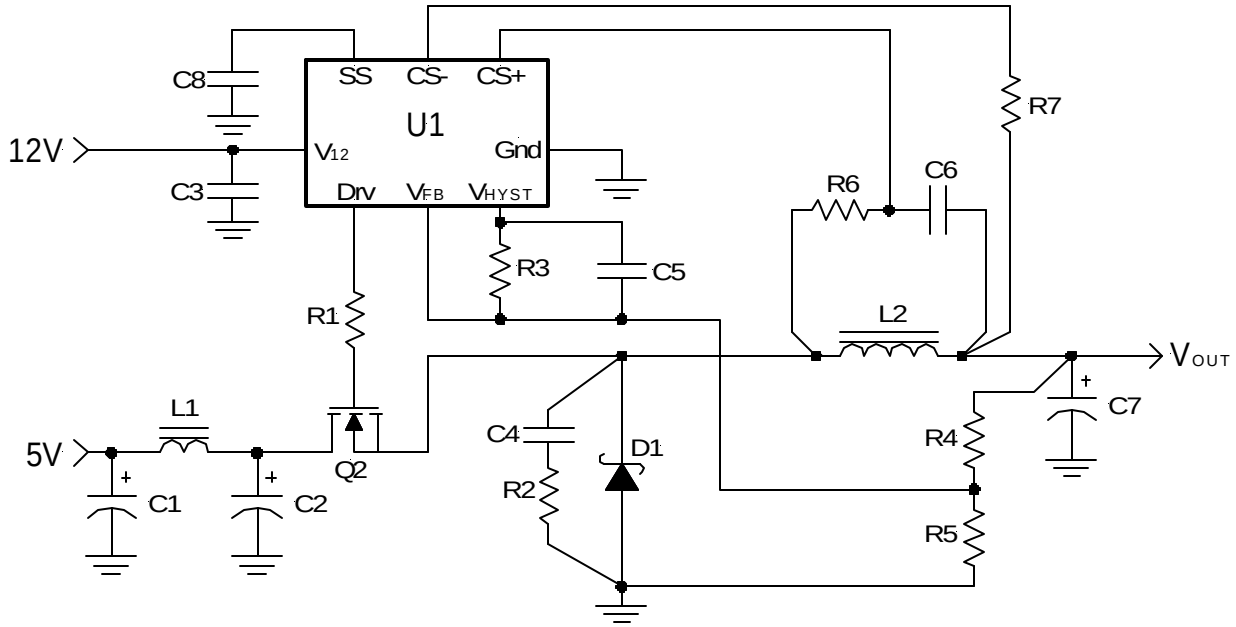


Figure 5 - The circuit in figure 5 is designed to provide loss-less output short detection by detecting the DC voltage across the inductor and shutting down the MOSFET and entering HICCUP mode. Note that the current limit point is a function of the inductor resistance and in this application with approximately 8mΩ resistance the peak CL is set at 10A. See application note on how to set the current limiting threshold.

Ref Desig	Description	Qty	Part #	Manuf
U1	Switcher IC	1	IRU3034CS (8-Pin SOIC)	IR
Q2	MOSFET	1	IRL3303 (TO-263)	IR
D1	Schottky Diode	1	PBYR735 (Axial Thru Hole pkg) PBYR1035B (SMT, T-263 pkg)	 Motorola
L2	Inductor	1	Core: T50-18, L=4μH Turns: 7T, 18 AWG	Micro Metal (core)
L1	Inductor	1	L=μH	
R1,2	Resistor	2	10Ω, 5%, SMT	
R3	Resistor	1	182KΩ, 1%, SMT	
R4	Resistor	1	1KΩ, 1%, SMT	
R5	Resistor	1	576Ω, 1%, SMT	
R7	Resistor	1	3.83KΩ, 1%, SMT	
R6	Resistor	1	1KΩ, 1%, SMT	
C1	Capacitor	1	470μF, Elect	
C2	Capacitor	1	6MV1000GX, 1000μF, 6.3V, Elect	Sanyo
C3	Capacitor	1	1μF, Ceramic, SMT	
C5	Capacitor	1	10pF, Ceramic, SMT	Sanyo
C6	Capacitor	1	0.1μF	
C7	Capacitor	2	6MV1000GX, 1000μF, 6.3V, Elect	Sanyo
C8	Capacitor	1	0.047μF	

APPLICATION INFORMATION

Introduction

The IRU3034 device is an application specific product designed to provide an on-board switching supply for the new generation of microprocessors requiring separate Core and I/O supplies where the load current demand from the I/O supply requires this regulator to also be a switching regulator such as the motherboard applications with AGP slot or the Pentium II with on-board 5V to 3.3V converter. The IRU3034 provides an easy and low cost switching regulator solution for Vcore and 3.3V supplies with true short circuit protection.

Switching Controller Operation

The operation of the switching controller is as follows:

After the power is applied, the output drive pin (Drv) goes to 100% duty cycle and the current in the inductor charges the output capacitor causing the output voltage to increase. When output reaches a pre-programmed set point the feedback pin (V_{FB}) exceeds 1.25V causing the output drive to switch Low and the V_{HYST} pin to switch High which jumps the feedback pin higher than 1.25V resulting in a fixed output ripple which is given by the following equation:

$$\Delta Vo = (Rt/Rh) \times 11$$

Where:
Rt = Resistor connected from V_{OUT} to the V_{FB} pin of IRU3034.
Rh = Resistor connected from V_{FB} pin to V_{HYST} pin.

For example, if Rt=1K and Rh=422K, then the output ripple is:

$$\Delta Vo = (1/422) \times 11 = 26mV$$

The advantage of fixed output ripple is that when the output voltage changes from 2V to 3.5V, the ripple voltage remains the same which is important in meeting the Intel maximum tolerance specification.

Soft-Start

The soft-start capacitor must be selected such that during the start-up when the output capacitors are charging up, the peak inductor current does not reach the current limit threshold. A minimum of 0.1µF capacitor insures this for most applications. During start-up the soft-start capacitor is charged up to approximately 6V keeping the output shutdown before an internal 10µA current source start discharging the soft-start capacitor which slowly ramps up the inverting input of the PWM comparator, V_{FB}. This insures the output to ramp up at the same rate as the soft-start cap thereby limiting the input current. For example, with 0.1µF and the 10µA internal current source the ramp up rate is:

$$(\Delta V/\Delta t) = I/Css = 10/0.1 = 100V/s \text{ or } 0.1V/ms$$

Assuming that the output capacitance is 6000µF, the peak input current will be:

$$I_{IN(pk)} = Css \times (\Delta V/\Delta t) = 6000\mu F \times (0.1V/ms) = 0.6A$$

The soft start capacitor also provides a delay in the turn on of the output which is given by:

$$T_D = Css \times K$$

Where:
K = 30ms/µF

For example for Css=0.1µF,

$$T_D = 0.1 \times 30 = 3ms$$

Switcher Current Limit Protection

The IRU3034 uses an external current sensing resistor and compares the voltage drop across it to a programmed voltage which is set externally via a resistor (R_{CL}) placed between the CS- terminal of the IC and V_{OUT}. Once the voltage across the sense resistor exceeds the threshold, the soft-start capacitor pulls up to 12V, pulling up the inverting pin of the error comparator higher than non-inverting which causes the external MOSFET to shut off. At this point the CS comparator changes its state and pulls the soft-start capacitor to Vcc which is 12V and shutting the PWM drive. After the output drive is turned off, an internal 10µA current source slowly discharges the soft-start capacitor to approximately 5.7V, before the output starts to turn back on causing a long delay before the MOSFET turns back on. This delay causes the catch diode to cool off between the current limit cycles allowing the converter to survive a short circuit condition. An example is given below as how to select the current limiting components. Assuming the desired current limit point is set to be 20A and the current sense resistor Rs=5mΩ, then the current limit programming resistor, R_{CL} is calculated as:

$$Vcs = I_{CL} \times Rs = 20 \times 0.005 = 0.1V$$

$$R_{CL} = Vcs/I_B = (0.1V)/(20\mu A) = 5K\Omega$$

Where:
I_B = 20µA is the internal current source of IRU3034

The peak power dissipated in the CS resistor is:

$$Ppk = I_{CL}^2 \times Rs = 20^2 \times 0.005 = 2W$$

However, the average power dissipated is much lower than 2W due to the long off time caused by the hiccup circuit of IRU3034. The average power is in fact the short circuit period divided by the short circuit period plus the off time or "Hiccup" period. For example, if the short circuit lasts for Tsc=100µs before the IRU3034 enters hiccup, the average power is calculated as:

$$P_{AVG} = 0.5 \times Ppk \times Dsc$$

Where:
Dsc = Tsc / T_{HCP}
T_{HCP} = Css × M
M = 200ms/µF
Css = The soft-start capacitor

For example:
For Css=0.1µF and Tsc=500µs=0.5ms

$$T_{HCP} = 0.1 \times 200 = 20ms$$

$$P_{AVG} = 0.5 \times 2 \times (0.5/20) = 25mW$$

Without "Hiccup" technique, the power dissipation of the resistor is 2W.

Switcher Output Voltage Setting
The output voltage can be set using the following equations:

Assuming, Vo=3.38V and the selected output ripple is ≈ 1.3%(44mV) of the output voltage, a set of equations are derived that selects the resistor divider and the hysteresis resistor:

Assuming, Rt = 1KΩ, 1%:

$$R_H = (11 \times Rt) / \Delta Vo$$

Where:
Rt = Top resistor of the resistor divider
R_H = Hysteresis resistor connected between pins 3 and 4 of the IRU3034
ΔVo = Selected output ripple (typically 1% to 2% of output voltage)

Assuming, ΔVo=44mV:

$$R_H = (11 \times 1000) / 0.044 = 250K\Omega$$

Select R_H = 249KΩ, 1%

The bottom resistor of the divider is then calculated using the following equations:

$$R_B = Rt / X$$

Where:
R_B = Bottom resistor of the divider
V_{REF} = 1.25V Typical

$$X = [(Vo + (\Delta Vo/2)) / V_{REF}] - 1$$

$$X=[(3.38+ (0.044/2)) / 1.25] - 1 = 1.72$$

$$R_B = 1000 / 1.72 = 580\Omega$$

Select R_B = 576Ω, 1%

Frequency Calculation
The IRU3034 frequency of operation is calculated using the following formula:

$$Fs = [(Vo \times (1-D) \times ESR)] / (L \times \Delta Vo) \quad (MHz)$$

Where:
Vo = Output voltage (V)
D = Duty cycle
ESR = Output capacitor ESR (V)
L = Output inductance (µH)
ΔVo = Output ripple voltage (V)

For our example:

$$D \approx (Vo + Vf) / V_{IN}$$

Where:
Vf = Forward voltage drop of the Schottky diode.

$$D = (3.38 + 0.5) / 5 = 0.78$$

The ESR=18mΩ for 2 of the Sanyo 1500µF, 6MV1500GX caps. If L=3.5µH then, Fs is calculated as follows:

$$Fs = \frac{[(3.38 \times (1-0.78) \times 0.018)]}{(3.5 \times 0.044)} = 0.087$$

Fs = 87KHz

TYPICAL PERFORMANCE CHARACTERISTICS

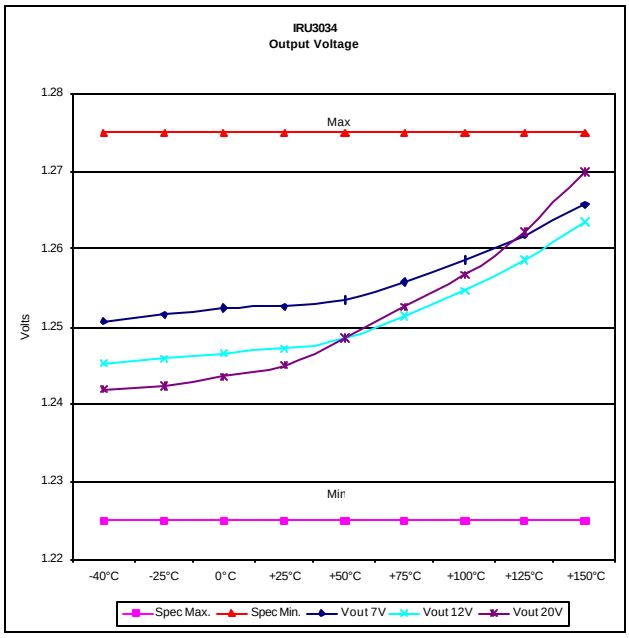


Figure 6 - Output Voltage.

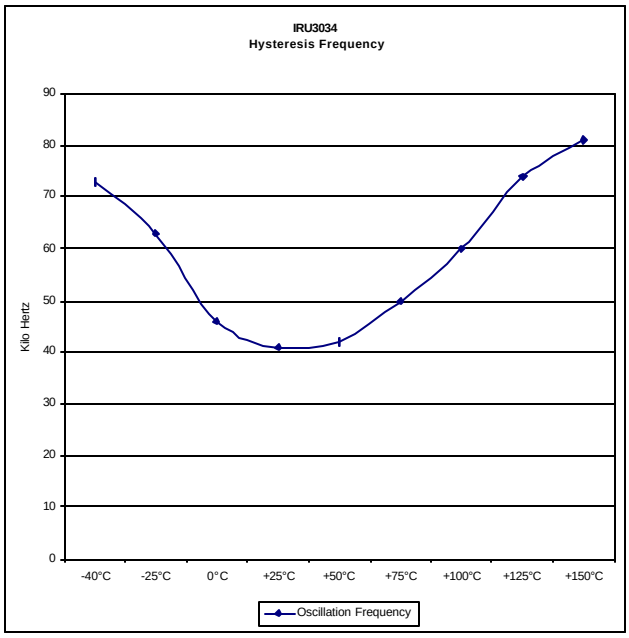


Figure 7 - Hysteresis Frequency.

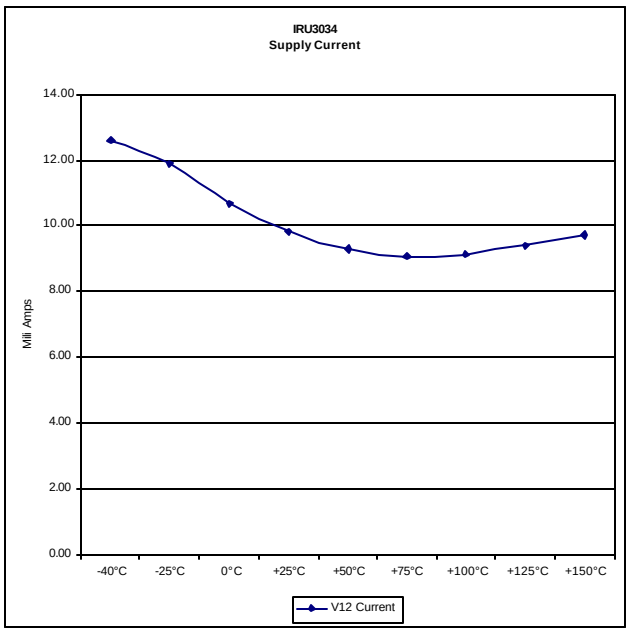


Figure 8 - Supply Current.

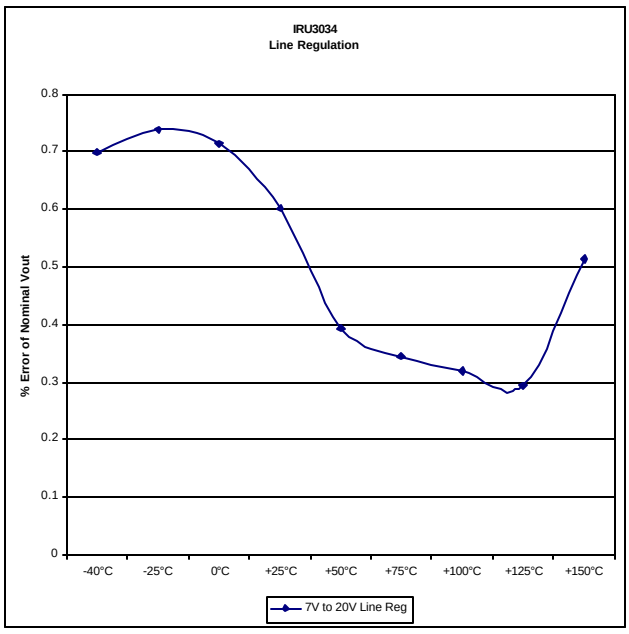


Figure 9 - Line Regulation.

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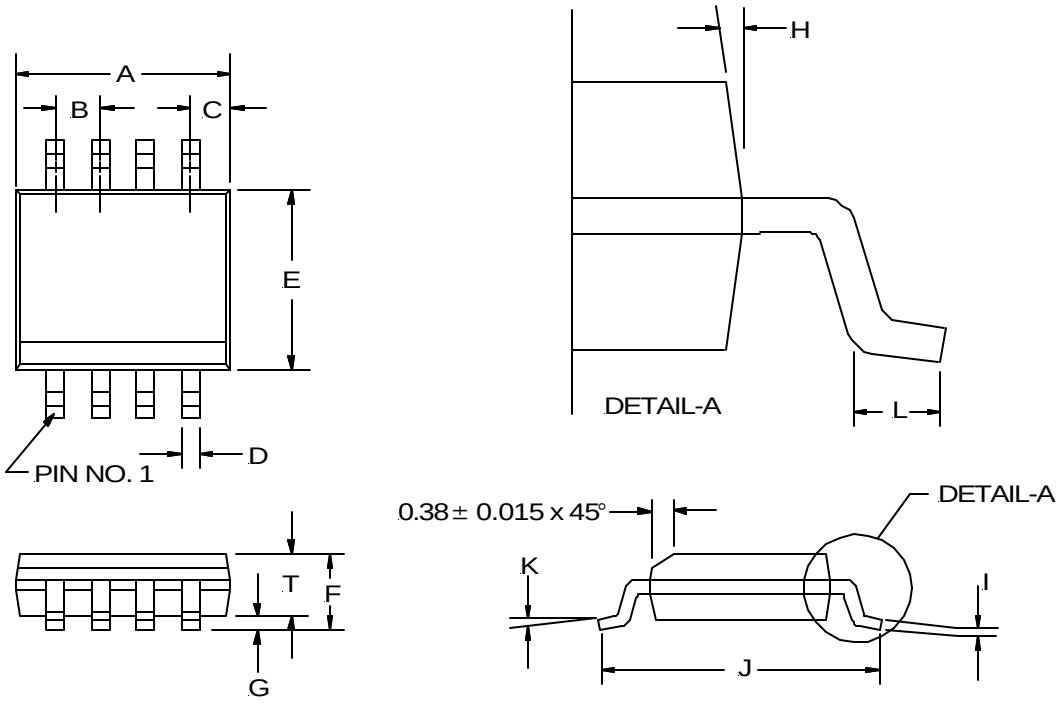
(S) SOIC Package
8-Pin Surface Mount, Narrow Body

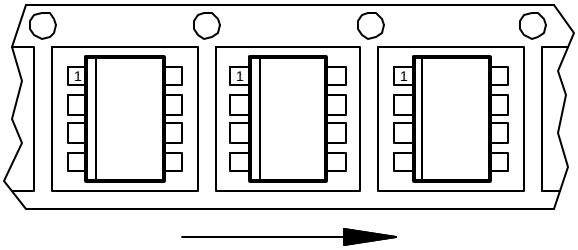


8-PIN		
SYMBOL	**MIN**	**MAX**
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
S	SOIC, Narrow Body	8	95	2500	Fig A



Feed Direction
Figure A

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IRU3037 / IRU3037A

8-PIN SYNCHRONOUS PWM CONTROLLER

FEATURES

- Synchronous Controller in 8-Pin Package
- Operating with single 5V or 12V supply voltage
- Internal 200KHz Oscillator (400KHz for IRU3037A)
- Soft-Start Function
- Fixed Frequency Voltage Mode
- 500mA Peak Output Drive Capability
- Protects the output when control FET is shorted

APPLICATIONS

- DDR memory source sink Vtt application
- Low cost on-board DC to DC such as 5V to 3.3V, 2.5V or 1.8V
- Graphic Card
- Hard Disk Drive

DESCRIPTION

The IRU3037 controller IC is designed to provide a low cost synchronous Buck regulator for on-board DC to DC converter applications. With the migration of today's ASIC products requiring low supply voltages such as 1.8V and lower, together with currents in excess of 3A, traditional linear regulators are simply too lossy to be used when input supply is 5V or even in some cases with 3.3V input supply. The IRU3037 together with dual N-channel MOSFETs such as IRF7313, provide a low cost solution for such applications. This device features an internal 200KHz oscillator (400KHz for "A" version), under-voltage lockout for both Vcc and Vc supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

TYPICAL APPLICATION

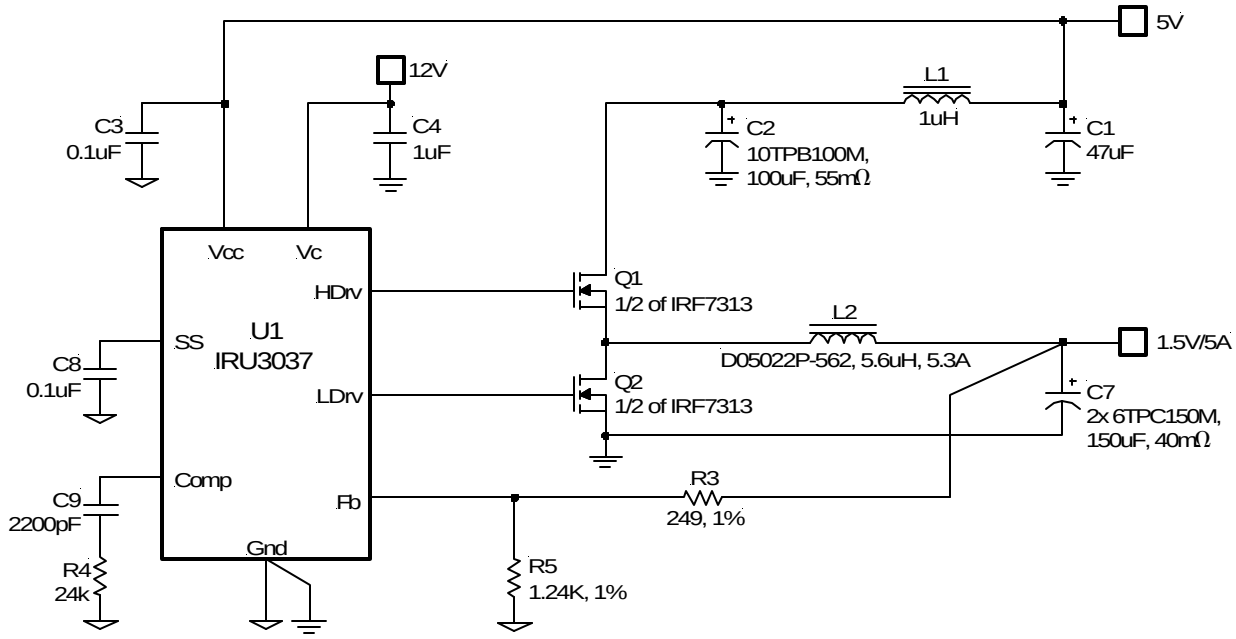


Figure 1 - Typical application of IRU3037 or IRU3037A.

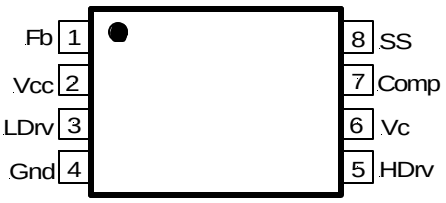
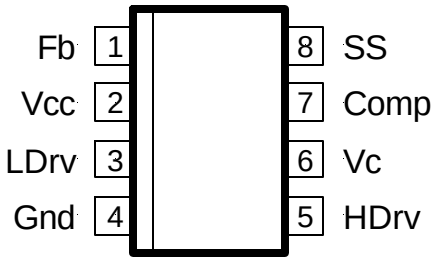
PACKAGE ORDER INFORMATION

T_A (°C)	DEVICE	PACKAGE	FREQUENCY
0 To 70	IRU3037CF	8-Pin Plastic TSSOP (F)	200KHz
0 To 70	IRU3037CS	8-Pin Plastic SOIC NB (S)	200KHz
0 To 70	IRU3037ACF	8-Pin Plastic TSSOP (F)	400KHz
0 To 70	IRU3037ACS	8-Pin Plastic SOIC NB (S)	400KHz

ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage 25V
Vc Supply Voltage ..... 30V (not rated for inductive load)
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

8-PIN PLASTIC TSSOP (F)	8-PIN PLASTIC SOIC (S)
	
θ_{JA}=124°C/W	θ_{JA}=160°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=5V, Vc=12V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage						
Fb Voltage	V_{FB}	IRU3037	1.225	1.250	1.275	
		IRU3037A	0.784	0.800	0.816	V
Fb Voltage Line Regulation	L_{REG}	5<Vcc<12		0.2	0.35	%
UVLO						
UVLO Threshold - Vcc	UVLO Vcc	Supply Ramping Up	4.0	4.2	4.4	V
UVLO Hysteresis - Vcc				0.25		V
UVLO Threshold - Vc	UVLO Vc	Supply Ramping Up	3.1	3.3	3.5	V
UVLO Hysteresis - Vc				0.2		V
UVLO Threshold - Fb	UVLO Fb	Fb Ramping Down (IRU3037)	0.4	0.6	0.8	V
		(IRU3037A)	0.3	0.4	0.5	
UVLO Hysteresis - Fb				0.1		V
Supply Current						
Vcc Dynamic Supply Current	Dyn Icc	Freq=200KHz, C_L=1500pF	2	5	8	mA
Vc Dynamic Supply Current	Dyn Ic	Freq=200KHz, C_L=1500pF	2	7	10	mA
Vcc Static Supply Current	I_{CCQ}	SS=0V	1	3.3	6	mA
Vc Static Supply Current	I_{CQ}	SS=0V	0.5	1	4.5	mA
Soft-Start Section						
Charge Current	SS_{IB}	SS=0V	-10	-20	-30	µA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Amp						
Fb Voltage Input Bias Current	I_{FB1}	SS=3V, Fb=1V		-0.1		µA
Fb Voltage Input Bias Current	I_{FB2}	SS=0V, Fb=1V		-64		µA
Transconductance	gm		450	600	750	µmho
Oscillator						
Frequency	Freq	IRU3037	180	200	220	KHz
		IRU3037A	360	400	440	
Ramp-Amplitude Voltage	V_{RAMP}		1.225	1.25	1.275	V
Output Drivers						
Rise Time	T_r	C_L=1500pF		50	100	ns
Fall Time	T_f	C_L=1500pF		50	100	ns
Dead Band Time	T_{DB}		50	150	250	ns
Max Duty Cycle	T_{ON}	Fb=1V, Freq=200KHz	85	90	95	%
Min Duty Cycle	T_{OFF}	Fb=1.5V	0	0		%

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Fb	This pin is connected directly to the output of the switching regulator via resistor divider to provide feedback to the Error amplifier.
2	Vcc	This pin provides biasing for the internal blocks of the IC as well as power for the low side driver. A minimum of 1µF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
3	LDrv	Output driver for the synchronous power MOSFET.
4	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane. A high frequency capacitor (0.1 to 1µF) must be connected from V5 and V12 pins to this pin for noise free operation.
5	HDrv	Output driver for the high side power MOSFET. Connect a diode, such as BAT54 or 1N4148, from this pin to ground for the application when the inductor current goes negative (Source/ Sink), soft-start at no load and for the fast load transient from full load to no load.
6	Vc	This pin is connected to a voltage that must be at least 4V higher than the bus voltage of the switcher (assuming 5V threshold MOSFET) and powers the high side output driver. A minimum of 1µF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
7	Comp	Compensation pin of the error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
8	SS	This pin provides soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the output of the switching regulator, preventing it from overshooting as well as limiting the input current. The converter can be shutdown by pulling this pin below 0.5V.

BLOCK DIAGRAM

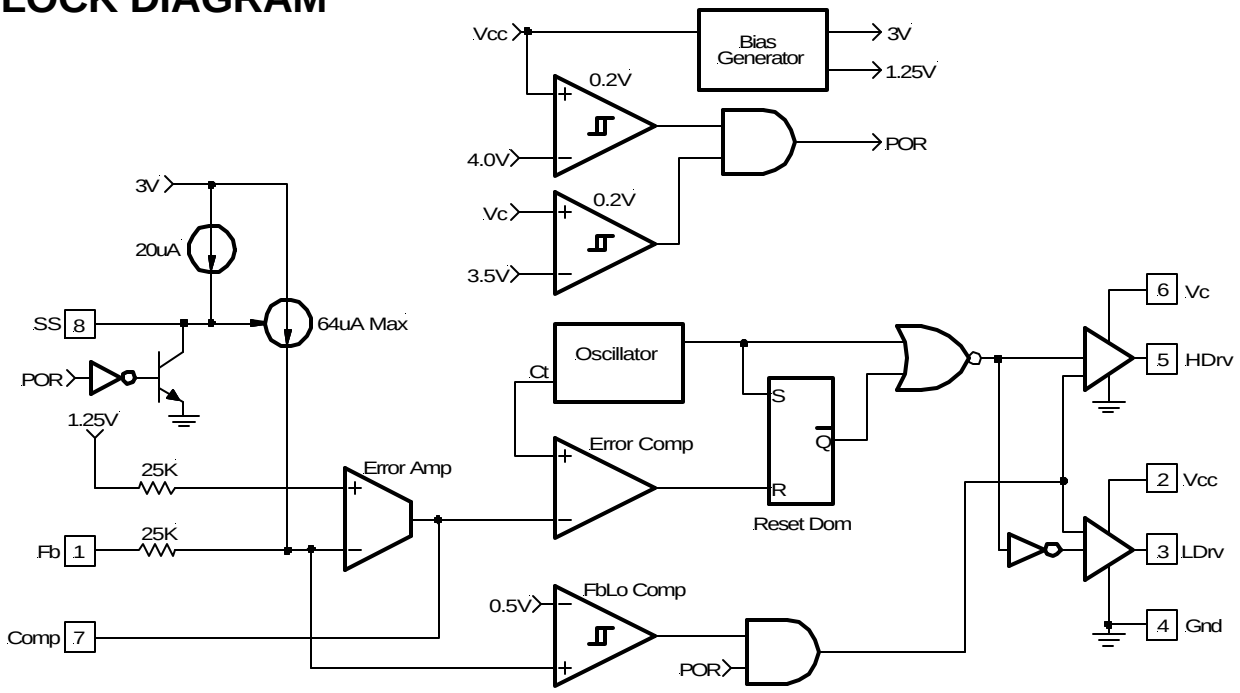


Figure 2 - Simplified block diagram of the IRU3037.

THEORY OF OPERATION

Introduction

The IRU3037 is a fixed frequency, voltage mode synchronous controller and consists of a precision reference voltage, an error amplifier, an internal oscillator, a PWM comparator, 0.5A peak gate driver, soft-start and shutdown circuits (see Block Diagram).

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier; this is the amplified error signal from the sensed output voltage and the reference voltage.

This voltage is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulses of variable duty-cycle, which drives the two N-channel external MOSFETs.The timing of the IC is provided through an internal oscillator circuit which uses on-chip capacitor to set the oscillation frequency to 200 KHz (400 KHz for “A” version).

Soft-Start

The IRU3037 has a programmable soft-start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vc and Vcc rise above their threshold (3.3V and 4.2V respectively) and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A’s output of the PWM converter. As the charging voltage of the external capacitor ramps up, the PWM signals increase from zero to the point the feedback loop takes control.

Short-Circuit Protection

The outputs are protected against the short-circuit. The IRU3037 protects the circuit for shorted output by sensing the output voltage (through the external resistor divider). The IRU3037 shuts down the PWM signals, when the output voltage drops below 0.6V (0.4V for IRU3037A).

The IRU3037 also protects the output from over-voltaging when the control FET is shorted. This is done by turning on the sync FET with the maximum duty cycle.

Under-Voltage Lockout

The under-voltage lockout circuit assures that the MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if Vc and Vcc fall below 3.3V and 4.2V respectively. Normal operation resumes once Vc and Vcc rise above the set values.

APPLICATION INFORMATION

Design Example:
The following example is a typical application for IRU3037, the schematic is Figure 18 on page 14.

V_{IN} = 5V
V_{OUT} = 3.3V
I_{OUT} = 4A
ΔV_{OUT} = 100mV
f_S = 200KHz

Output Voltage Programming
Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 1.25V (0.8V for IRU3037A). The divider is ratioed to provide 1.25V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_6}{R_5}\right) \qquad ---(1)$$

When an external resistor divider is connected to the output as shown in Figure 3.

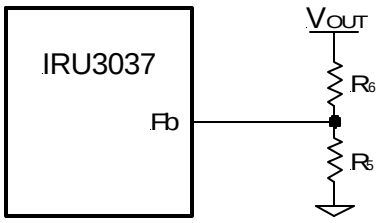


Figure 3 - Typical application of the IRU3037 for programming the output voltage.

Equation (1) can be rewritten as:

$$R_6 = R_5 \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

Choose R_5 = 1KΩ
This will result to R_6 = 1.65KΩ

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-Start Programming
The soft-start timing can be programmed by selecting the soft start capacitance value. The start up time of the converter can be calculated by using:

$$t_{START} = 75 \times Css \quad (ms) \qquad ---(2)$$

Where:
C_{SS} is the soft-start capacitor (μF)

For a start-up time of 7.5ms, the soft-start capacitor will be 0.1μF. Choose a ceramic capacitor at 0.1μF.

Shutdown
The converter can be shutdown by pulling the soft-start pin below 0.5V. The control MOSFET turns off and the synchronous MOSFET turns on during shutdown.

Boost Supply Vc
To drive the high-side switch it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 18. The capacitor is charged up to approximately twice the bus voltage. A capacitor in the range of 0.1μF to 1μF is generally adequate for most applications. In application, when a separate voltage source is available the boost circuit can be avoided as shown in Figure 1.

Input Capacitor Selection
The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The larger capacitor, the less ripple expected but consider should be taken for the higher surge current during the power-up. The IRU3037 provides the soft-start function which controls and limits the current surge. The value of the input capacitor can be calculated by the following formula:

$$C_{IN} = \frac{I_{IN} \times \Delta t}{\Delta V} \qquad ---(3)$$

Where:
C_{IN} is the input capacitance (μF)
I_{IN} is the input current (A)
Δt is the turn on time of the high-side switch (μs)
ΔV is the allowable peak to peak voltage ripple (V)

Assuming the following:

ΔV = 1%(V_{IN}), Efficiency(η) = 90%

$$\Delta t = D \times \frac{1}{f_S} \quad \textbf{Y} \quad \Delta t = 3.3\mu s$$

$$I_{IN} = \frac{V_O \times I_O}{\eta \times V_{IN}} \quad \textbf{Y} \quad I_{IN} = 2.93A$$

By using equation (3), C_{IN} = 193.3μF
For higher efficiency, low ESR capacitor is recommended. Choose two 100μF capacitors.

The Sanyo TPB series PosCap capacitor 100μF, 10V with 55mΩ ESR is a good choice.

Output Capacitor Selection

The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$ESR \leq \frac{\Delta V_O}{\Delta I_O} \qquad ---(4)$$

Where:
ΔV_O = Output Voltage Ripple
ΔI_O = Output Current
ΔV_O=100mV and ΔI_O=4A
Results to ESR=25mΩ

The Sanyo TPC series, PosCap capacitor is a good choice. The 6TPC150M 150μF, 6.3V has an ESR 40mΩ. Selecting two of these capacitors in parallel, results to an ESR of $\cong$ 20mΩ which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi). The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \; ; \; \Delta t = D \times \frac{1}{f_S} \; ; \; D = \frac{V_{IN}}{V_{OUT}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \qquad ---(5)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OUT} = Output Voltage
Δi = Inductor Ripple Current
f_S = Switching Frequency
Δt = Turn On Time
D = Duty Cycle

If Δi = 20%(I_O), then the output inductor will be:

L = 7μH

The Toko D124C series provides a range of inductors in different values, low profile suitable for large currents, 10μH, 4.2A is a good choice for this application. This will result to a ripple approximately 14% of output current.

Power MOSFET Selection

The IRU3037 uses two N-Channel MOSFETs. The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{IN}).

The gate drive requirement is almost the same for both MOSFETs. Logic-level transistor can be used and caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{COND} \text{ (Upper Switch)} = I^2_{LOAD} \times R_{DS(ON)} \times D \times \vartheta$$

$$P_{COND} \text{ (Lower Switch)} = I^2_{LOAD} \times R_{DS(ON)} \times (1 - D) \times \vartheta$$

ϑ = $R_{DS(ON)}$ Temperature Dependency

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

For this design, IRF7301 is a good choice. The device provides low on-resistance in a compact SOIC 8-Pin package.

The IRF7301 has the following data:

V_{DSS} = 20V
I_D = 5.2A
$R_{DS(ON)}$ = 0.05Ω

The total conduction losses will be:

$P_{CON(TOTAL)}=P_{CON}$(Upper Switch)+P_{CON}(Lower Switch)

$P_{CON(TOTAL)} = I^2_{LOAD} \times R_{DS(ON)} \times \vartheta$

ϑ = 1.5 according to the IRF7301 data sheet for 150°C junction temperature

$P_{CON(TOTAL)}$ = 1.2W

The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turnoff delays and rise and fall times. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \qquad ---(6)$$

Where:
$V_{DS(OFF)}$ = Drain to Source Voltage at off time
t_r = Rise Time
t_f = Fall Time
T = Switching Period
I_{LOAD} = Load Current

The switching time waveform is shown in figure 4.

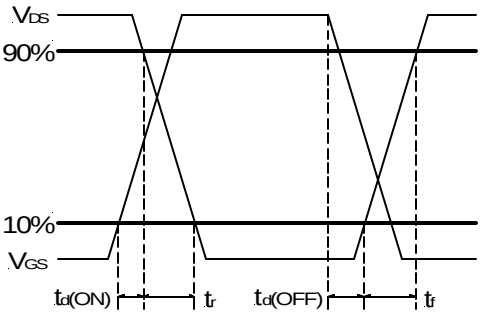


Figure 4 - Switching time waveforms.

From IRF7301 data sheet we obtain:

t_r = 42ns
t_f = 51ns

These values are taken under a certain condition test. For more detail please refer to the IRF7301 data sheet.

By using equation (6), we can calculate the switching losses.

P_{SW} = 0.186W

Feedback Compensation

The IRU3037 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 5). The Resonant frequency of the LC filter expressed as follows:

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad ---(7)$$

Figure 5 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

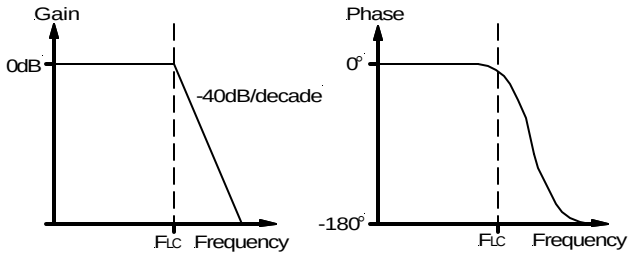


Figure 5 - Gain and phase of LC filter.

The IRU3037's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in Figure 6.

Note that this method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general the output capacitor's ESR generates a zero typically at 5KHz to 50KHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \qquad ---(8)$$

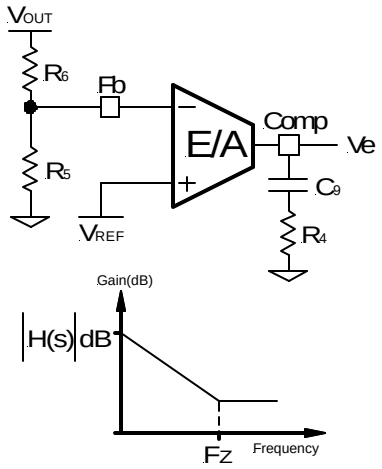


Figure 6 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / V_{OUT}) is given by:

$$H(s) = \left(g_m \times \frac{R_5}{R_6 + R_5}\right) \times \frac{1 + sR_4C_9}{sC_9} \qquad ---(9)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = g_m \times \frac{R_5}{R_6 \times R_5} \times R_4 \qquad ---(10)$$

$$F_Z = \frac{1}{2\pi \times R_4 \times C_9} \qquad ---(11)$$

The gain is determined by the voltage divider and E/A's transconductance gain.

First select the desired zero-crossover frequency (Fo):

$Fo > F_{ESR}$ and $F_O \leq (1/5 \sim 1/10) \times f_S$

Use the following equation to calculate R_4:

$$R_4 = \frac{V_{OSC}}{V_{IN}} \times \frac{Fo \times F_{ESR}}{F_{LC}^2} \times \frac{R_5 + R_6}{R_5} \times \frac{1}{g_m} \qquad ---(12)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Fo = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_5 and R_6 = Resistor Dividers for Output Voltage Programming
g_m = Error Amplifier Transconductance

For:
V_{IN} = 5V
V_{OSC} = 1.25V
Fo = 30KHz
F_{ESR} = 26.52KHz
F_{LC} = 2.9KHz
R_5 = 1K
R_6 = 1.65K
g_m = 600µmho

This results to R_4=104.4KΩ. Choose R_4=105KΩ

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$F_Z \cong 75\% F_{LC}$

$$F_Z \cong 0.75 \times \frac{1}{2\pi\sqrt{L_O \times C_O}} \qquad ---(13)$$

For:
Lo = 10µH
Co = 300µF
F_Z = 2.17KHz
R_4 = 86.6KΩ

Using equations (11) and (13) to calculate C_9, we get:

C_9 = 698pF
Choose C_9 = 680pF

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to supress the switching noise. The additional pole is given by:

$$F_P = \frac{1}{2\pi \times R_4 \times \frac{C_9 \times C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi \times R_4 \times f_S - \frac{1}{C_9}} \cong \frac{1}{\pi \times R_4 \times f_S}$$

for $F_P << \frac{f_S}{2}$

For a general solution for unconditionally stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 7.

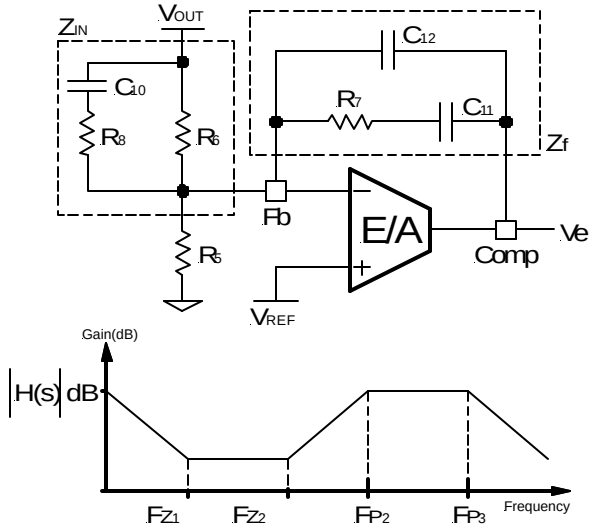


Figure 7 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m Z_f >> 1 \quad \text{and} \quad g_m Z_{IN} >> 1 \qquad \text{---(14)}$$

By replacing Z_{IN} and Z_f according to Figure 7, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11}) \times [1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+sR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_O = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \qquad \text{---(15)}$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Lo = Output Inductor
Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition (14) regarding transconductance error amplifier.

1) Select the crossover frequency:
$F_O < F_{ESR}$ and $F_O \leq (1/10 \sim 1/6) \times f_S$

2) Select R_7, so that $R_7 >> \frac{2}{g_m}$

3) Place first zero before LC's resonant frequency pole.
$F_{Z1} \cong 75\% F_{LC}$

$$C_{11} = \frac{1}{2\pi \times F_{Z1} \times R_7}$$

4) Place third pole at the half of the switching frequency.

$$F_{P3} = \frac{f_S}{2}$$

$$C_{12} = \frac{1}{2\pi \times R_7 \times F_{P3}}$$

$C_{12} > 50pF$
If not, change R_7 selection.

5) Place R_7 in (15) and calculate C_{10}:

$$C_{10} \leq \frac{2\pi \times Lo \times Fo \times Co}{R_7} \times \frac{V_{OSC}}{V_{IN}}$$

6) Place second pole at the ESR zero.
$F_{P2} = F_{ESR}$

$$R_8 = \frac{1}{2\pi \times C_{10} \times F_{P2}}$$

Check if $R_8 > \frac{1}{gm}$

If R_8 is too small, increase R_7 and start from step 2.

7) Place second zero around the resonant frequency.
$F_{Z2} = F_{LC}$

$$R_6 = \frac{1}{2\pi \times C_{10} \times F_{Z2}} - R_8$$

8) Use equation (1) to calculate R_5.

$$R_5 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_6$$

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

IC Quiescent Power Dissipation
Power dissipation for IC controller is a function of applied voltage, gate driver loads and switching frequency. The IC's maximum power dissipation occurs when the IC operating with single 12V supply voltage (Vcc=12V and Vc≅24V) at 400KHz switching frequency and maximum gate loads.

Figures 9 and 10 show voltage vs. current, when the gate drivers loaded with 470pF, 1150pF and 1540pF capacitors. The IC's power dissipation results to an excessive temperature rise. This should be considered when using IRU3037A for such application.

Layout Consideration
The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

Figure 8 shows a suggested layout for the critical components, based on the schematic on page 14.

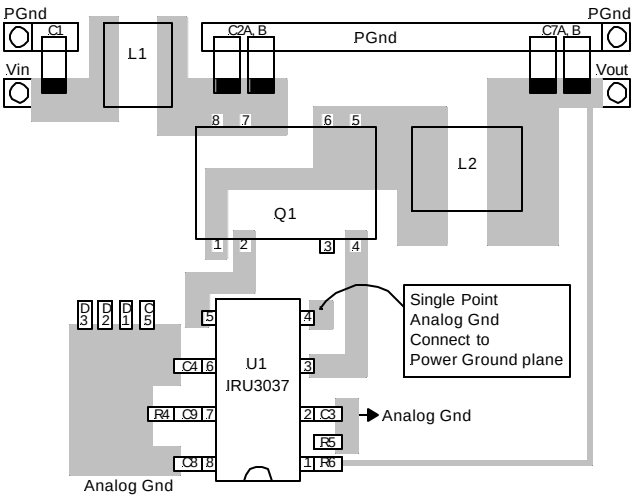


Figure 8 - Suggested layout.
(Topside shown only)

TYPICAL PERFORMANCE CHARACTERISTICS

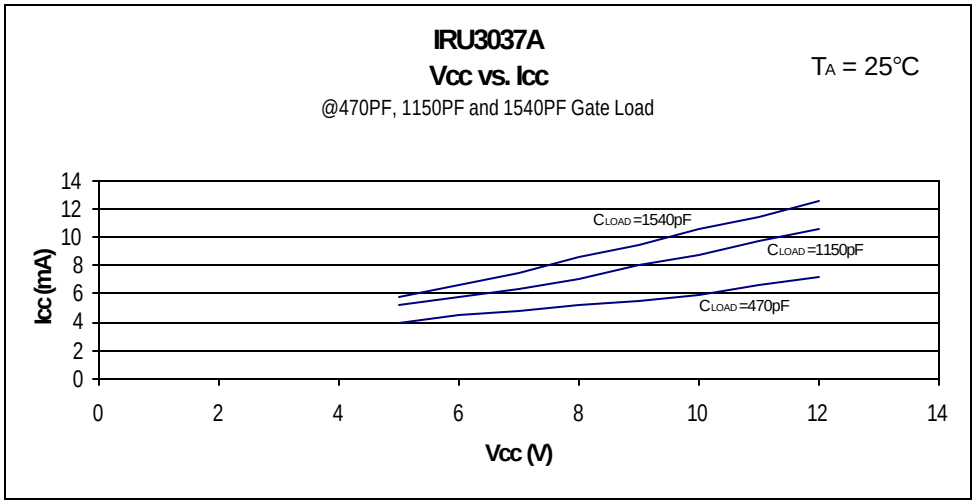


Figure 9 - Vcc vs. Icc

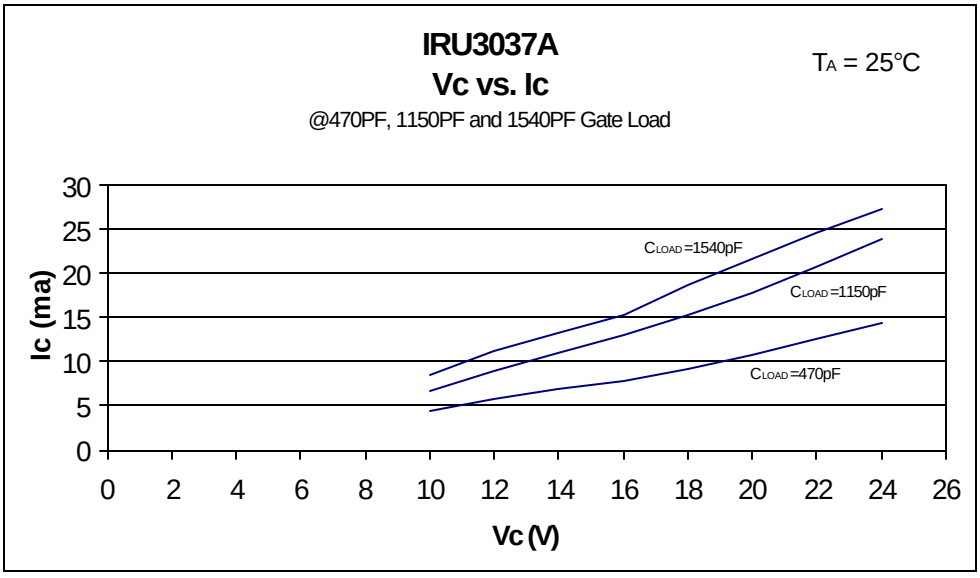


Figure 10 - Vc vs. Ic

TYPICAL PERFORMANCE CHARACTERISTICS

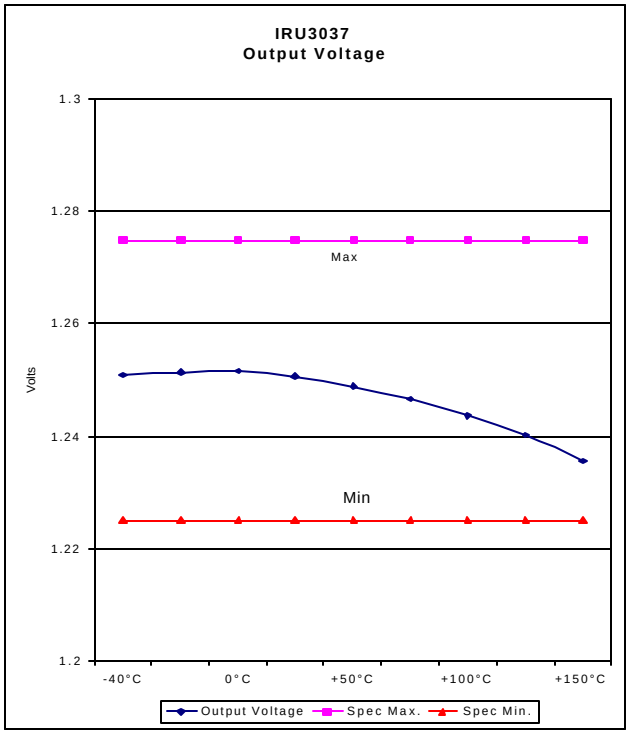


Figure 11 - Output Voltage

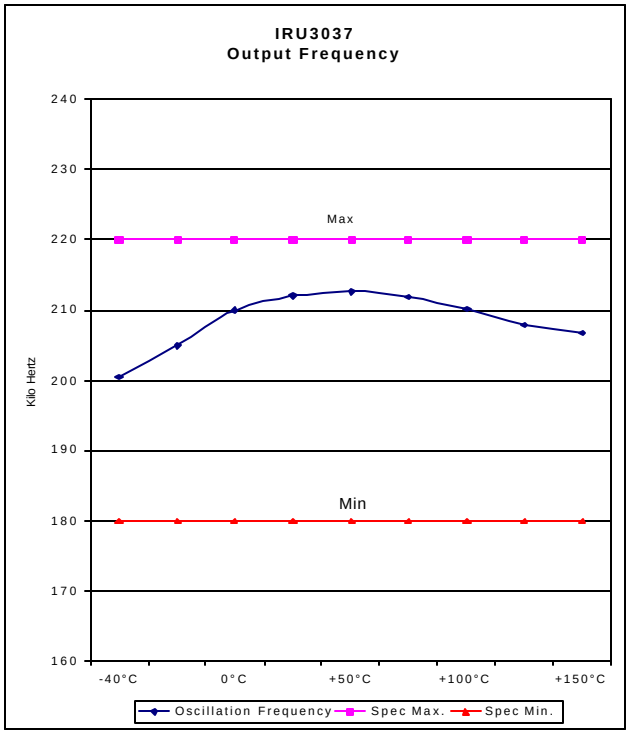


Figure 12 - Output Frequency

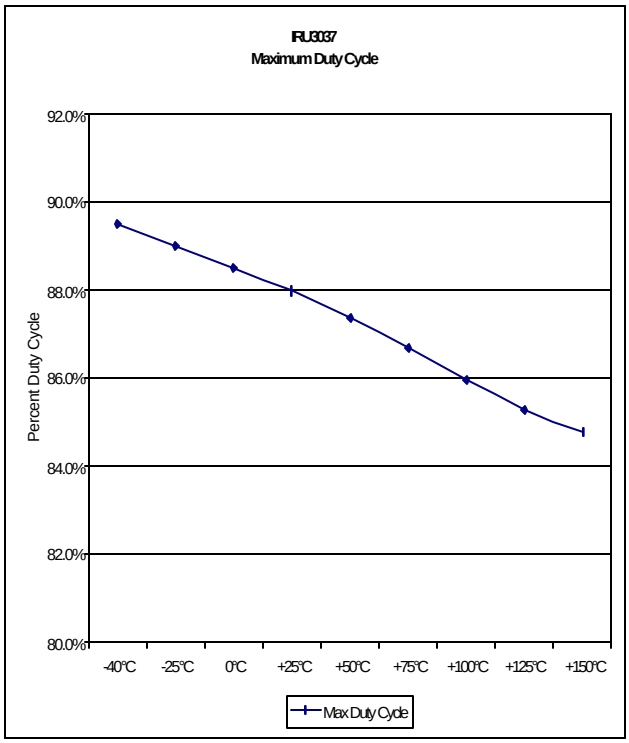


Figure 13 - Maximum Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS

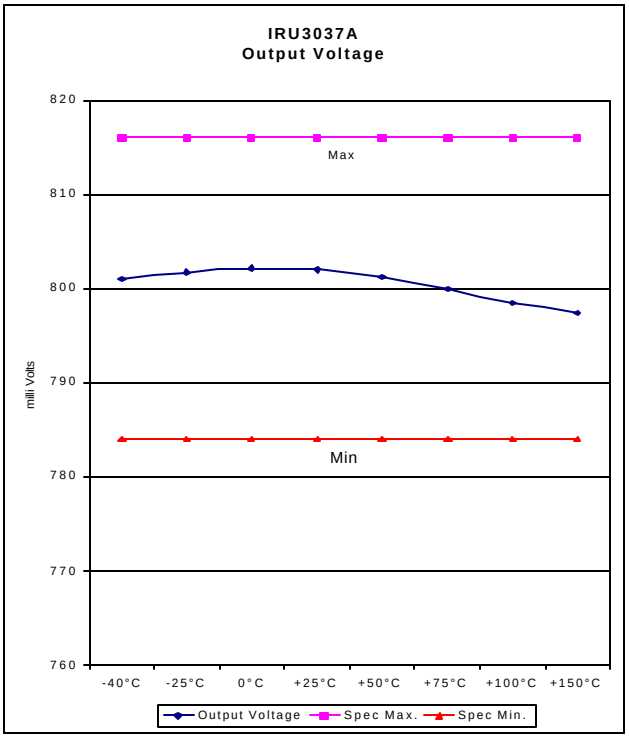


Figure 14 - Output Voltage

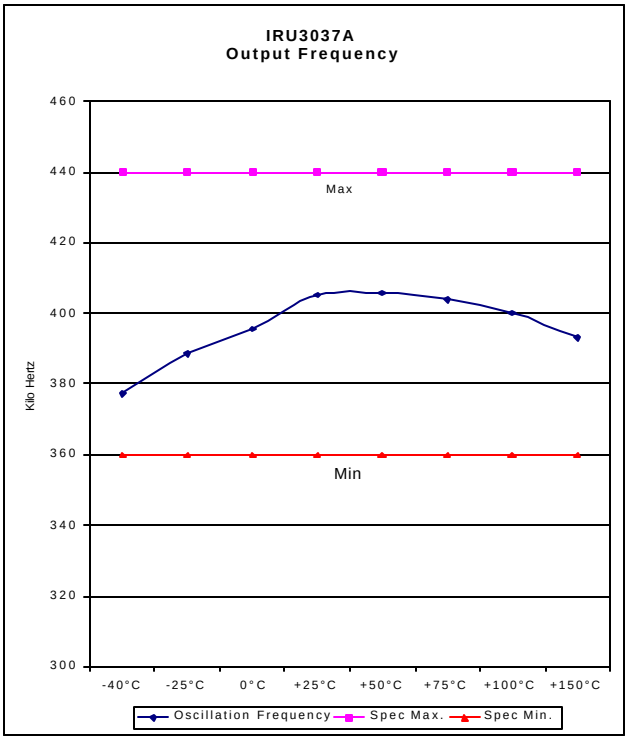


Figure 15 - Output Frequency

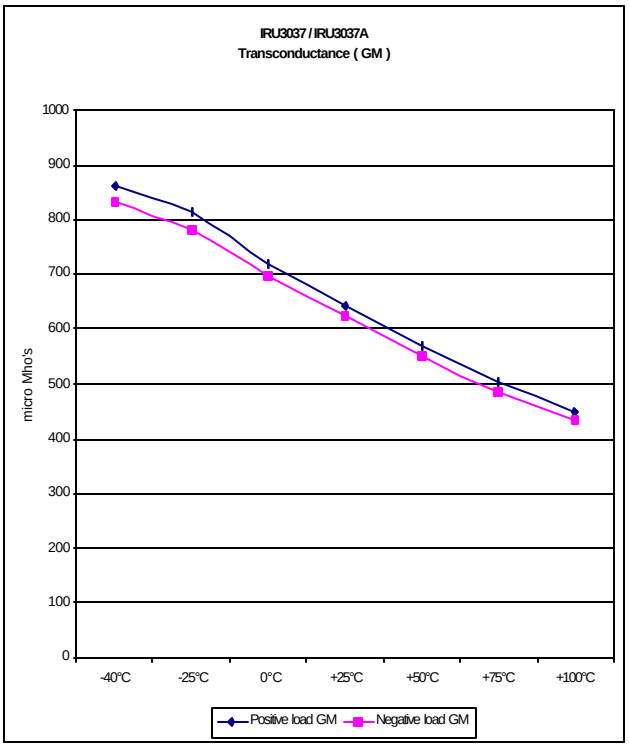


Figure 16 - Transconductance

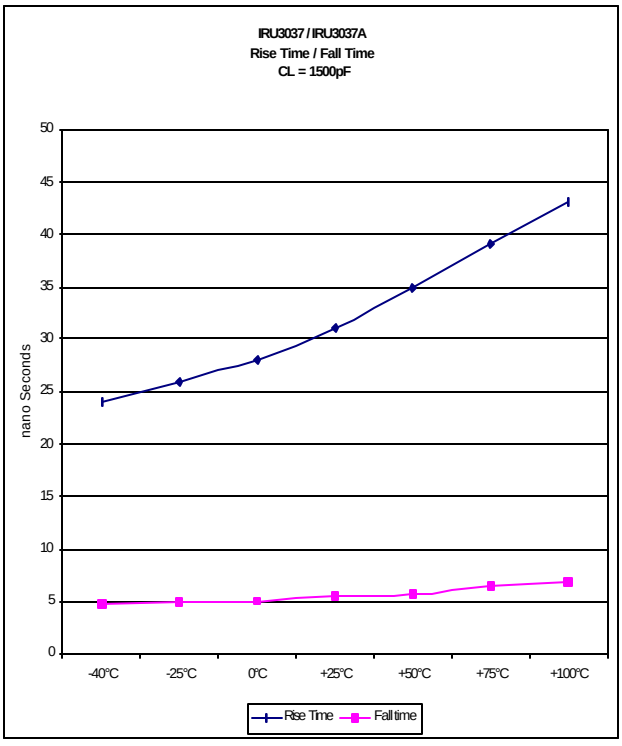


Figure 17 - Rise Time and Fall Time

TYPICAL APPLICATION

Single Supply 5V Input

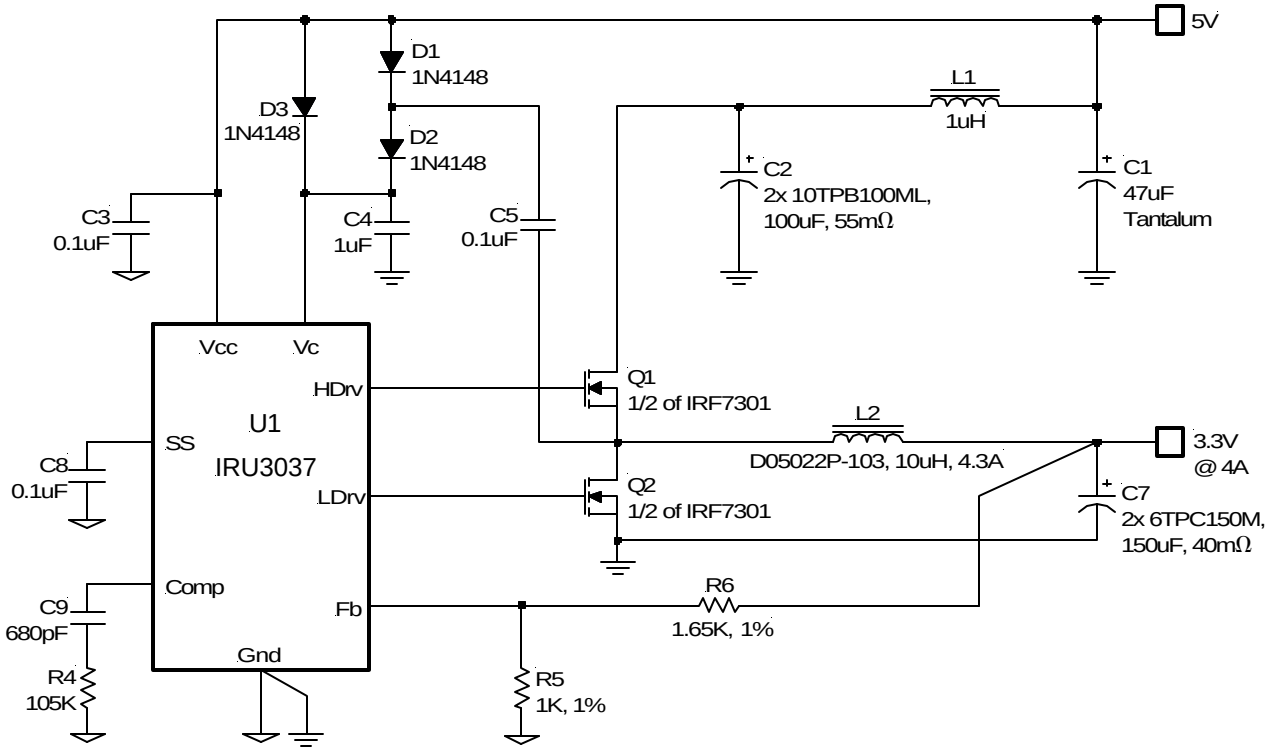


Figure 18 - Typical application of IRU3037 in an on-board DC-DC converter using a single 5V supply.

TYPICAL APPLICATION

Dual Supply, 5V Bus and 12V Bias Input

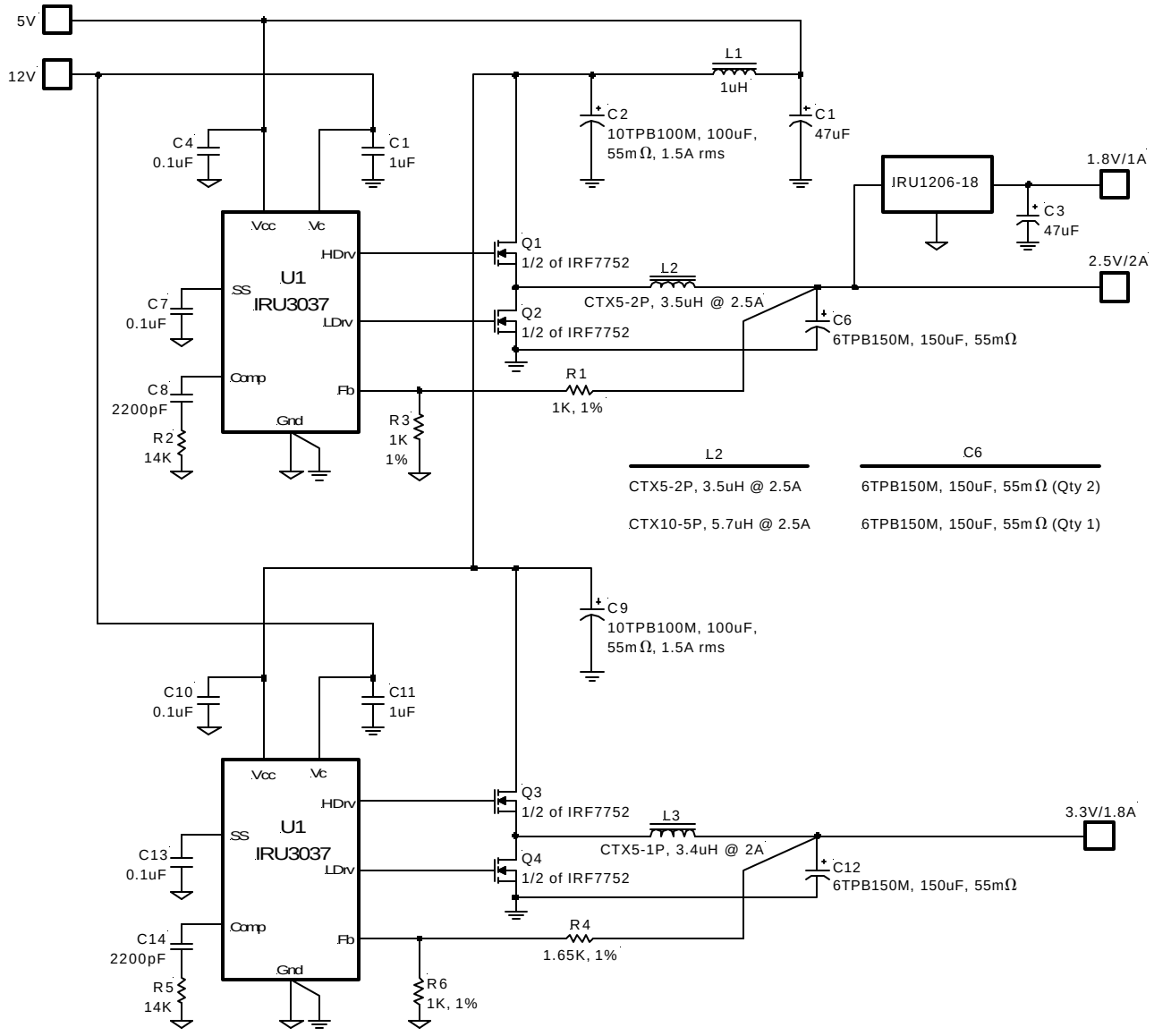


Figure 19 - Typical application of IRU3037 or IRU3037A in an on-board DC-DC converter providing the Core, GTL+, and Clock supplies for the Pentium II microprocessor.

TYPICAL APPLICATION

1.8V to 7.5V / 0.5A Boost Converter

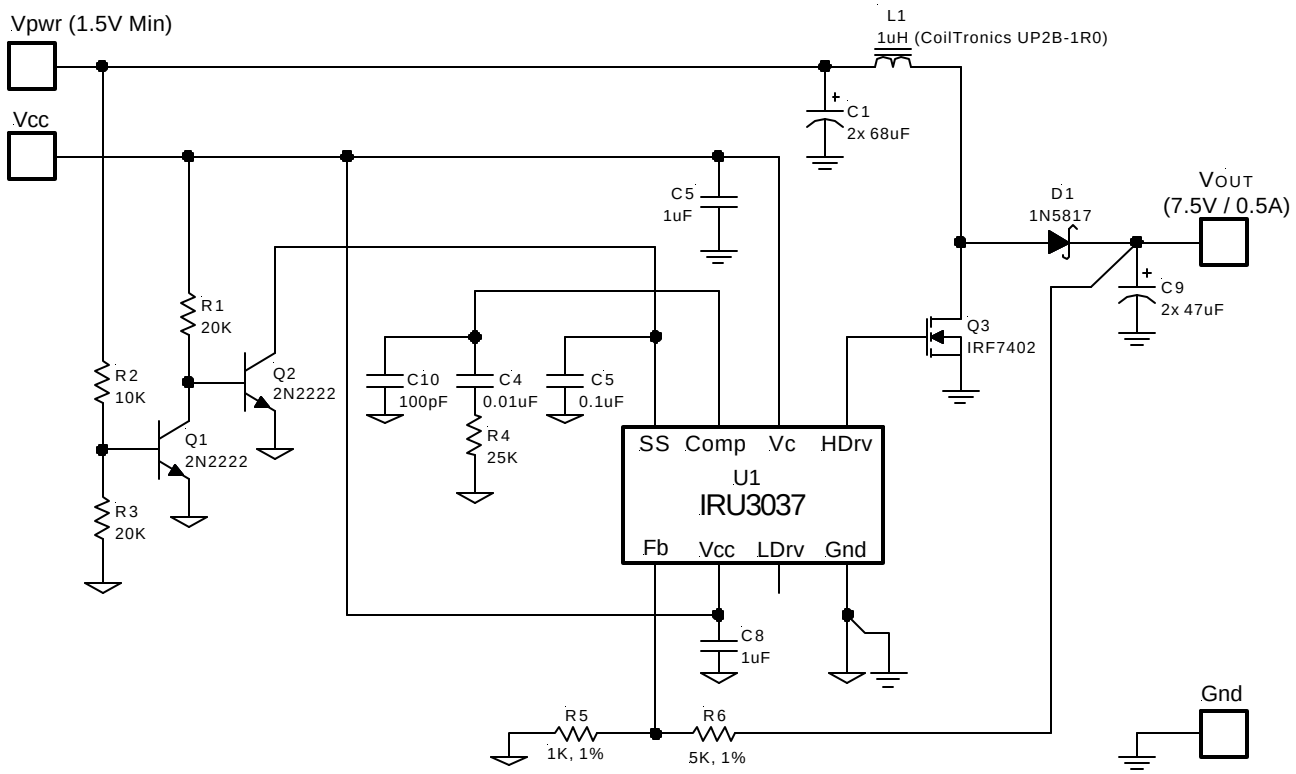


Figure 20 - Typical application of IRU3037 as a boost converter.

DEMO-BOARD APPLICATION

5V or 12V to 3.3V @ 10A

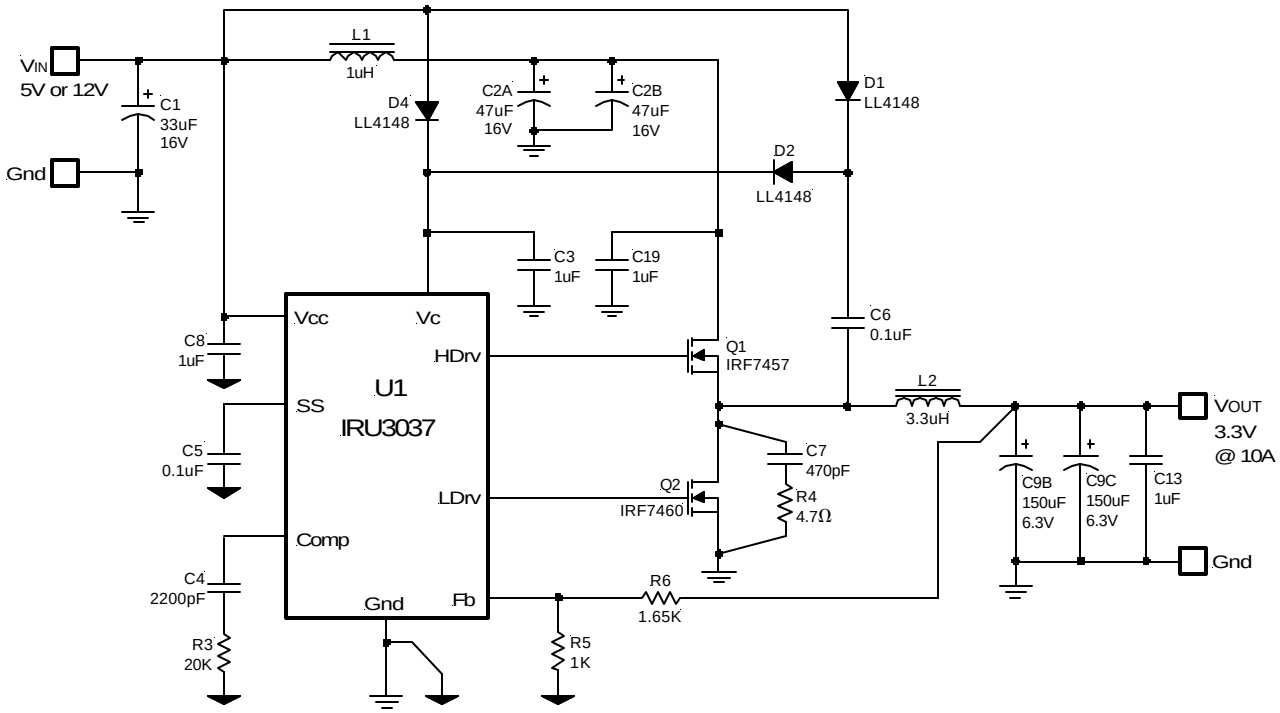


Figure 21 - Demo-board application of IRU3037.

Application Parts List

Ref Desig	Description	Value	Qty	Part#	Manuf
Q1	MOSFET	20V, 7mΩ, 15A	1	IRF7457	IR
Q2	MOSFET	20V, 10mΩ, 12A	1	IRF7460	IR
U1	Controller	Synchronous PWM	1	IRU3037	IR
D1, D2, D4	Diode	Fast Switching	3	LL4148	
L1	Inductor	1µH, 10A	1	D03316P-102HC	Coilcraft
L2	Inductor	3.3µH, 12A	1	D05022P-332HC	Coilcraft
C1	Capacitor, Tantalum	33µF, 16V	1	ECS-T1CD336R	Panasonic
C2A, C2B	Capacitor, Poscap	47µF, 16V, 70mΩ	2	16TPB47M	Sanyo
C9B, C9C	Capacitor, Poscap	150µF, 6.3V, 40mΩ	2	6TPC150M	Sanyo
C5, C6	Capacitor, Ceramic	0.1µF, Y5V, 25V	2	ECJ-2VF1E104Z	Panasonic
C3	Capacitor, Ceramic	1µF, X7R, 25V	1	ECJ-3YB1E105K	Panasonic
C4	Capacitor, Ceramic	2200pF, X7R, 50V	1	ECJ-2VB1H222K	Panasonic
C7	Capacitor, Ceramic	470pF, X7R	1	ECJ-2VB2D471K	Panasonic
C8, C13, C19	Capacitor, Ceramic	1µF, Y5V, 16V	3	ECJ-2VF1C105Z	Panasonic
R3	Resistor	20K, 5%	1		
R4	Resistor	4.7Ω, 5%	1		
R5	Resistor	1K, 1%	1		
R6	Resistor	1.65K, 1%	1		

DEMO-BOARD WAVEFORMS

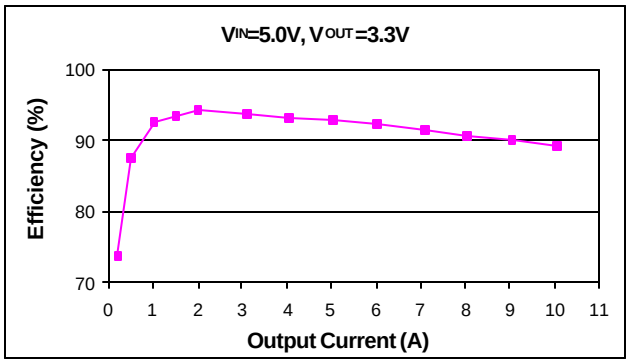


Figure 22 - Efficiency for IRU3037 Evaluation Board.

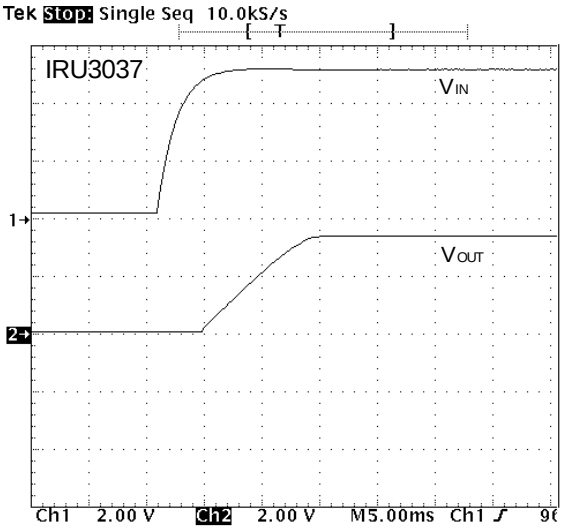


Figure 23 - Start-up time @ I_{OUT}=5A.

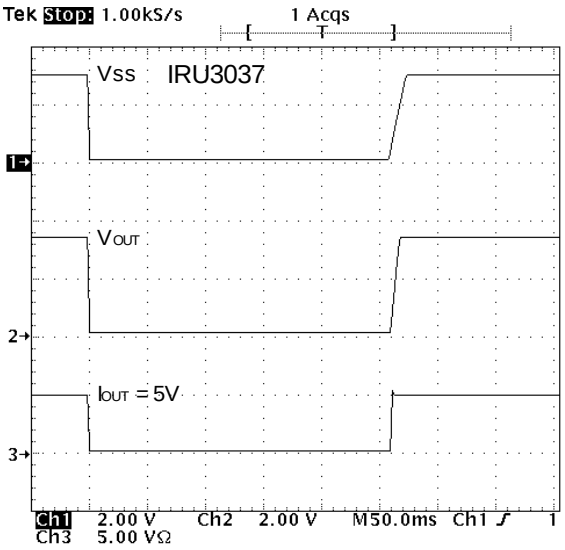


Figure 24 - Shutdown the output by pulling down the soft-start.

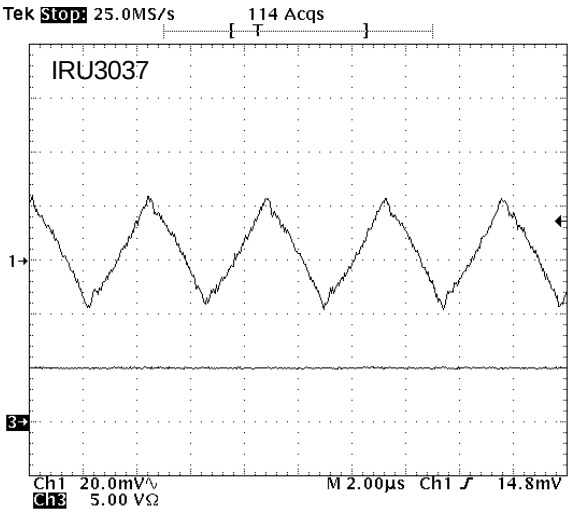


Figure 25 - 3.3V output voltage ripple @ I_{OUT}=5A.

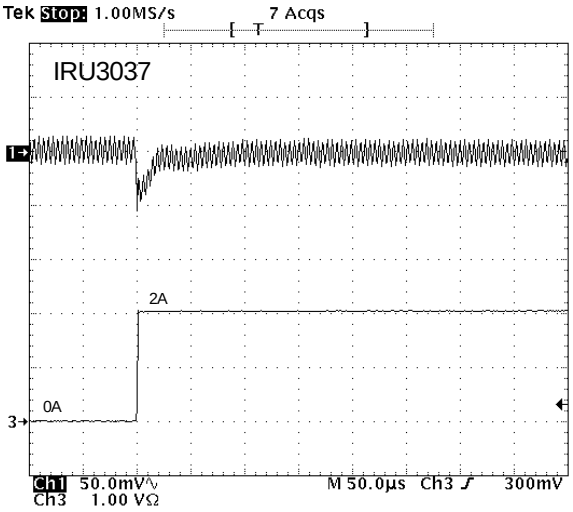


Figure 26 - Transient response @ I_{OUT} = 0 to 2A.

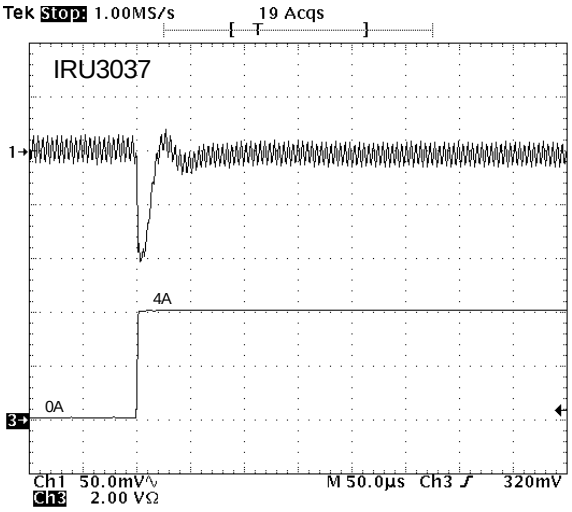
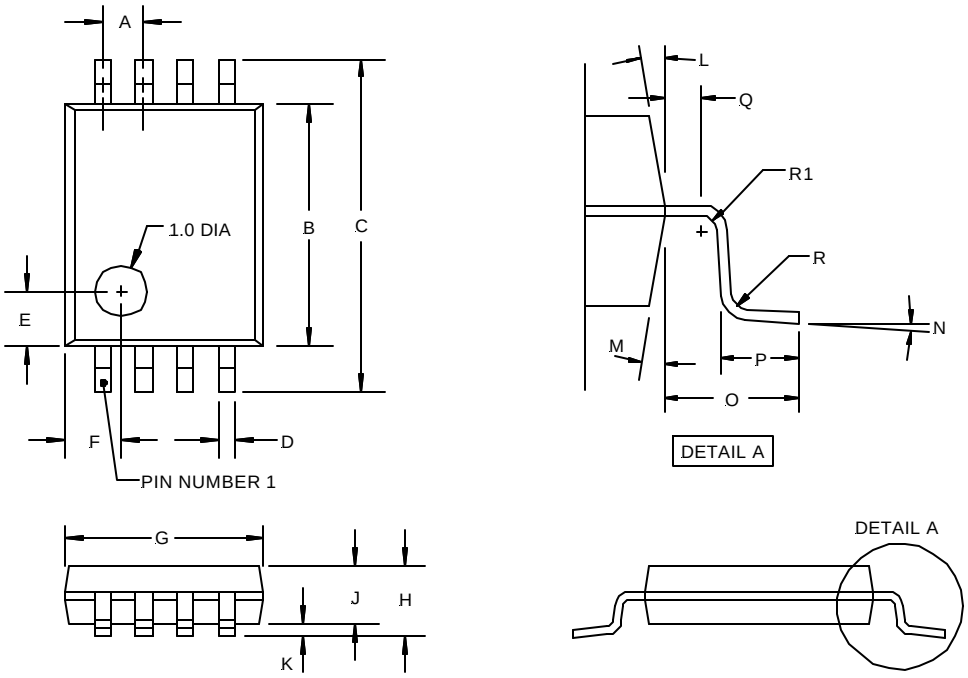


Figure 27 - Transient response @ I_{OUT} = 0 to 4A.

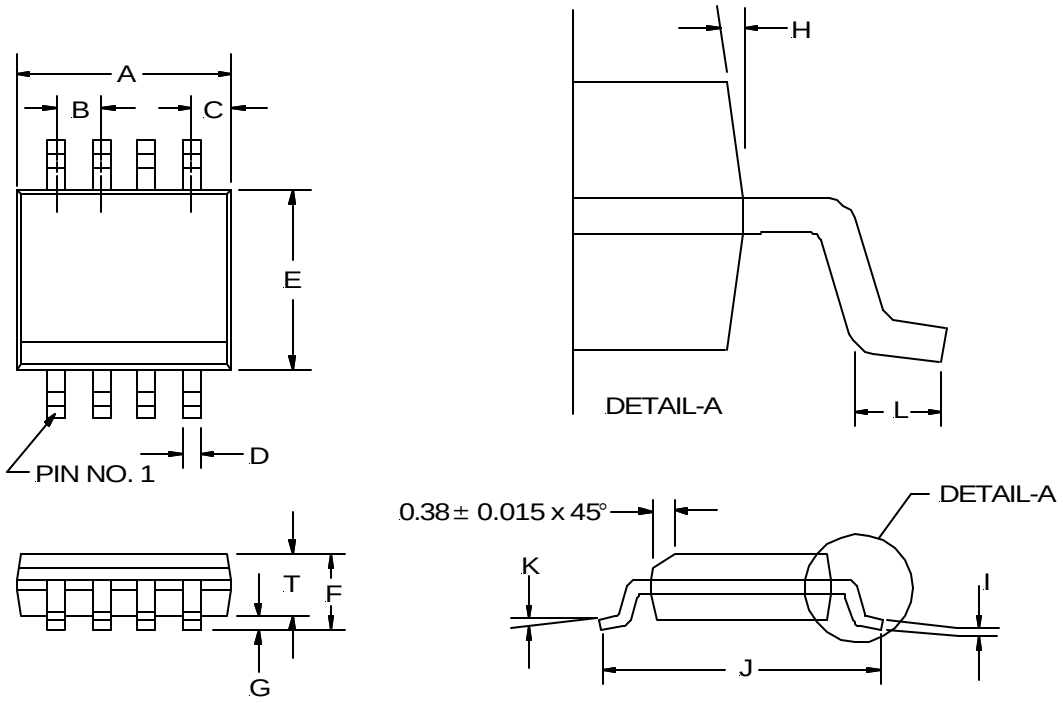
(F) TSSOP Package
8-Pin



SYMBOL DESIG	8-PIN		
	MIN	NOM	MAX
A		0.65 BSC	
B	4.30	4.40	4.50
C		6.40 BSC	
D	0.19	---	0.30
E		1.00	
F		1.00	
G	2.90	3.00	3.10
H	---	---	1.10
J	0.85	0.90	0.95
K	0.05	---	0.15
L		12° REF	
M		12° REF	
N	0°	---	8°
O		1.00 REF	
P	0.50	0.60	0.75
Q		0.20	
R	0.09	---	---
R1	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

(S) SOIC Package
8-Pin Surface Mount, Narrow Body

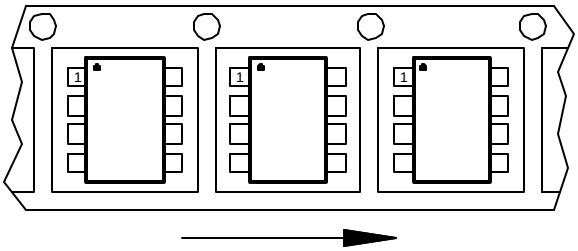


8-PIN		
SYMBOL	**MIN**	**MAX**
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

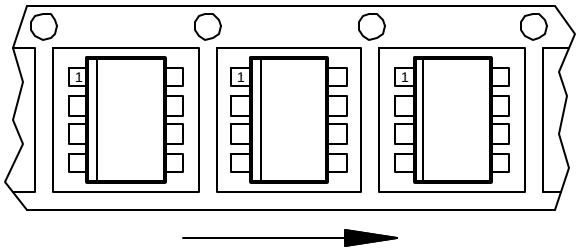
NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
F	TSSOP Plastic	8	100	2500	Fig A
S	SOIC, Narrow Body	8	95	2500	Fig B



Feed Direction
Figure A



Feed Direction
Figure B

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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IRU3038

SYNCHRONOUS PWM CONTROLLER FOR TERMINATION POWER SUPPLY APPLICATIONS

PRELIMINARY DATA SHEET

FEATURES

- Synchronous Controller in 14-Pin Package
- Operating with single 5V or 12V supply voltage
- 200KHz to 400KHz operation set by an external resistor
- Soft-Start Function
- Fixed Frequency Voltage Mode
- 500mA Peak Output Drive Capability
- Uncommitted Error Amplifier available for DDR voltage tracking application
- 1.25V Reference Voltage
- Protects the output when control FET is shorted

APPLICATIONS

- DDR memory source sink Vtt application
- Low cost on-board DC to DC such as 5V to 3.3V, 2.5V or 1.8V
- Graphic Card
- Hard Disk Drive

DESCRIPTION

The IRU3038 controller IC is designed to provide a low cost synchronous Buck regulator for voltage tracking applications such DDR memory and general purpose on-board DC to DC converter. Modern micro processors combined with DDR memory, need high-speed bandwidth data bus which requires a particular bus termination voltage. This voltage will be tightly regulated to track the half of chipset voltage for best performance. The IRU3038 together with dual N-channel MOSFETs such as IRF7313, provide a low cost solution for such applications. This device features a programmable frequency set from 200KHz to 400KHz, under-voltage lockout for both Vcc and Vc supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

TYPICAL APPLICATION

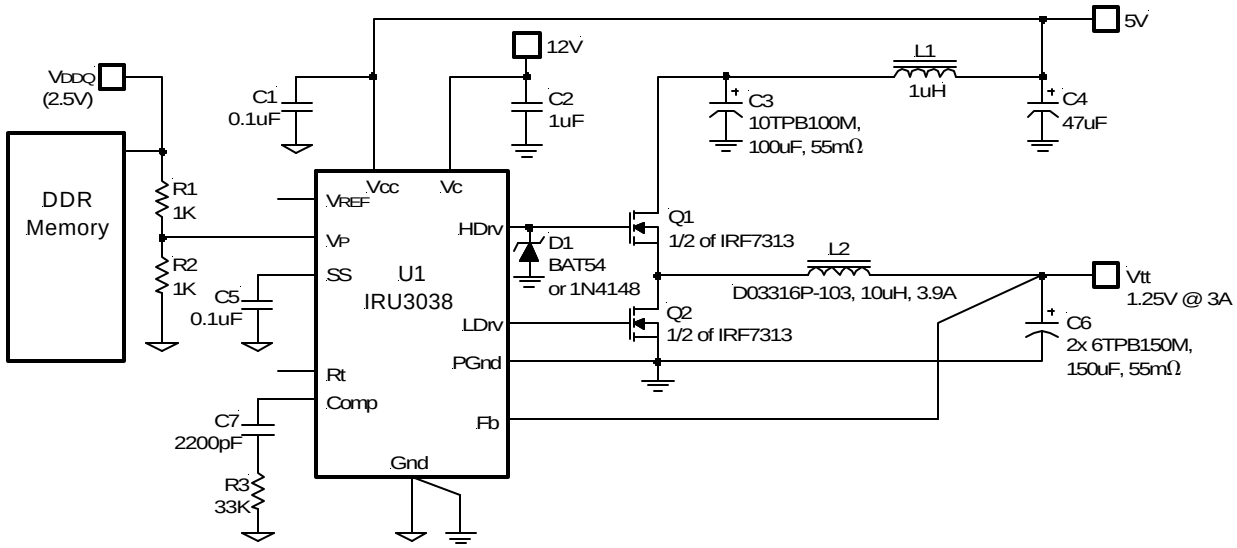


Figure 1 - Typical application of IRU3038 when Vtt tracks the V_{DDQ}.

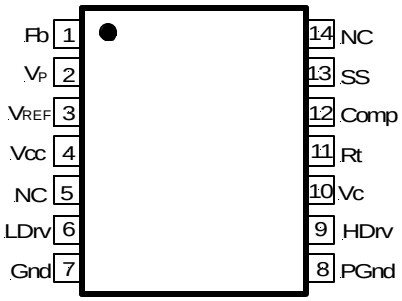
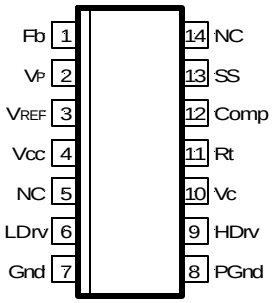
PACKAGE ORDER INFORMATION

T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3038CF	14-Pin Plastic TSSOP (F)
0 To 70	IRU3038CS	14-Pin Plastic SOIC NB (S)

ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage 25V
Vc Supply Voltage ..... 30V (not rated for inductive load)
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

14-PIN PLASTIC TSSOP (F)	14-PIN PLASTIC SOIC (S)
	
θ_{JA}=100°C/W	θ_{JA}=88°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=5V, Vc=12V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage						
V_{REF} Voltage	V_{FB}		1.225	1.250	1.275	V
Fb Voltage Line Regulation	L_{REG}	5<Vcc<12		0.2	0.35	%
UVLO						
UVLO Threshold - Vcc	UVLO Vcc	Supply Ramping Up	4	4.2	4.4	V
UVLO Hysteresis - Vcc				0.25		V
UVLO Threshold - Vc	UVLO Vc	Supply Ramping Up	3.1	3.3	3.5	V
UVLO Hysteresis - Vc				0.2		V
UVLO Threshold - Fb	UVLO Fb	Fb Ramping Down	0.4	0.6	0.8	V
UVLO Hysteresis - Fb				0.1		V
Supply Current						
Vcc Dynamic Supply Current	Dyn Icc	Freq=200KHz, C_L=1500pF	2	5	8	mA
Vc Dynamic Supply Current	Dyn Ic	Freq=200KHz, C_L=1500pF	2	7	10	mA
Vcc Static Supply Current	I_{CCQ}	SS=0V	1	3.5	6	mA
Vc Static Supply Current	I_{CQ}	SS=0V	0.5	1	4.5	mA
Soft-Start Section						
Charge Current	SS_{IB}	SS=0V	-10	-20	-30	µA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Amp						
Fb Voltage Input Bias Current	I_{FB1}	SS=3V, Fb=1V		-0.1		µA
Fb Voltage Input Bias Current	I_{FB2}	SS=0V, Fb=1V		-64		µA
V_P Voltage Range			0.8		1.5	V
Transconductance	gm		450	600	750	µmho
Oscillator						
Frequency	Freq	Rt=Open	180	200	220	KHz
		Rt=Gnd	360	400	440	
Ramp Amplitude	V_{RAMP}		1.225	1.25	1.275	V
Output Drivers						
Rise Time	T_r	C_{LOAD}=1500pF		50	100	ns
Fall Time	T_f	C_{LOAD}=1500pF		50	100	ns
Dead Band Time	T_{DB}		50	150	250	ns
Max Duty Cycle	T_{ON}	Fb=1V, Freq=200KHz	85	90	95	%
Min Duty Cycle	T_{OFF}	Fb=1.5V	0	0		%

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Fb	This pin is connected directly to the output of the switching regulator via resistor divider to provide feedback to the Error amplifier.
2	V_P	Non-inverting input of error amplifier.
3	V_{REF}	Reference Voltage.
4	Vcc	This pin provides biasing for the internal blocks of the IC as well as power for the low side driver. A minimum of 1µF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
5 14	NC	No Connection.
6	LDrv	Output driver for the synchronous power MOSFET.
7	Gnd	Analog ground for internal reference and control circuitry. Connect to PGnd with a short trace.
8	PGnd	This pin serves as the separate ground for MOSFET's drivers and should be connected to system's ground plane. A high frequency capacitor (0.1 to 1µF) must be connected from Vcc and Vc pins to this pin for noise free operation.
9	HDrv	Output driver for the high side power MOSFET. Connect a diode, such as BAT54 or 1N4148, from this pin to ground for the application when the inductor current goes negative (Source/ Sink), soft-start at no load and for the fast load transient from full load to no load.
10	Vc	This pin is connected to a voltage that must be at least 4V higher than the bus voltage of the switcher (assuming 5V threshold MOSFET) and powers the high side output driver. A minimum of 1µF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
11	Rt	The switching frequency can be Programmed between 200KHz and 400KHz by connecting a resistor between Rt and Gnd. Floating the pin set the switching frequency to 200KHz and grounding the pin set the switching frequency to 400KHz.
12	Comp	Compensation pin of the error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
13	SS	This pin provides soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the output of the switching regulator, preventing it from overshooting as well as limiting the input current. The converter can be shutdown by pulling this pin below 0.5V.

BLOCK DIAGRAM

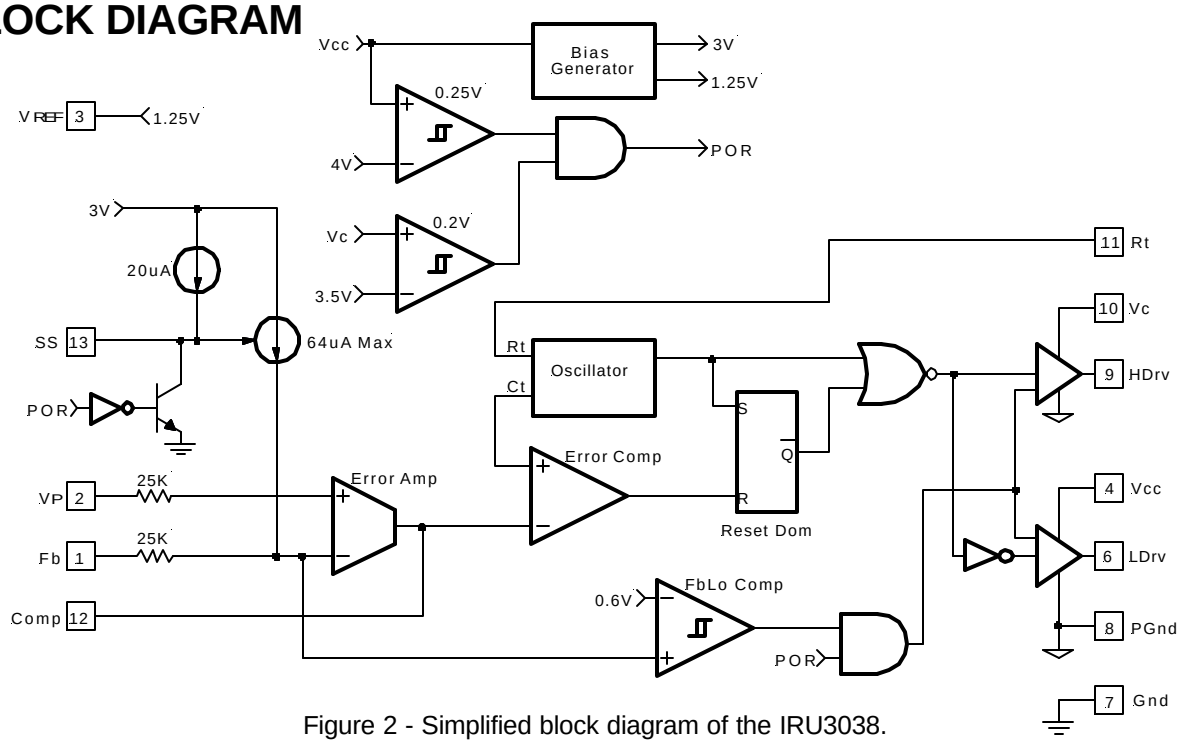


Figure 2 - Simplified block diagram of the IRU3038.

THEORY OF OPERATION

Introduction

The IRU3038 is a fixed frequency, voltage mode synchronous controller and consists of a precision reference voltage, an uncommitted error amplifier, an internal oscillator, a PWM comparator, 0.5A peak gate driver, soft-start and shutdown circuits (see Block Diagram).

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier; this is the amplified error signal from the sensed output voltage and the voltage on non-inverting input of error amplifier(V_P). This voltage is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulses of variable duty-cycle, which drives the two N-channel external MOSFETs.

The timing of the IC is provided through an internal oscillator circuit which uses on-chip capacitor. The oscillation frequency is programmable between 200 to 400KHz by using an external resistor. Figure 12 shows switching frequency vs. external resistor (Rt).

Soft-Start

The IRU3038 has a programmable soft-start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vc and Vcc rise above their threshold (3.3V and 4.2V respectively) and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter. As the charging voltage of the external capacitor ramps up, the PWM signals increase from zero to the point the feedback loop takes control.

Short-Circuit Protection

The outputs are protected against the short-circuit. The IRU3038 protects the circuit for shorted output by sensing the output voltage (through the external resistor divider). The IRU3038 shuts down the PWM signals, when the output voltage drops below 0.6V.

The IRU3038 also protects the output from over-voltaging when the control FET is shorted. This is done by turning on the sync FET with the maximum duty cycle.

Under-Voltage Lockout

The under-voltage lockout circuit assures that the MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if Vc and Vcc fall below 3.3V and 4.2V respectively. Normal operation resumes once Vc and Vcc rise above the set values.

APPLICATION INFORMATION

Design Example:
The following example is a typical application for IRU3038, the schematic is Figure 11 on page 12.

V_{IN} = 5V
V_{OUT} = 2.5V
I_{OUT} = 8A
ΔV_{OUT} = 100mV
f_S = 200KHz

Output Voltage Programming
Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is referenced to the voltage on non-inverting pin of error amplifier. For this application, this pin (V_P) is connected to reference voltage (V_{REF}). The output voltage is defined by using the following equation:

$$V_{OUT} = V_P \times \left(1 + \frac{R_6}{R_5}\right) \qquad ---(1)$$

$V_P = V_{REF}$ = 1.25V

When an external resistor divider is connected to the output as shown in Figure 3.

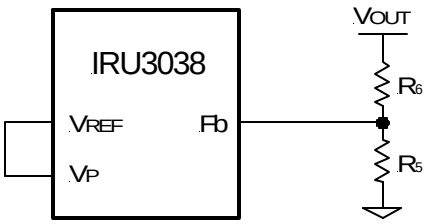


Figure 3 - Typical application of the IRU3038 for programming the output voltage.

Equation (1) can be rewritten as:

$$R_6 = R_5 \times \left(\frac{V_{OUT}}{V_P} - 1\right)$$

Choose R_5 = 1KΩ
This will result to R_6 = 1KΩ

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-Start Programming
The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated by using:

$$t_{START} = 75 \times Css \quad (ms) \qquad ---(2)$$

Where C_{SS} is the soft-start capacitor (μF)

For a start-up time of 7.5ms, the soft-start capacitor will be 0.1μF. Choose a ceramic capacitor at 0.1μF.

Shutdown
The converter can be shutdown by pulling the soft-start pin below 0.5V. The control MOSFET turns off and the synchronous MOSFET turns on during shutdown.

Boost Supply Vc
To drive the high-side switch it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 11. The capacitor is charged up to approximately twice the bus voltage. A capacitor in the range of 0.1μF to 1μF is generally adequate for most applications. In application, when a separate voltage source is available the boost circuit can be avoided as shown in Figure 1.

Input Capacitor Selection
The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of control MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_{OUT}\sqrt{D \times (1\text{-}D)} \qquad ---(3)$$

Where:
D is the Duty Cycle, $D=V_{OUT}/V_{IN}$.
I_{RMS} is the RMS value of the input capacitor current.
I_{OUT} is the output current for each channel.

For V_{IN}=5V, I_{OUT}=8A and D=0.5, the I_{RMS}=4A

For higher efficiency, a low ESR capacitor is recommended. Choose two Poscap from Sanyo 10TPB100ML (10V, 100μF, 55mΩ) with a maximum allowable ripple current of 1.9A.

Output Capacitor Selection

The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$ESR \leq \frac{\Delta V_O}{\Delta I_O} \qquad ---(4)$$

Where:
ΔV_O = Output Voltage Ripple
ΔI_O = Output Current
ΔV_O=100mV and ΔI_O=4A
This results to: ESR=25mΩ

The Sanyo TPC series, Poscap capacitor is a good choice. The 6TPC150M 150μF, 6.3V has an ESR 40mΩ. Selecting two of these capacitors in parallel, results to an ESR of $\cong$ 20mΩ which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi). The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \; ; \; \Delta t = D \times \frac{1}{f_S} \; ; \; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \qquad ---(5)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OUT} = Output Voltage
Δi = Inductor Ripple Current
f_S = Switching Frequency
Δt = Turn On Time
D = Duty Cycle

If $\Delta i = 30\%(I_O)$, then the output inductor will be:

$L = 2.6\mu H$

The Coilcraft DO5022HC series provides a range of inductors in different values, low profile suitable for large currents, 3.3μH, 10A is a good choice for this application. This will result to a ripple approximately 26.5% of output current.

Power MOSFET Selection

The IRU3038 uses two N-Channel MOSFETs. The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{IN}).

The gate drive requirement is almost the same for both MOSFETs. Logic-level transistor can be used and caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter, the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{COND} \text{ (Upper Switch)} = I_{LOAD}^2 \times R_{DS(ON)} \times D \times \vartheta$$

$$P_{COND} \text{ (Lower Switch)} = I_{LOAD}^2 \times R_{DS(ON)} \times (1 - D) \times \vartheta$$

$\vartheta = R_{DS(ON)}$ Temperature Dependency

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

Choose IRF7460 for both control MOSFET and synchronous MOSFET. This device provides low on-resistance in a compact SOIC 8-Pin package.

The MOSFET has the following data:

IRF7460
V_{DSS} = 20V
I_D = 10A @ 75°C
$R_{DS(ON)}$ = 10mΩ @ V_{GS}=10V
ϑ = 1.8 for 150°C (Junction Temperature)

The total conduction losses will be:

$P_{CON(TOTAL)}$ = 1.152W

The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turnoff delays and rise and fall times. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \qquad ---(6)$$

Where:
$V_{DS(OFF)}$ = Drain to Source Voltage at off time
t_r = Rise Time
t_f = Fall Time
T = Switching Period
I_{LOAD} = Load Current

The switching time waveform is shown in Figure 4.

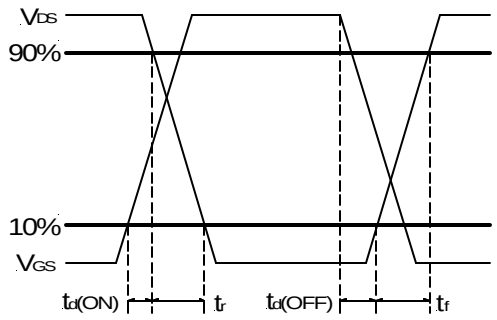


Figure 4 - Switching time waveforms.

From IRF7460 data sheet we obtain:

t_r = 6.9ns
t_f = 4.3ns

These values are taken under a certain condition test. For more detail please refer to the IRF7460 data sheet.

By using equation (6), we can calculate the total switching losses.

$P_{SW(TOTAL)}$ = 44.8mW

Feedback Compensation

The IRU3038 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 5). The Resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad ---(7)$$

Figure 5 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

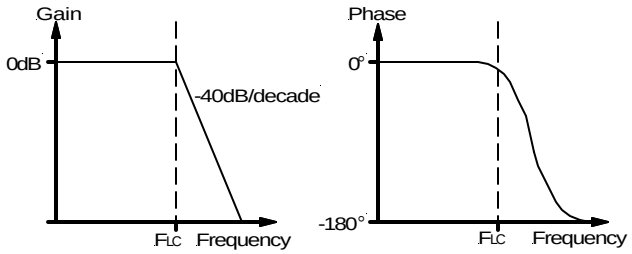


Figure 5 - Gain and phase of LC filter.

The IRU3038's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback, the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in Figure 6.

Note that this method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general, the output capacitor's ESR generates a zero typically at 5KHz to 50KHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \qquad ---(8)$$

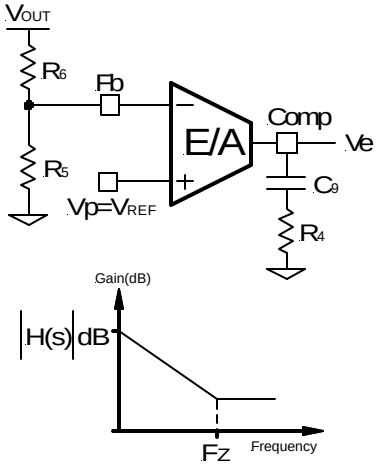


Figure 6 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / V_{OUT}) is given by:

$$H(s) = \left(g_m \times \frac{R_5}{R_6 + R_5}\right) \times \frac{1 + sR_4C_9}{sC_9} \qquad ---(9)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = g_m \times \frac{R_5}{R_6 \times R_5} \times R_4 \qquad ---(10)$$

$$F_Z = \frac{1}{2\pi \times R_4 \times C_9} \qquad ---(11)$$

The gain is determined by the voltage divider and E/A's transconductance gain.

First select the desired zero-crossover frequency (Fo):

$Fo > F_{ESR}$ and $Fo \leq (1/5 \sim 1/10) \times f_S$

Use the following equation to calculate R_4:

$$R_4 = \frac{V_{OSC}}{V_{IN}} \times \frac{Fo \times F_{ESR}}{F_{LC}^2} \times \frac{R_5 + R_6}{R_5} \times \frac{1}{g_m} \qquad ---(12)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Fo = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_5 and R_6 = Resistor Dividers for Output Voltage Programming
g_m = Error Amplifier Transconductance

For:
V_{IN} = 5V
V_{OSC} = 1.25V
Fo = 30KHz
F_{ESR} = 26.5KHz
F_{LC} = 5KHz
R_5 = 1K
R_6 = 1K
g_m = 600µmho

This results to R_4=26.52KΩ. Choose R_4=26.1KΩ

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$F_Z \cong 75\% F_{LC}$

$$F_Z \cong 0.75 \times \frac{1}{2\pi\sqrt{L_O \times C_O}} \qquad ---(13)$$

For:
Lo = 10µH
Co = 300µF
F_Z = 3.8KHz
R_4 = 26.1KΩ

Using equations (11) and (13) to calculate C_9, we get:

$C_9 \cong$ 1800pF

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to suppress the switching noise. The additional pole is given by:

$$F_P = \frac{1}{2\pi \times R_4 \times \frac{C_9 \times C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi \times R_4 \times f_S - \frac{1}{C_9}} \cong \frac{1}{\pi \times R_4 \times f_S}$$

for $F_P << \frac{f_S}{2}$

For a general solution for unconditionally stability for ceramic capacitor with very low ESR and any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 7.

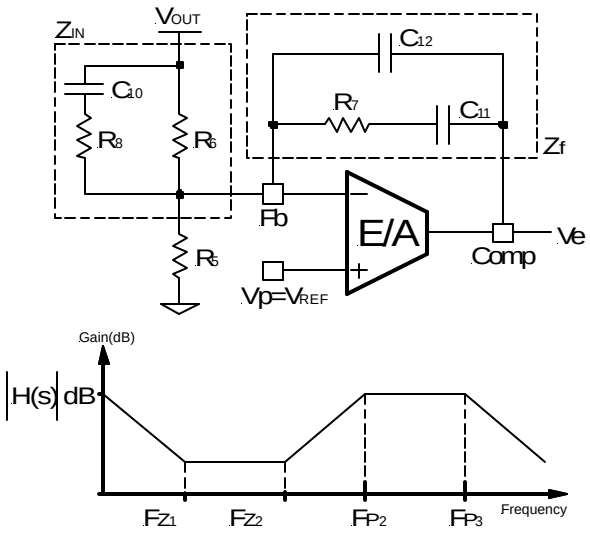


Figure 7 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m Z_f >> 1 \quad \text{and} \quad g_m Z_{IN} >> 1 \qquad \text{---(14)}$$

By replacing Z_{IN} and Z_f according to Figure 7, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11}) \times [1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12}C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+sR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_O = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \qquad \text{---(15)}$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Lo = Output Inductor
Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition (14) regarding transconductance error amplifier.

1) Select the crossover frequency:
$F_O < F_{ESR}$ and $F_O \leq (1/10 \sim 1/6) \times f_S$

2) Select R_7, so that $R_7 >> \frac{2}{g_m}$

3) Place first zero before LC's resonant frequency pole.
$F_{Z1} \cong 75\% F_{LC}$

$$C_{11} = \frac{1}{2\pi \times F_{Z1} \times R_7}$$

4) Place third pole at the half of the switching frequency.

$$F_{P3} = \frac{f_S}{2}$$

$$C_{12} = \frac{1}{2\pi \times R_7 \times F_{P3}}$$

$C_{12} > 50pF$
If not, change R_7 selection.

5) Place R_7 in equation (15) and calculate C_{10}:

$$C_{10} \leq \frac{2\pi \times Lo \times F_O \times Co}{R_7} \times \frac{V_{OSC}}{V_{IN}}$$

6) Place second pole at the ESR zero.

$F_{P2} = F_{ESR}$

$$R_8 = \frac{1}{2\pi \times C_{10} \times F_{P2}}$$

Check if $R_8 > \frac{1}{gm}$

If R_8 is too small, increase R_7 and start from step 2.

7) Place second zero around the resonant frequency.

$F_{Z2} = F_{LC}$

$$R_6 = \frac{1}{2\pi \times C_{10} \times F_{Z2}} - R_8$$

8) Use equation (1) to calculate R_5:

$$R_5 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_6$$

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

IC Quiescent Power Dissipation

Power dissipation for IC controller is a function of applied voltage, gate driver loads and switching frequency. The IC's maximum power dissipation occurs when the IC operating with single 12V supply voltage (Vcc=12V and Vc≅24V) at 400KHz switching frequency and maximum gate loads.

This IC's power dissipation results to an excessive temperature rise and should be considered when using IRU3038 for such an application.

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components. Make all the connections in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET. To reduce the ESR, replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources and be placed close to the IC. In multilayer PCB, use one layer as power ground plane and have a separate control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

TYPICAL PERFORMANCE CHARACTERISTICS

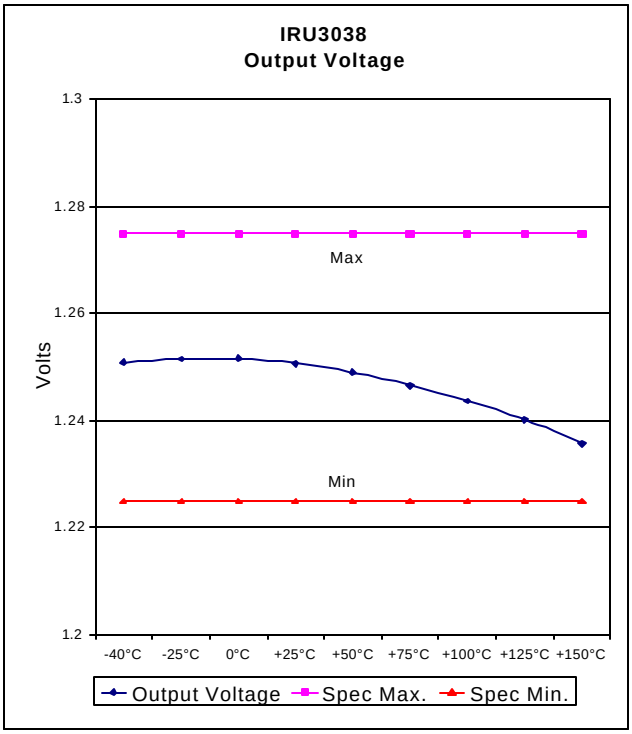


Figure 8 - Output voltage of IRU3038.

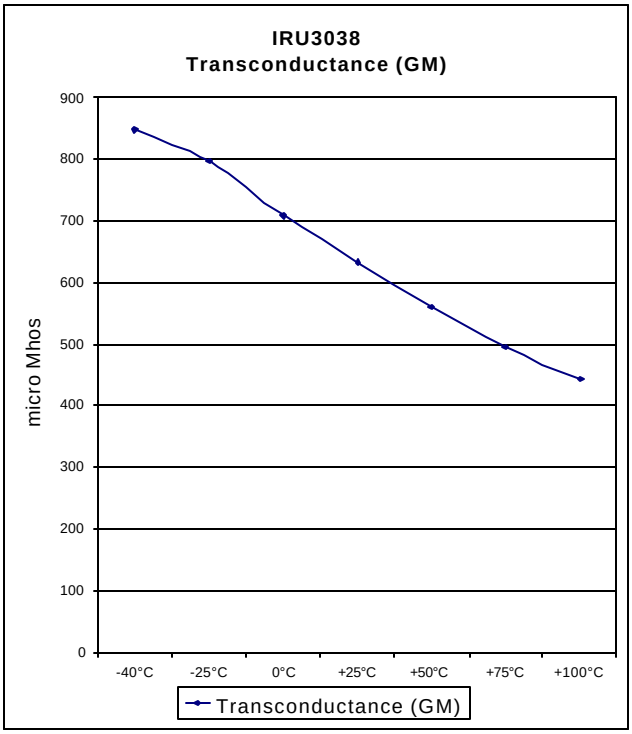


Figure 9 - Transconductance of IRU3038.

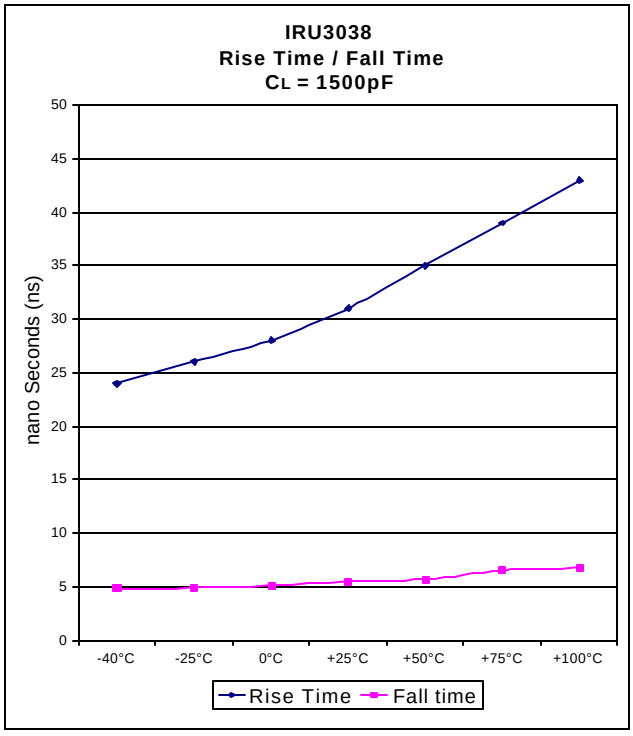


Figure 10 - Rise and fall time of IRU3038.

TYPICAL APPLICATION

Single Supply 5V Input

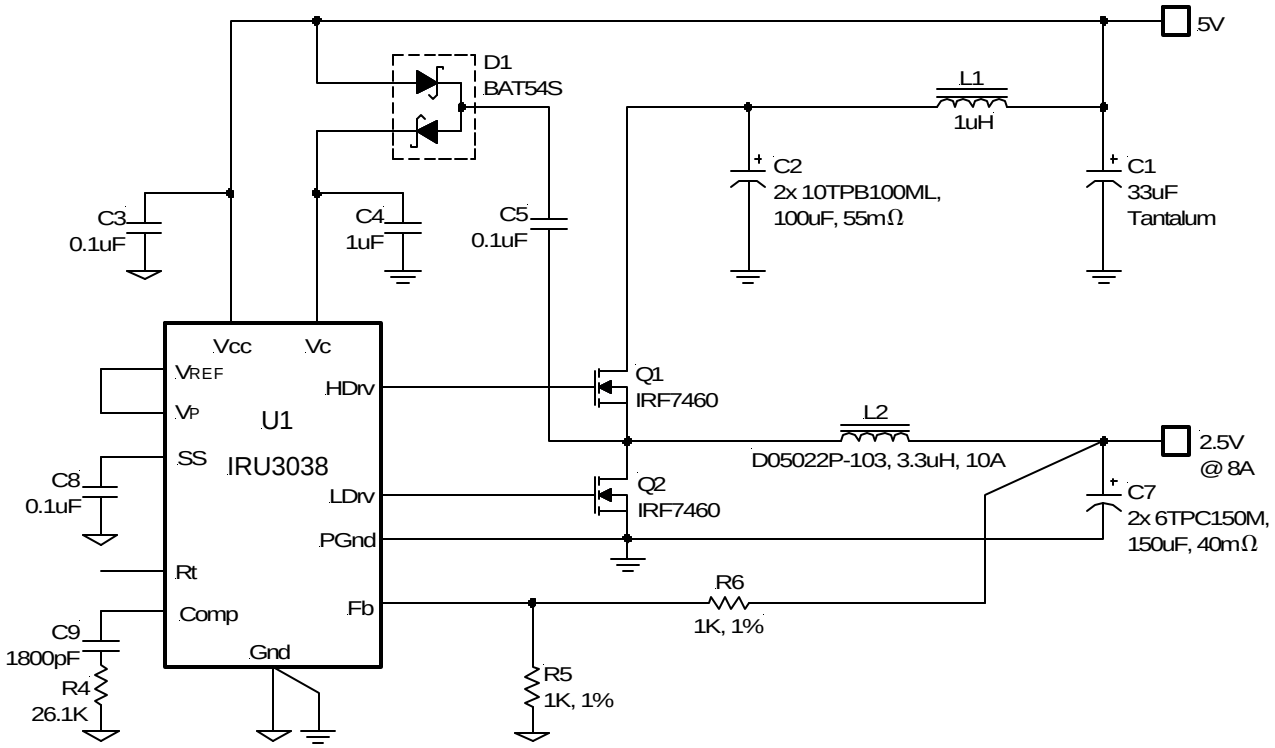


Figure 11 - Typical application of IRU3038 in an on-board DC-DC converter using a single 5V supply.

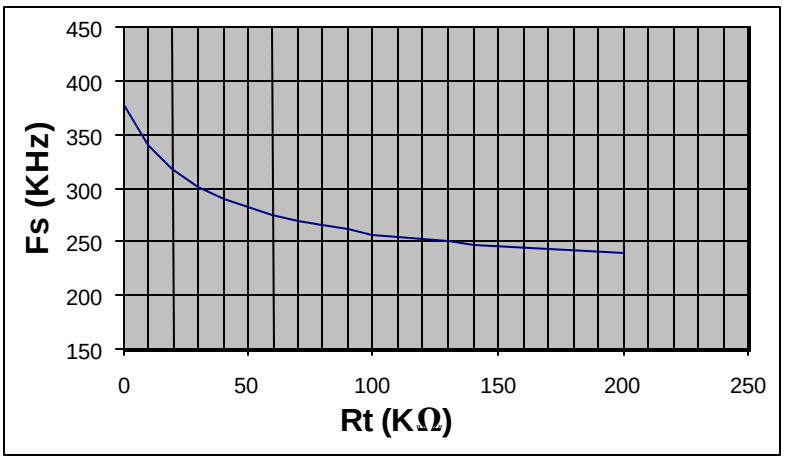


Figure 12 - Switching frequency vs. Rt.

TYPICAL APPLICATION

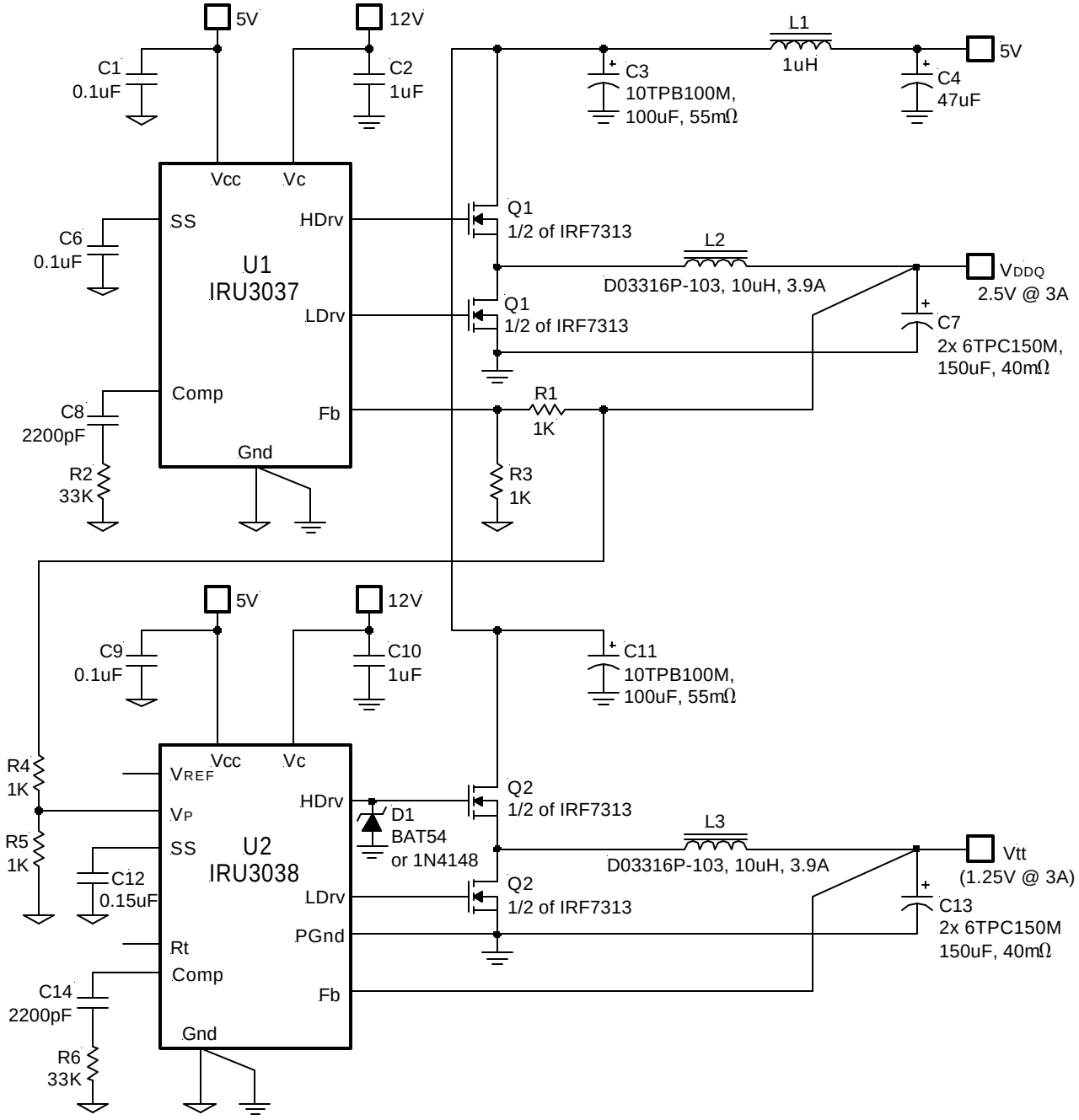


Figure 13 - Typical application of IRU3038 for DDR memory when the termination voltage tracks the core voltage generated by IRU3037.

DEMO-BOARD APPLICATION

5V to 2.5V @ 8A

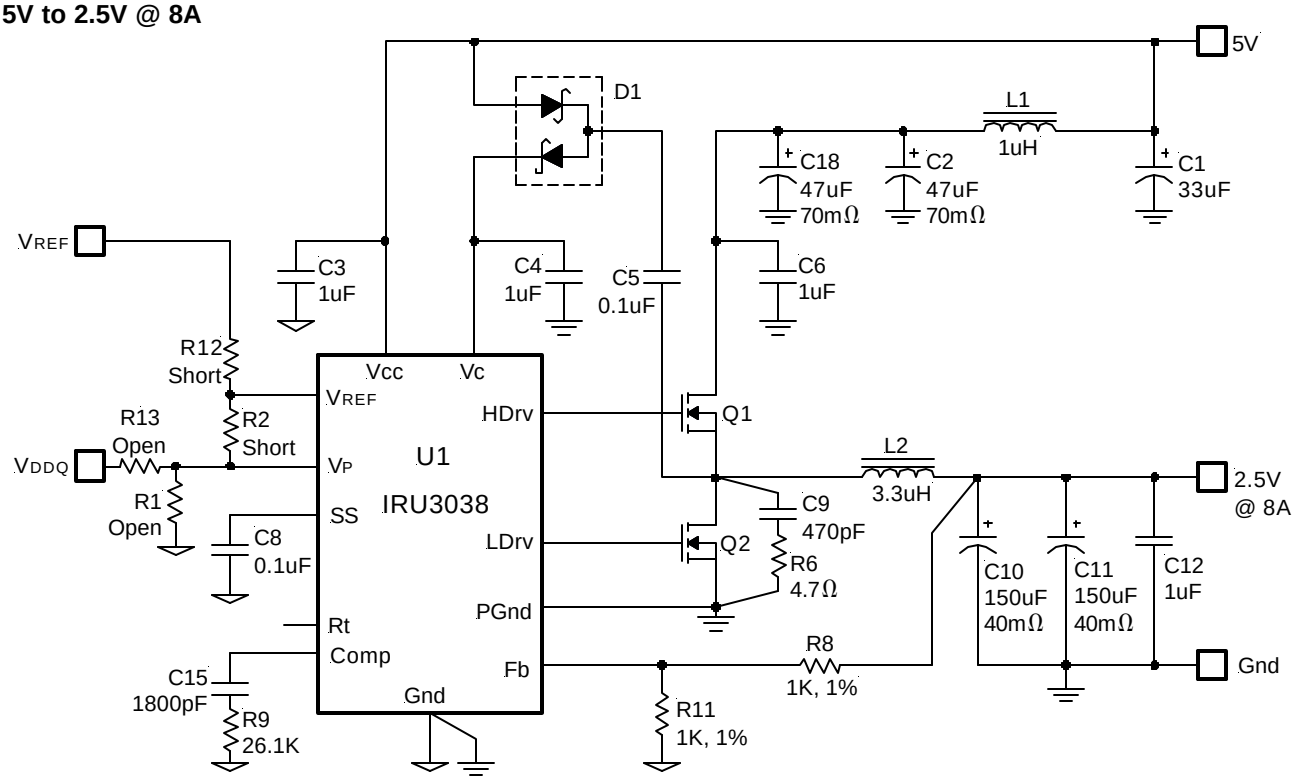


Figure 14 - Demo-board application of IRU3038.

Application Parts List

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1, Q2	MOSFET	20V, 10mΩ, 12A	2	IRF7460	IR	irf.com
U1	Controller	Synchronous PWM	1	IRU3038	IR	
D1	Diode	Fast Switching, Schottky	1	BAT54S	IR	
L1	Inductor	1µH, 10A	1	D03316P-102HC	Coilcraft	coilcraft.com
L2	Inductor	3.3µH, 12A	1	D05022P-332HC	Coilcraft	
C1	Cap, Tantalum	33µF, 16V	1	ECS-T1CD336R	Panasonic	maco.panasonic.co.jp
C2,C18	Cap, Poscap	47µF, 16V, 70mΩ	2	16TPB47M	Sanyo	sanyo.com/industrial
C10,C11	Cap, Poscap	150µF, 6.3V, 40mΩ	2	6TPC150M	Sanyo	
C5,C8	Cap, Ceramic	0.1µF, Y5V, 25V	2	ECJ-2VF1E104Z	Panasonic	maco.panasonic.co.jp
C4	Cap, Ceramic	1µF, X7R, 25V	1	ECJ-3YB1E105K	Panasonic	
C15	Cap, Ceramic	1800pF, X7R, 50V	1	ECJ-2VB1H182K	Panasonic	
C9	Cap, Ceramic	470pF, X7R	1	ECJ-2VB2D471K	Panasonic	
C3,C6,C12	Cap, Ceramic	1µF, Y5V, 16V	3	ECJ-2VF1C105Z	Panasonic	
R9	Resistor	26.1K, 5%	1			
R6	Resistor	4.7Ω, 5%	1			
R8,R11	Resistor	1K, 1%	2			

TYPICAL PERFORMANCE CHARACTERISTICS

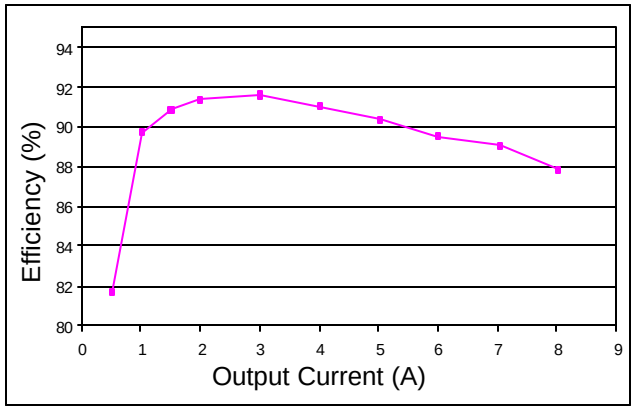


Figure 15 - Efficiency for IRU3038 Evaluation Board. V_{IN}=5V, V_{OUT}=2.5V

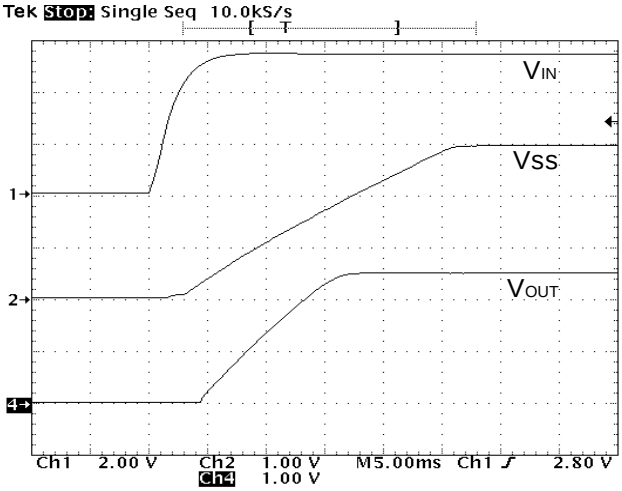


Figure 16 - Start-up time @ I_{OUT}=5A.

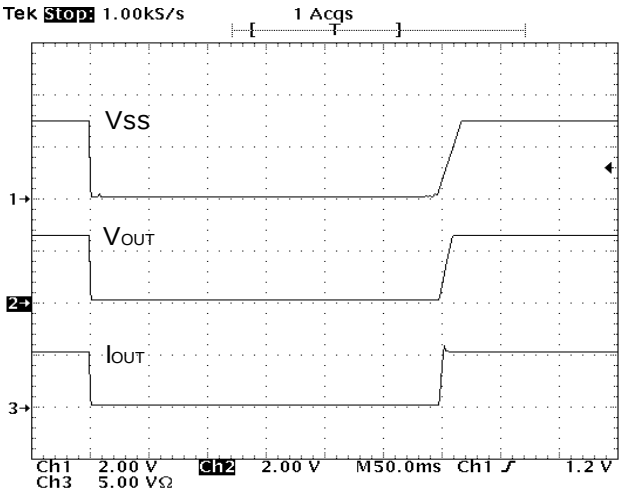


Figure 17 - Shutdoown the output by pulling down the soft-start.

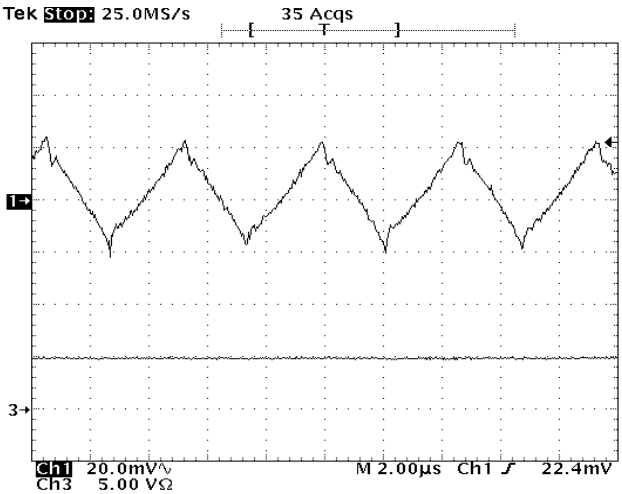


Figure 18 - 3.3V output voltage ripple @ I_{OUT}=5A.

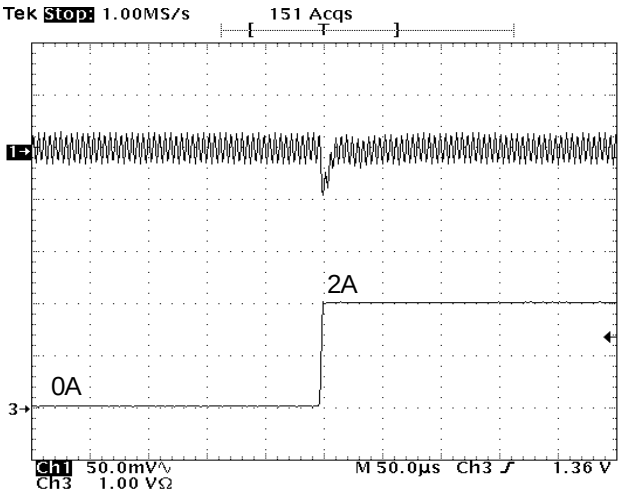


Figure 19 - Transient response @ I_{OUT}=0 to 2A.

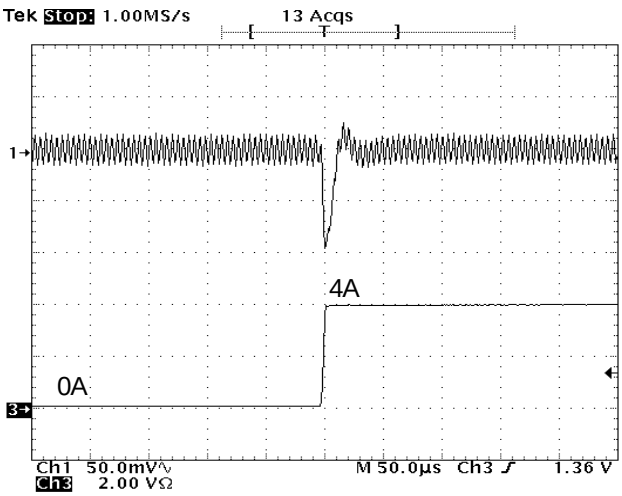
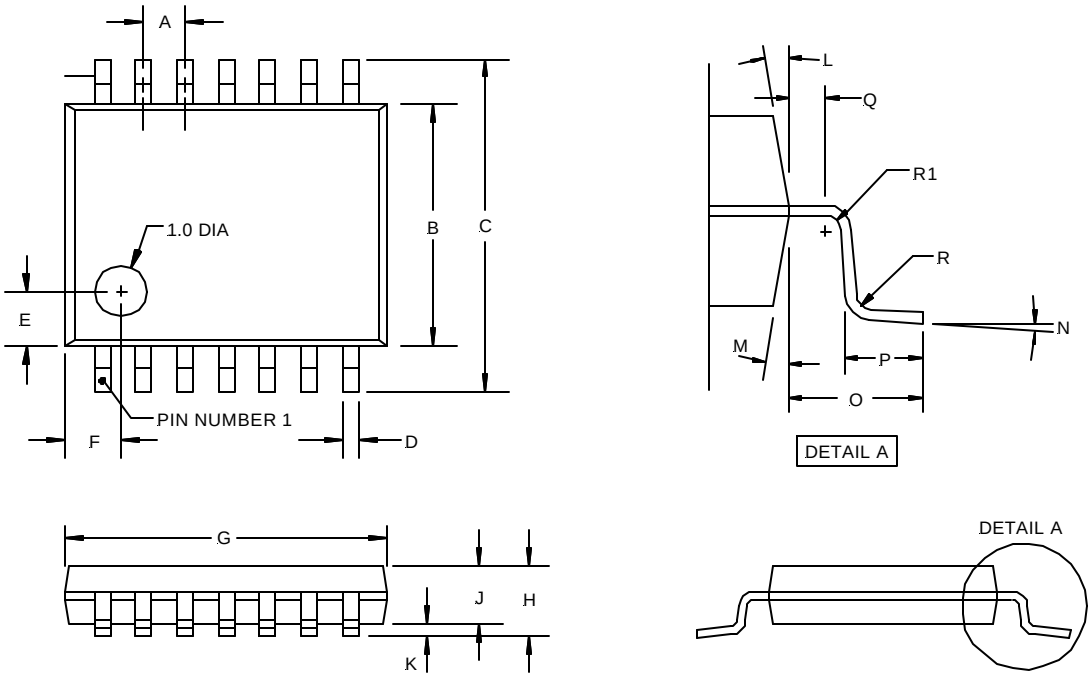


Figure 20 - Transient response @ I_{OUT}=0 to 4A.

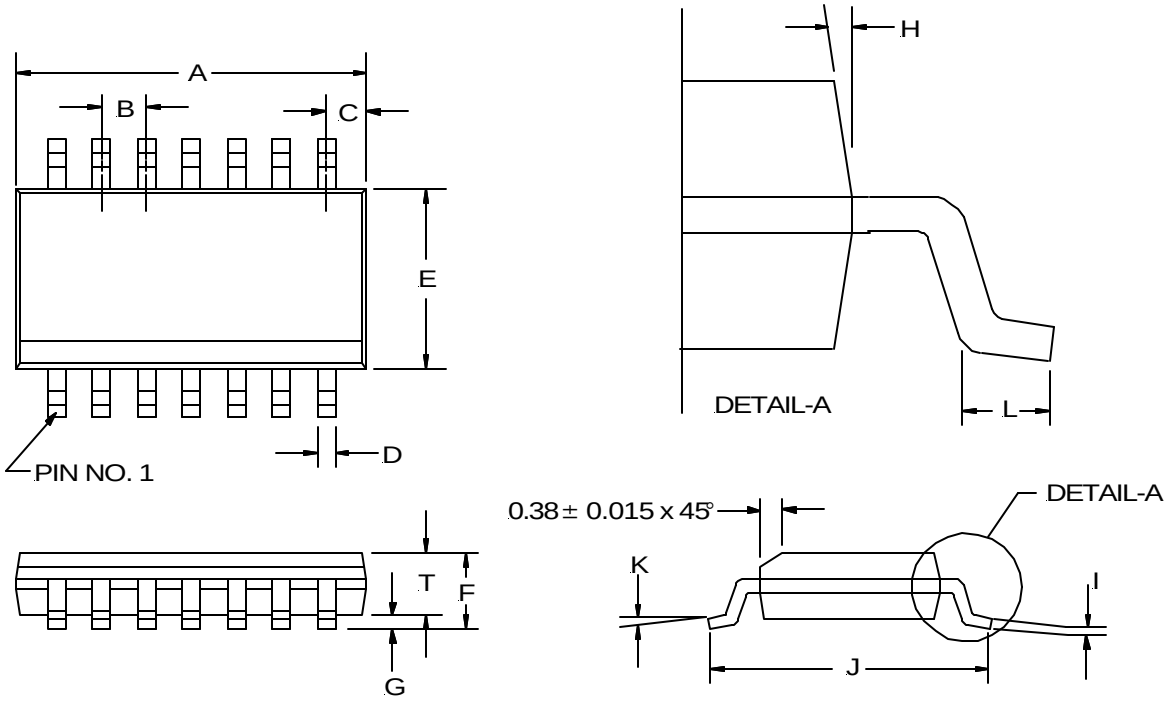
(F) TSSOP Package
14-Pin



SYMBOL	14-PIN		
DESIG	MIN	NOM	MAX
A		0.65 BSC	
B	4.30	4.40	4.50
C		6.40 BSC	
D	0.19	---	0.30
E		1.00	
F		1.00	
G	4.90	5.00	5.10
H	---	---	1.10
J	0.85	0.90	0.95
K	0.05	---	0.15
L		12° REF	
M		12° REF	
N	0°	---	8°
O		1.00 REF	
P	0.50	0.60	0.75
Q		0.20	
R	0.09	---	---
R1	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

(S) SOIC Package
14-Pin Surface Mount, Narrow Body



14-PIN		
SYMBOL	**MIN**	**MAX**
A	8.56	8.74
B	1.27 BSC	
C	0.51 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
F	TSSOP Plastic	14	100	2500	Fig A
S	SOIC, Narrow Body	14	55	2500	Fig B

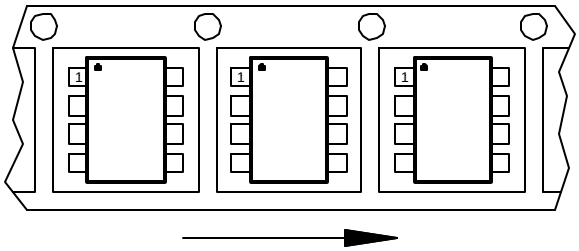


Figure A

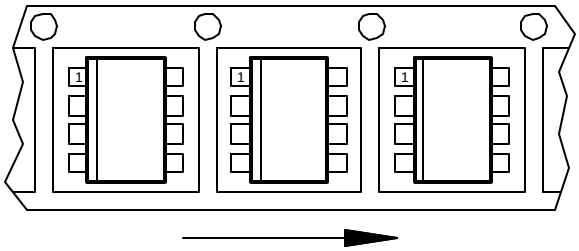


Figure B

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information

IRU3046

DUAL SYNCHRONOUS PWM CONTROLLER WITH CURRENT SHARING CIRCUITRY AND LDO CONTROLLER

PRELIMINARY DATA SHEET

FEATURES

- Dual Synchronous Controller in 24-Pin Package with 180° out-of-phase operation
- LDO Controller with Independent Bias Supply
- Can be configured as 2-Independent or 2-Phase PWM Controller
- Programmable Current Sharing in 2-Phase Configuration
- Flexible, Same or Separate Supply Operation
- Operation from 4V to 25V Input
- Programmable Switching Frequency up to 400KHz
- Soft-Start controls all outputs
- Precision Reference Voltage Available
- 500mA Peak Output Drive Capability
- Short Circuit Protection for all outputs
- Power Good Output
- Synchronizable with External Clock

DESCRIPTION

The IRU3046 IC combines a Dual synchronous Buck controller and a linear regulator controller, providing a cost-effective, high performance and flexible solution for multi-output applications. The Dual synchronous controller can be configured as 2-independent or 2-phase controller. In 2-phase configuration, the IRU3046 provides a programmable current sharing which is ideal when the output power exceeds any single input power budget. IRU3046 provides a separate adjustable output by driving a switch as a linear regulator. This device features programmable switching frequency up to 400KHz per phase, under-voltage lockout for all input supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

APPLICATIONS

- Dual-Phase Power Supply
- DDR Memory Source Sink Vtt Application
- Graphic Card
- Hard Disk Drive
- Power supplies requiring multiple outputs

TYPICAL APPLICATION

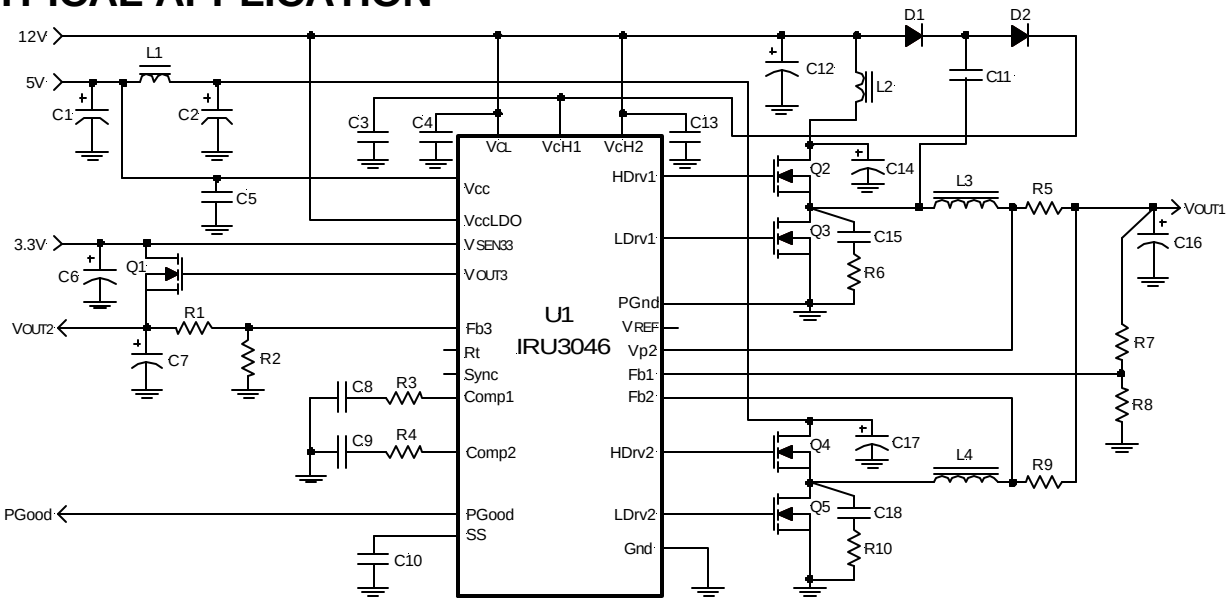


Figure 1 - Typical application of IRU3046 configured as 2-phase converter with current sharing.

PACKAGE ORDER INFORMATION

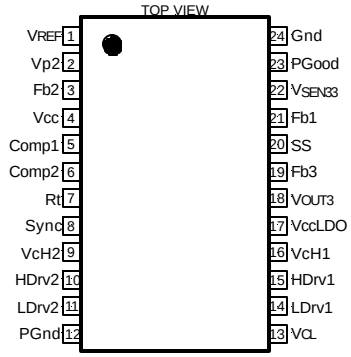
T_A (°C)	DEVICE	PACKAGE	FREQUENCY
0 To 70	IRU3046CF	24-Pin Plastic TSSOP (F)	200-400KHz

ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage 25V
VccLDO, VcH1, VcH2 and V_{CL} Supply Voltage ..... 30V (not rated for inductive load)
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

24-PIN PLASTIC TSSOP (F)



θ_{JA} = 84°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=5V, VcH1=VcH2=V_{CL}=VccLDO=12V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage Section						
Fb Voltage	V_{FB}		1.225	1.250	1.275	V
Fb Voltage Line Regulation	L_{REG}	5<Vcc<12		0.2		%
UVLO Section						
UVLO Threshold - Vcc	$UVLO_{Vcc}$	Supply Ramping Up		4.2		V
UVLO Hysteresis - Vcc				0.25		V
UVLO Threshold - VccLDO	$UVLO_{VccLDO}$	Supply Ramping Up		4.2		V
UVLO Hysteresis - VccLDO				0.25		V
UVLO Threshold - VcH1	$UVLO_{VcH1}$	Supply Ramping Up		3.5		V
UVLO Hysteresis - VcH1				0.2		V
UVLO Threshold - VcH2	$UVLO_{VcH2}$	Supply Ramping Up		3.5		V
UVLO Hysteresis - VcH2				0.2		V
UVLO Threshold - Fb	$UVLO_{Fb}$	Fb Ramping Down		0.6		V
UVLO Hysteresis - Fb				0.1		V
UVLO Threshold - V_{SEN33}	$UVLO_{VSEN33}$	Supply Ramping Up		2.5		V
UVLO Hysteresis - V_{SEN33}				0.2		V
Supply Current Section						
Vcc Dynamic Supply Current	Dyn I_{CC}	Freq=200KHz, C_L=1500pF		5		mA
VcH1 Dynamic Supply Current	Dyn I_{CH1}	Freq=200KHz, C_L=1500pF		7		mA
VcH2 Dynamic Supply Current	Dyn I_{CH2}	Freq=200KHz, C_L=1500pF		7		mA
Vcc Static Supply Current	I_{CCQ}	SS=0V		3.5		mA
VcH1 Static Supply Current	I_{CH1Q}	SS=0V		2		mA
VcH2 Static Supply Current	I_{CH2Q}	SS=0V		2		mA
VccLDO Static Supply Current	I_{CLDO}	SS=0V		1		mA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Soft-Start Section						
Charge Current	SS_{IB}	SS=0V	15	25	30	µA
Power Good Section						
Fb1 Lower Trip Point	PG_{FB1L}	Fb1 Ramping Down		$0.9V_{REF}$		V
Fb1 Upper Trip Point	PG_{FB1H}	Fb1 Ramping Up		$1.1V_{REF}$		V
Fb2 Lower Trip Point	PG_{FB2L}	Fb2 Ramping Down		$0.9V_{REF}$		V
Fb2 Upper Trip Point	PG_{FB2H}	Fb2 Ramping Up		$1.1V_{REF}$		V
Fb3 Lower Trip Point	PG_{FB3L}	Fb3 Ramping Down		$0.9V_{REF}$		V
Fb3 Upper Trip Point	PG_{FB3H}	Fb3 Ramping Up		$1.1V_{REF}$		V
Power Good Voltage OK	V_{PG}	5K resistor pulled up to 5V	4.5	4.8	5	V
Error Amp Section						
Fb Voltage Input Bias Current	I_{FB1}	SS=3V		-0.1		µA
Fb Voltage Input Bias Current	I_{FB2}	SS=0V		-64		µA
Transconductance 1	g_{m1}			400		µmho
Transconductance 2	g_{m2}			600		µmho
Input Offset Voltage for PWM2	$V_{OS(ERR)2}$	Fb2 to V_{P2}	-2	0	+2	mV
Oscillator Section						
Frequency	Freq	Rt=Open	180	200	220	KHz
		Rt=Gnd	300	350	450	
Ramp Amplitude	V_{RAMP}			1.25		V
Output Drivers Section						
Rise Time	Tr	C_L=1500pF		35	100	ns
Fall Time	Tf	C_L=1500pF		50	100	ns
Dead Band Time	T_{DB}		50	150	250	ns
Max Duty Cycle	T_{ON}	Fb=1V, Freq=200KHz	85	90		%
Min Duty Cycle	T_{OFF}	Fb=1.5V	0	0		%
LDO Controller Section						
Drive Current	I_{LDO}		30	45		mA
Fb Voltage	V_{FB}LDO		1.225	1.25	1.275	V
Input Bias Current	$I_{LDO(BIAS)}$			0.5	2	µA

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	V_{REF}	Reference Voltage.
2	Vp2	Non-inverting input to the second error amplifier. In the current sharing mode, it is connected to the programming resistor. In independent 2-channel mode it is connected to V_{REF} pin when Fb2 is connected to the resistor divider to set the output voltage.
3 21	Fb2 Fb1	Inverting inputs to the error amplifiers. In current sharing mode, Fb1 is connected to a resistor divider to set the output voltage and Fb2 is connected to programming resistor to achieve current sharing. In independent 2-channel mode, these pins work as feedback inputs for each channel.
4	Vcc	Supply voltage for the internal blocks of the IC.
5,6	Comp1, Comp2	Compensation pins for the error amplifiers.
7	Rt	The switching frequency can be programmed between 200KHz and 400KHz by connecting a resistor between Rt and Gnd. By floating the pin, the switching frequency will be 200KHz and by grounding the pin, the switching frequency will be 400KHz.
8	Sync	The internal oscillator may be synchronized to an external clock via this pin.
9 16	VcH2 VcH1	Supply voltage for the high side output drivers. These are connected to voltages that must be at least 4V higher than their bus voltages (assuming 5V threshold MOSFET). A minimum of 1µF, high frequency capacitor must be connected from these pins to PGnd to provide peak drive current capability.

PIN#	PIN SYMBOL	PIN DESCRIPTION
10,15	HDrv2, HDrv1	Output driver for the high side power MOSFET. Connect a diode, such as BAT54 or 1N4148, from these pins to ground for the application when the inductor current goes negative (Source/Sink), soft-start at no load and for the fast load transient from full load to no load.
11,14	LDrv2, LDrv1	Output driver for the synchronous power MOSFET.
12	PGnd	This pin serves as the separate ground for MOSFET's driver and should be connected to the system's ground plane. A high frequency capacitor (0.1 to 1μF) must be connected from Vcc, V_{CL}, VcH1 and VcH2 pins to this pin for noise free operation.
13	V_{CL}	Supply voltage for the low side output drivers.
17	VccLDO	Separate input supply for LDO controller.
18	V_{OUT3}	Driver signal for the LDO's external transistor.
19	Fb3	LDO's feedback pin, connected to a resistor divider to set the output voltage of LDO.
20	SS	This pin provides soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the output of the switching regulator, preventing it from overshooting as well as limiting the input current. The converter can be shutdown by pulling this pin below 0.5V.
22	V_{SEN33}	Sense the LDO input voltage for UVLO.
23	PGood	Power good pin. This pin is a collector output that switches Low when any of the outputs are outside of the specified under voltage trip point.
24	Gnd	Analog ground for internal reference and control circuitry. Connect to PGnd with a short trace.

BLOCK DIAGRAM

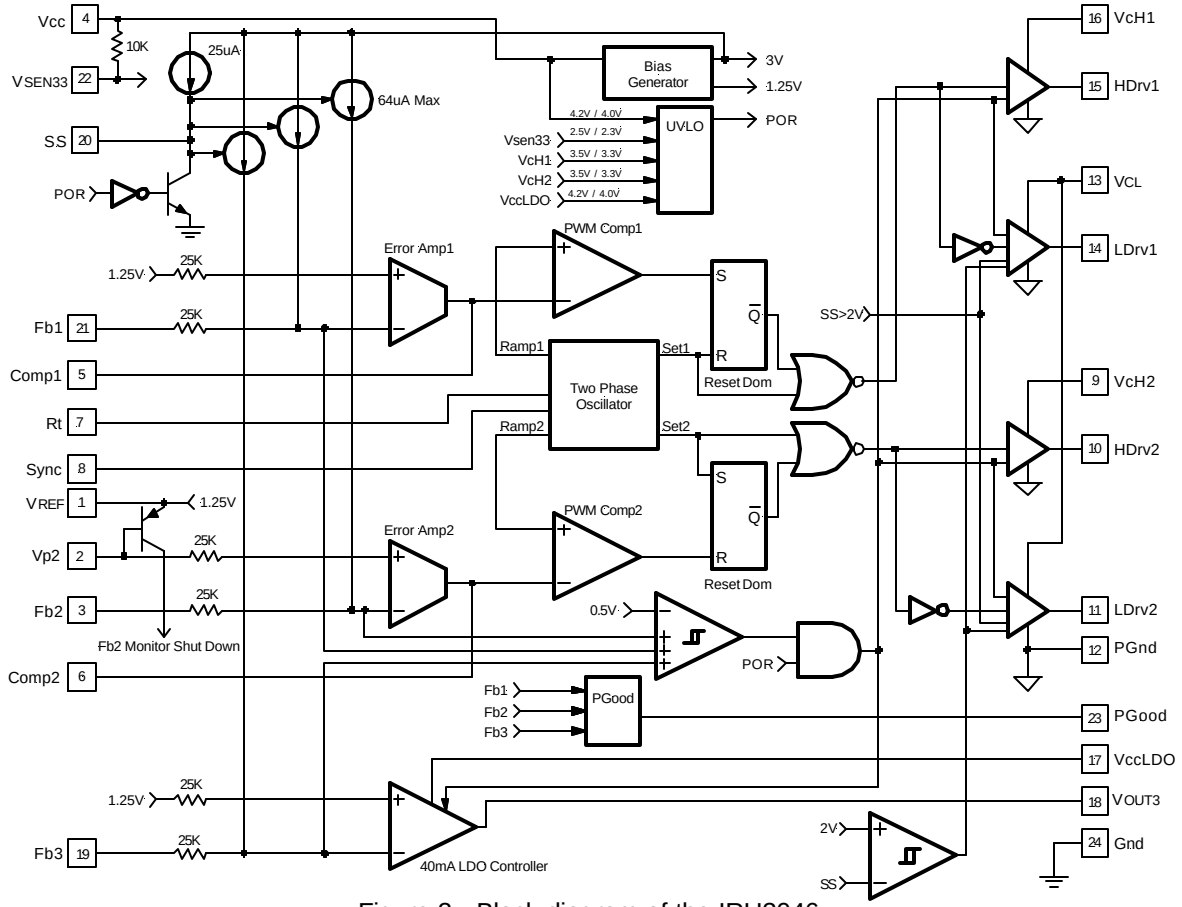


Figure 2 - Block diagram of the IRU3046.

THEORY OF OPERATION

Introduction
The IRU3046 is designed for multi-outputs applications. It includes two synchronous buck controllers and a linear regulator controller. The two synchronous controller operates with fixed frequency voltage mode and can be configured as two independent controller or 2-phase controller with current sharing. The timing of the IC is provided through an internal oscillator circuit. These are two out of phase oscillators and can be programmed by using an external resistor from 200KHz to 400KHz per phase. Figure 11 shows switching frequency versus external resistor.

Independent Mode
In this mode the IRU3046 provides two independent outputs with either common or different input voltages. The output voltage of the individual channel is set and controlled by the output of the error amplifier, this is the amplified error signal from the sensed output voltage and the reference voltage. This voltage is compared to the ramp signal and generates fixed frequency pulses of variable duty-cycle, which drives the two N-channel external MOSFETs.

Current Sharing Mode
In the current sharing mode, the two converter's outputs tied together and provide one single output (see Figure 1). In this mode, one control loop acts as a master and sets the output voltage as a regular Voltage Mode buck controller and the other control loop acts as a slave and monitors the current information for current sharing. The current sharing is programmable and sets by using two external resistors in output currents' path. The slave's error amplifier, error amplifier 2 (see Block Diagram) measures the voltage drops across the current sense resistors, the differential of these signals is amplified and compared with the ramp signal and generate the fixed frequency pulses of variable duty cycle to match the output currents.

Out of Phase Operation
The IRU3046 drives its two output stages 180° out of phase. In 2-phase configuration, the two inductor ripple currents cancel each other and result to a reduction of the output current ripple and contribute to a smaller output capacitor for the same ripple voltage requirement.

In application with single input voltage, the 2-phase configuration reduces the input ripple current. This results in much smaller RMS current in the input capacitor and reduction of input capacitor.

Soft-Start
The IRU3046 has a programmable soft start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vcc, VcH1, VcH2, VccLDO and $V_{SEN}33$ rise above their threshold and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter. As the charging voltage of the external capacitor ramps up, the PWM signals increase from zero to the point the feedback loop takes control.

Shutdown
The converter can be shutdown by pulling the soft-start pin below 0.5V. This can be easily done by using an external small signal transistor. During shutdown the MOSFET drivers and the LDO controller turn off.

Power Good
The IRU3046 provides a power good signal. This is an open collector output and it is pulled low if the output voltages are not within the specified threshold. This pin can be left floating if not used.

Short-Circuit Protection
The outputs are protected against the short circuit. The IRU3046 protects the circuit for shorted output by sensing the output voltages. The IRU3046 shuts down the PWM signals and LDO controller, when the output voltages drops below the set values.

Under-Voltage Lockout
The under-voltage lockout circuit assures that the MOSFET driver outputs and LDO controller remain in the off state whenever the supply voltages drop below set parameters. Normal operation resumes once the supply voltages rise above the set values.

Frequency Synchronization
The IRU3046 can be synchronized with an external clock signal. The synchronizing pulses must have a minimum pulse width of 100ns. If the sync function is not used, the Sync pin can be either connected to ground or be floating.

APPLICATION INFORMATION

Design Example:
The following example is a typical application for IRU3046 in current sharing mode. The schematic is Figure 13 on page 15.

For Switcher:	For Linear Regulator:
$V_{IN1(MASTER)}$ = 5V	V_{IN3} = 3.3V
$V_{IN2(SLAVE)}$ = 12V	V_{OUT2} = 2.5V
V_{OUT1} = 1.5V	I_{OUT2} = 2A
I_{OUT} = 16A	
ΔV_{OUT} = 75mV	
f_S = 200KHz	

PWM Section

Output Voltage Programming
Output voltage is programmed by reference voltage and external voltage divider. The Fb1 pin is the inverting input of the error amplifier, which is internally referenced to 1.25V. The divider is ratioed to provide 1.25V at the Fb1 pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT1} = V_{REF} \times \left(1 + \frac{R_6}{R_5}\right) \qquad ---(1)$$

When an external resistor divider is connected to the output as shown in Figure 3.

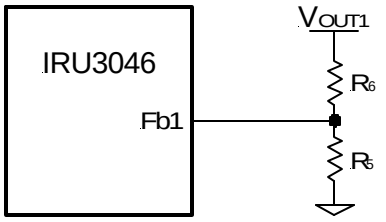


Figure 3 - Typical application of the IRU3046 for programming the output voltage.

Equation (1) can be rewritten as:

$$R_6 = R_5 \times \left(\frac{V_{OUT1}}{V_{REF}} - 1\right)$$

This will result to:
V_{OUT1} = 1.5V, V_{REF} = 1.25V, R_5 = 1K, R_6 = 200Ω

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-Start Programming
The soft-start timing can be programmed by selecting the soft start capacitance value. The start up time of the converter can be calculated by using:

$$t_{START} = 75 \times Css \quad (ms) \qquad ---(2)$$

Where:
C_{SS} is the soft-start capacitor (μF)

For a start-up time of 7.5ms, the soft-start capacitor will be 0.1μF. Choose a ceramic capacitor at 0.1μF.

Boost Supply
To drive the high-side switch it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 1. The capacitor is charged up to approximately twice the bus voltage. A capacitor in the range of 0.1μF to 1μF is generally adequate for most applications.

Sense Resistor Selection
These resistors will determine the current sharing between two channels. The relationship between the Master and Slave output currents is expressed by:

$$R_{SEN1} \times I_{MASTER} = R_{SEN2} \times I_{SLAVE} \qquad ---(3)$$

For an equal current sharing, R_{SEN1}=R_{SEN1}
Choose R_{SEN1}=R_{SEN2}=5mΩ

Input Capacitor selection
The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of control MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_{OUT} \sqrt{D \times (1\text{-}D)} \qquad ---(4)$$

Where:
D is the Duty Cycle, simply D=V_{OUT}/V_{IN}.
I_{RMS} is the RMS value of the input capacitor current.
I_{OUT} is the output current for each channel.

For V_{IN1}=5V, I_{OUT1}=8A and D1=0.3
Results to: I_{RMS1}=3.6A

And for V_{IN2}=12V, I_{OUT2}=8A and D2=0.125
Results to: I_{RMS2}=2.6A

For higher efficiency, a low ESR capacitor is recommended.

For V_{IN1}=5V, choose two Poscap from Sanyo 6TPB330M (6.3V, 330µF, 40mΩ, 3A)

For V_{IN2}=12V, choose two 16TPB47M (16V, 47µF, 70mΩ, 1.4A).

Output Capacitor Selection

The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$ESR \leq \frac{\Delta V_O}{\Delta I_O} \qquad ---(5)$$

Where:
ΔV_O = Output Voltage Ripple
ΔI_O = Output Current
ΔV_O=75mV and ΔI_O=10A, result to ESR=7.5mΩ

The Sanyo TPC series, Poscap capacitor is a good choice. The 6TPC150M 150µF, 6.3V has an ESR 40mΩ. Selecting six of these capacitors in parallel, results to an ESR of ≅ 7mΩ which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

The resulting output ripple current is smaller then each channel ripple current due to the 180° phase shift. These currents cancel each other. The cancellation is not the maximum because of the different duty cycle for each channel.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi); the optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \; ; \; \Delta t = D \times \frac{1}{f_S} \; ; \; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \qquad ---(6)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OUT} = Output Voltage
Δi = Inductor Ripple Current
f_S = Switching Frequency
Δt = Turn On Time
D = Duty Cycle

For Δi_1=30% of I_1, we get: L_1=2.18µH
For Δi_2=30% of I_2, we get: L_2=2.7µH

The Coilcraft DO5022HC series provides a range of inductors in different values and low profile for large currents.
For L_1 choose: DO5022P-222HC (2.2µH,12A)
For L_2 choose: DO5022P-332HC (3.3µH,10A)

Power MOSFET Selection

The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{IN}).

The gate drive requirement is almost the same for both MOSFETs. Caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{COND} \text{ (Upper Switch)} = I^2_{LOAD} \times R_{DS(ON)} \times D \times \vartheta$$

$$P_{COND} \text{ (Lower Switch)} = I^2_{LOAD} \times R_{DS(ON)} \times (1 - D) \times \vartheta$$

ϑ = $R_{DS(ON)}$ Temperature Dependency

The total conduction loss is defined as:

$$P_{CON(TOTAL)} = P_{CON}\text{(Upper Switch)}\vartheta + P_{CON}\text{(Lower Switch)}\vartheta$$

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

Choose IRF7460 for control MOSFET and IRF7457 for synchronous MOSFET. These devices provide low on-resistance in a compact SOIC 8-Pin package.

The MOSFETs have the following data:

IRF7460	IRF7457
V_{DSS} = 20V	V_{DSS} = 20V
I_D = 10A @ 75°C	I_D = 12A @ 70°C
$R_{DS(ON)}$ = 10mΩ @ V_{GS}=10V	$R_{DS(ON)}$ = 7.5mΩ @ V_{GS}=10V
ϑ = 1.8 for 150°C (Junction Temperature)	ϑ = 1.5 for 150°C (Junction Temperature)

The total conduction losses for the master channel is:

$P_{CON(MASTER)}$ = 0.85W

The total conduction losses for the slave channel is:

$P_{CON(SLAVE)}$ = 0.77W

The control MOSFET contributes to the majority of the switching losses in synchronous Buck converter. The synchronous MOSFET turns on under zero-voltage condition, therefore the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \qquad ---(7)$$

Where:

$V_{DS(OFF)}$ = Drain to Source Voltage at off time

t_r = Rise Time

t_f = Fall Time

T = Switching Period

I_{LOAD} = Load Current

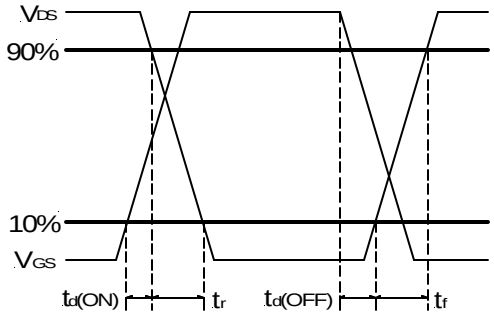


Figure 4 - Switching time waveforms.

From IRF7460 data sheet we obtain:

IRF7460

t_r = 6.9ns

t_f = 4.3ns

These values are taken under a certain condition test. For more detail please refer to the IRF7460 and IRF7457 data sheets.

By using equation (7), we can calculate the switching losses.

$P_{SW(MASTER)}$ = 44.8mW

$P_{SW(SLAVE)}$ = 107.5mW

Feedback Compensation

The control scheme for master and slave channels is based on voltage mode control, but the compensation of these two feedback loops is slightly different.

The Master channel sets the output voltage and its feedback loop should take care of double pole introduced by the output filter as a regular voltage mode control loop. The goal is to provide a close loop transfer function with the highest 0dB crossing frequency and adequate phase margin. The slave feedback loop acts slightly different and its goal is using the current information for current sharing.

The master feedback loop sees the output filter. The output LC filter introduces a double pole, -40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 5). The resonant frequency of the LC filter expressed as follows:

$$F_{LC(MASTER)} = \frac{1}{2\pi\sqrt{Lo \times Co}} \qquad ---(8)$$

Figure 5 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

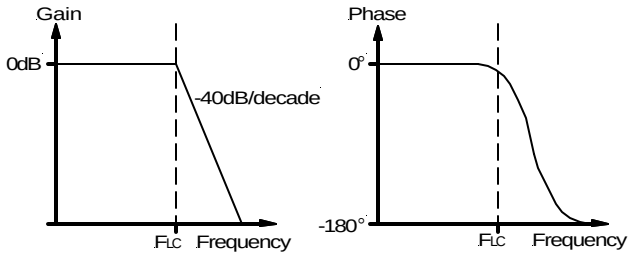


Figure 5 - Gain and phase of LC filter.

The master error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp1 pin to ground as shown in Figure 6.

The ESR zero of the LC filter expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \qquad ---(9)$$

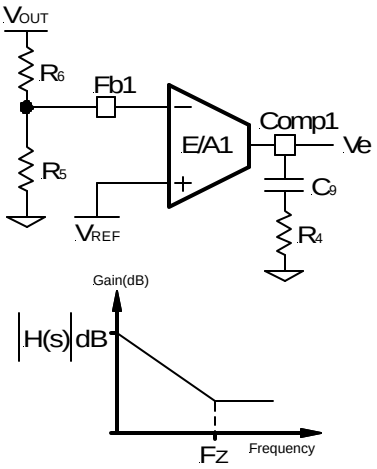


Figure 6 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / V_{OUT}) is given by:

$$H(s) = \left(g_m \times \frac{R_5}{R_6 + R_5} \right) \times \frac{1 + sR_4C_9}{sC_9} \qquad ---(10)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = g_m \times \frac{R_5}{R_6 \times R_5} \times R_4 \qquad ---(11)$$

$$F_Z = \frac{1}{2\pi \times R_4 \times C_9} \qquad ---(12)$$

The gain is determined by the voltage divider and E/A's transconductance gain.

First select the desired zero-crossover frequency (Fo):

$F_{O1} > F_{ESR}$ and $F_{O1} \leq (1/5 \sim 1/10) \times f_S$

Use the following equation to calculate R_4:

$$R_4 = \frac{V_{OSC}}{V_{IN(MASTER)}} \times \frac{F_{O1} \times F_{ESR}}{F_{LC}^2} \times \frac{R_5 + R_6}{R_5} \times \frac{1}{gm} \qquad ---(13)$$

Where:
$V_{IN(MASTER)}$ = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
F_{O1} = Crossover Frequency for the master E/A
F_{ESR} = Zero Frequency of the Output Capacitor
$F_{LC(MASTER)}$ = Resonant Frequency of Output Filter
gm = Error Amplifier Transconductor
R_5 and R_6 = Resistor Dividers for Output Voltage Programming

For:
$V_{IN(MASTER)}$ = 5V
V_{OSC} = 1.25V
F_{O1} = 30KHz
F_{ESR} = 25.26KHz
$F_{LC(MASTER)}$ = 3.57KHz
R_5 = 1K
R_6 = 200Ω
gm = 600μmho

This results to: R_4=29.7KΩ. Choose: R_4=29.4KΩ

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$F_Z \cong 75\% F_{LC(MASTER)}$

$$F_Z \cong 0.75 \times \frac{1}{2\pi \sqrt{L_O \times C_O}} \qquad ---(14)$$

For:
Lo = 2.2μH
Co = 900μF
Fz = 2.67KHz
R_4 = 24.9KΩ

Using equations (12) and (14) to calculate C_9, we get:

C_9 = 2003pF
Choose: C_9 = 2200pF

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to suppress the switching noise. The additional pole is given by:

$$F_P = \frac{1}{2\pi \times R_4 \times \frac{C_9 \times C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi \times R_4 \times f_S - \frac{1}{C_9}} \cong \frac{1}{\pi \times R_4 \times f_S}$$

For $F_P << \frac{f_S}{2}$

For a general solution for unconditionally stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 7.

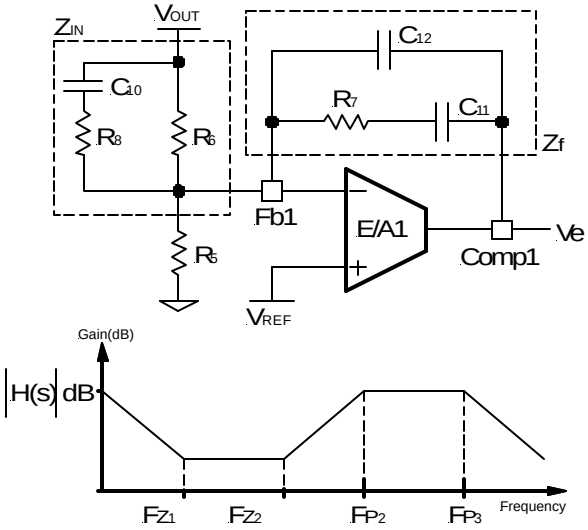


Figure 7 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m Z_f >> 1 \quad \text{and} \quad g_m Z_{IN} >> 1 \qquad \text{---(15)}$$

By replacing Z_{IN} and Z_f according to figure 7, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11}) \times [1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12}C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+sR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_{O1} = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \qquad \text{---(16)}$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Lo = Output Inductor
Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition (15) regarding transconductance error amplifier.

1) Select the crossover frequency:

   $Fo < F_{ESR}$ and $Fo \leq (1/10 \sim 1/6) \times f_S$

2) Select R_7, so that $R_7 >> \frac{2}{g_m}$

3) Place first zero before LC's resonant frequency pole.

   $F_{Z1} \cong 75\% F_{LC}$

   $$C_{11} = \frac{1}{2\pi \times F_{Z1} \times R_7}$$

4) Place third pole at the half of the switching frequency.

$$F_{P3} = \frac{f_S}{2}$$

$$C_{12} = \frac{1}{2\pi \times R_7 \times F_{P3}}$$

$C_{12} > 50pF$
If not, change R_7 selection.

5) Place R_7 in (16) and calculate C_{10}:

$$C_{10} \leq \frac{2\pi \times Lo \times F_O \times Co}{R_7} \times \frac{V_{OSC}}{V_{IN}}$$

6) Place second pole at ESR zero.
$F_{P2} = F_{ESR}$

$$R_8 = \frac{1}{2\pi \times C10 \times F_{P2}}$$

Check if $R_8 > \frac{1}{gm}$

If R_8 is too small, increase R_7 and start from step 2.

7) Place second zero around the resonant frequency.
$F_{Z2} = F_{LC}$

$$R_6 = \frac{1}{2\pi \times C10 \times F_{Z2}} - R_8$$

8) Use equation (1) to calculate R_5:

$$R_5 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_6$$

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

The slave error amplifier is a differential-input transconductance amplifier as well, the main goal for the slave feed back loop is to control the inductor current to match the masters inductor current as well provides highest bandwidth and adequate phase margin for overall stability.

The transfer function of power stage is expressed by:

$$G(s) = \frac{I_{L2}(s)}{Ve(s)} = \frac{V_{IN} - V_{OUT}}{sL_2 \times V_{OSC}} \quad ---(17)$$

Where:
V_{IN} = Input Voltage
V_{OUT} = Output Voltage
L_2 = Output Inductor
V_{OSC} = Oscillator Peak Voltage

As shown the transfer function is a function of inductor current.

The transfer function for the compensation network is given by equation (18), when using a series RC circuit as shown in Figure 8:

$$D(s) = \frac{Ve(s)}{R_{S2} \times I_{L2}(s)} = \left(g_m \times \frac{R_{S1}}{R_{S2}}\right) \times \left(\frac{1 + sC_2R_2}{sC_2}\right) \quad ---(18)$$

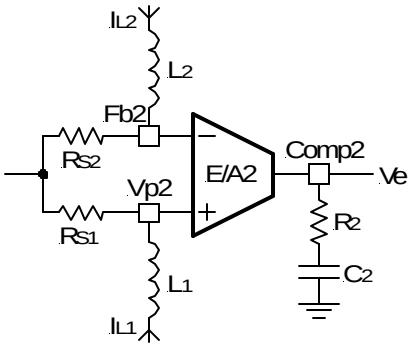


Figure 8 - The PI compensation network for slave channel.

The loop gain function is:

$H(s)=[G(s) \times D(s) \times R_{S2}]$

$$H(s)=R_{S2} \times \left(g_m \times \frac{R_{S1}}{R_{S2}}\right) \times \left(\frac{1+sR_2C_2}{sC_2}\right) \times \left(\frac{V_{IN}-V_{OUT}}{sL_2 \times V_{OSC}}\right)$$

Select a zero crossover frequency (F_{O2}) one-tenth of the switching frequency:

$$F_{O2} = \frac{f_S}{10}$$

F_{O2} = 20KHz

$$H(Fo) = g_m \times R_{S1} \times R_2 \times \frac{V_{IN} - V_{OUT}}{2\pi \times Fo \times L_2 \times V_{OSC}} = 1 \quad ---(19)$$

From (18), R_2 can be express as:

$$R_2 = \frac{1}{g_m \times R_{S1}} \times \frac{2\pi \times F_{O2} \times L_2 \times V_{OSC}}{V_{IN(SLAVE)} - V_{OUT}} \quad ---(20)$$

Set the zero of compensator to be half of $F_{LC(SLAVE)}$, the compensator capacitor, C_2, can be calculated as:

$$F_{LC(SLAVE)} = \frac{1}{2\pi \sqrt{L_2 \times C_{OUT}}}$$

$$Fz = \frac{F_{LC(SLAVE)}}{2}$$

$$C_2 = \frac{1}{2\pi \times R_2 \times Fz} \quad ---(21)$$

Using equations (20) and (21) we get the following values for R_2 and C_2.

R_2=16.45K; Choose: R_2=16.5K

C_2=6606pF; Choose: C_2=6800pF

LDO Section

Output Voltage Programming

Output voltage for LDO is programmed by reference voltage and external voltage divider. The Fb3 pin is the inverting input of the error amplifier, which is internally referenced to 1.25V. The divider is ratioed to provide 1.25V at the Fb3 pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT2} = V_{REF} \times \left(1 + \frac{R_7}{R_{10}}\right)$$

For:
V_{OUT2} = 2.5V
V_{REF} = 1.25V
R_{10} = 1KΩ

Results to R_7=1KΩ

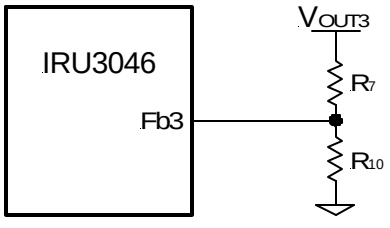


Figure 9 - Programming the output voltage for LDO.

LDO Power MOSFET Selection

The first step in selecting the power MOSFET for the linear regulator is to select the maximum $R_{DS(ON)}$ based on the input to the dropout voltage and the maximum load current.

$$R_{DS(ON)} = \frac{V_{IN3} - V_{OUT2}}{I_{OUT2}}$$

For:
V_{IN3} = 3.3V
V_{OUT2} = 2.5V
I_{OUT2} = 2A

Results to: $R_{DS(ON)(MAX)} = 0.4\Omega$

Note that since the MOSFET $R_{DS(ON)}$ increases with temperature, this number must be divided by ~1.5 in order to find the $R_{DS(ON)(MAX)}$ at room temperature. The IRLR2703 has a maximum of 0.065Ω $R_{DS(ON)}$ at room temperature, which meets our requirements.

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

TYPICAL APPLICATION

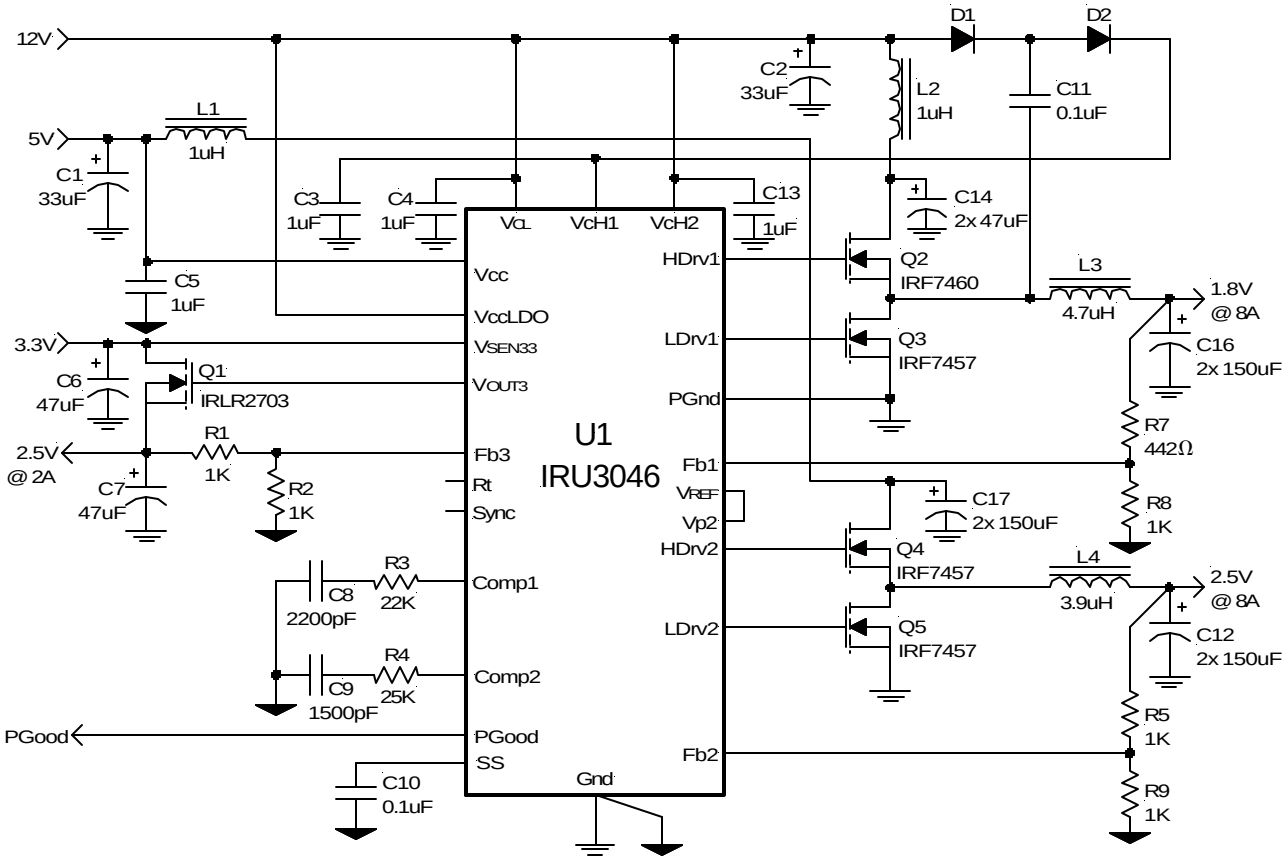


Figure 10 - Typical application for IRU3046 configured as two independent controllers.

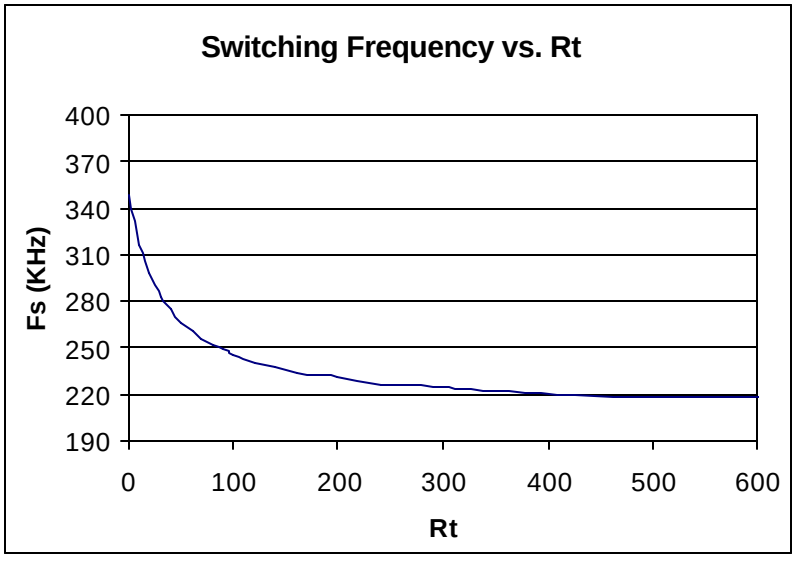


Figure 11 - Switching frequency per phase vs. Rt

TYPICAL APPLICATION

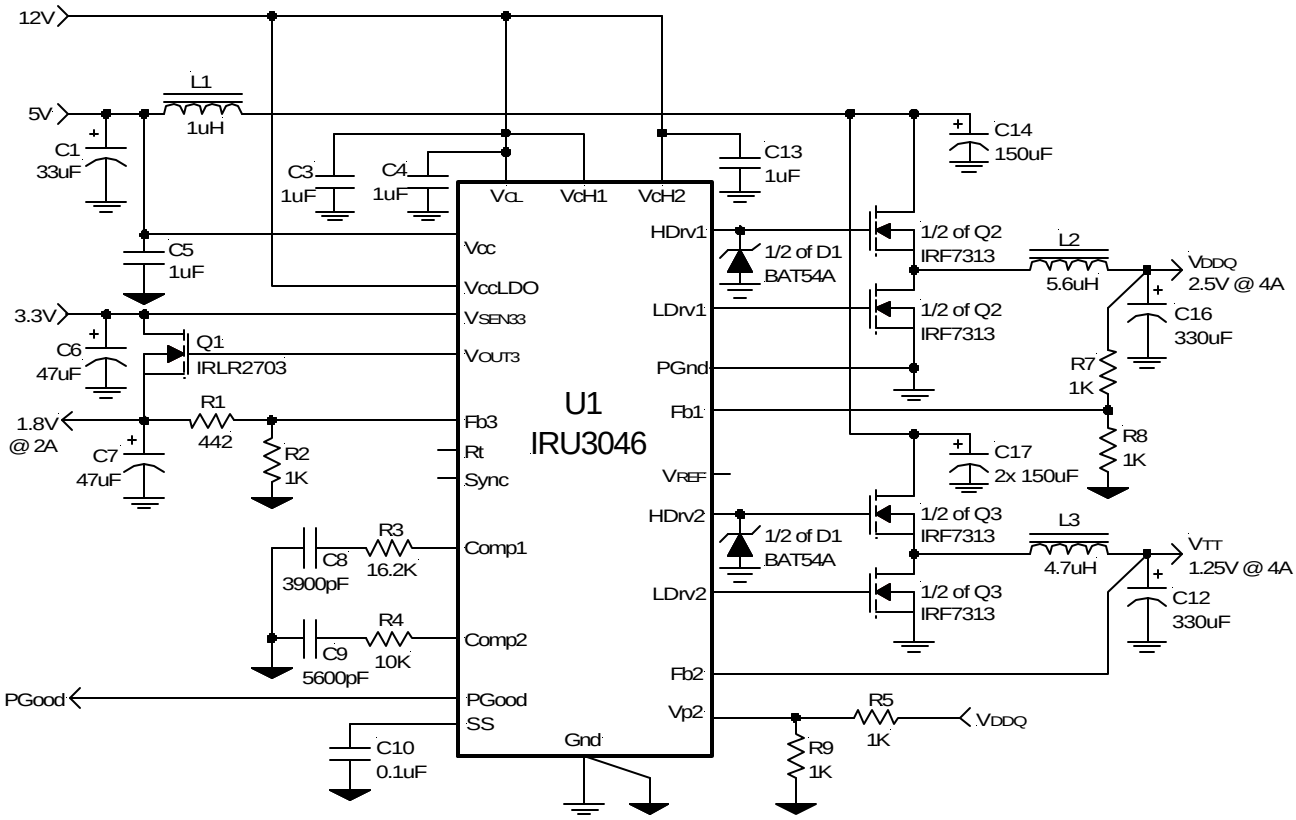


Figure 12 - Typical application for IRU3046 configured for DDR memory application.

DEMO-BOARD APPLICATION

Dual Input: 5V and 12V to 1.5V @ 16A

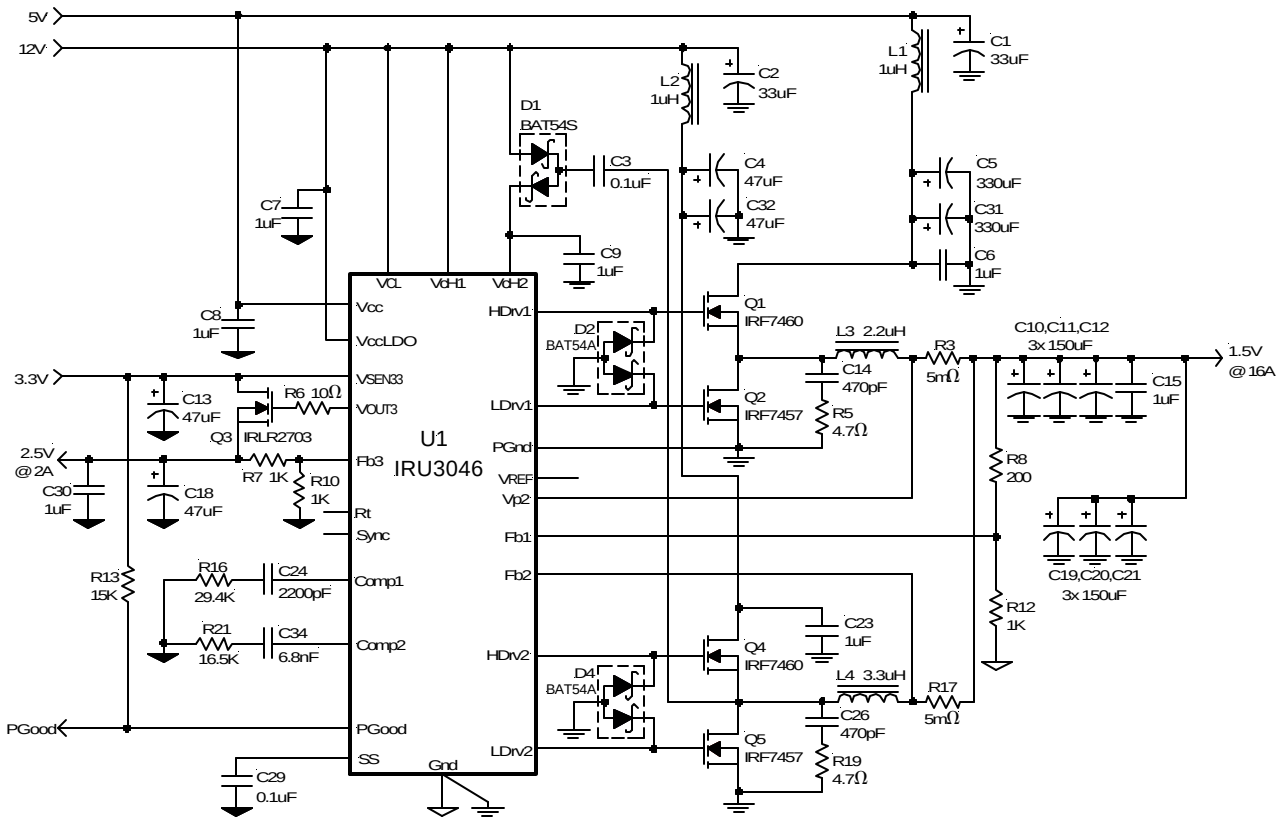


Figure 13 - Demo-board application of IRU3046.

DEMO-BOARD APPLICATION

Application Parts List

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1,Q4	MOSFET	20V, 10mΩ, 12A	2	IRF7460	IR	irf.com
Q2,Q5	MOSFET	20V, 7mΩ, 15A	2	IRF7457	IR	
Q3	MOSFET	30V, 0.045Ω, 23A	1	IRLR2703	IR	
U1	Controller	Synchronous PWM	1	IRU3046	IR	
D1	Diode	Fast Switching	1	BAT54S	IR	
D2,D4	Diode	Fast Switching	2	BAT54A or 1N4148	IR Any	
L1,L2	Inductor	1μH, 6.8A	2	D03316P-102	Coilcraft	coilcraft.com
L3	Inductor	2.2μH, 12A	1	D05022P-222HC	Coilcraft	
L4	Inductor	3.3μH, 10A	1	D05022P-332HC	Coilcraft	
C1,C2	Cap, Tantalum	33μF, 16V	2	ECS-T1CD336R	Panasonic	maco.panasonic.co.jp
C4,C32	Cap, Poscap	47μF, 16V	2	16TPB47M	Sanyo	sanyo.com/industrial
C5,C31	Cap, Poscap	330μF, 6.3V	2	6TPB330M	Sanyo	
C10,11,12, 19,20,21	Cap, Poscap	150μF, 6.3V, 40mΩ	6	6TPC150M	Sanyo	
C3,C29	Cap, Ceramic	0.1μF, Y5V, 25V	2	ECJ-2VF1E104Z	Panasonic	maco.panasonic.co.jp
C9	Cap, Ceramic	1μF, X7R, 25V	1	ECJ-3YB1E105K	Panasonic	
C24	Cap, Ceramic	2200pF, X7R, 50V	1	ECJ-2VB1H222K	Panasonic	
C34	Cap, Ceramic	6800pF, X7R, 50V	1	ECJ-2VB1H682K	Panasonic	
C14,C26	Cap, Ceramic	470pF, X7R, 50V	2	ECJ-2VC1H471J	Panasonic	
C6,7,8, 15,23,30	Cap, Ceramic	1μF, Y5V, 16V	6	ECJ-2VF1C105Z	Panasonic	
C13,C18	Cap, Tantalum	47μF, 10V	2	ECS-T1AD476R	Panasonic	
R2,4,15,18	Resistor	2.15Ω	4			
R16	Resistor	29.4K	1			
R21	Resistor	16.5K	1			
R5,R19	Resistor	4.7Ω	2			
R8	Resistor	200, 1%	1			
R7,10,12	Resistor	1K, 1%	3			
R3,R17	Resistor	5mΩ, 1W, 1%	2	ERJ-M1WSF5MOU	Panasonic	
R13	Resistor	15K	1			
R6	Resistor	10Ω	1			

WAVEFORMS

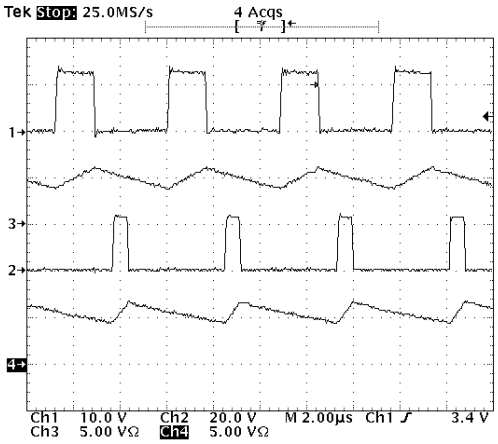


Figure 14 - Gate signals vs. inductor currents.

Ch1: Gate signal for control FET(master) (10V/div).
Ch2: Gate signal for control FET(slave) (20V/div).
Ch3: Inductor current for master channel (5A/div).
Ch4: Inductor current for slave channel (5A/div).
V_{MASTER}=5V, V_{SLAVE}=12V, I_{OUT}=10A

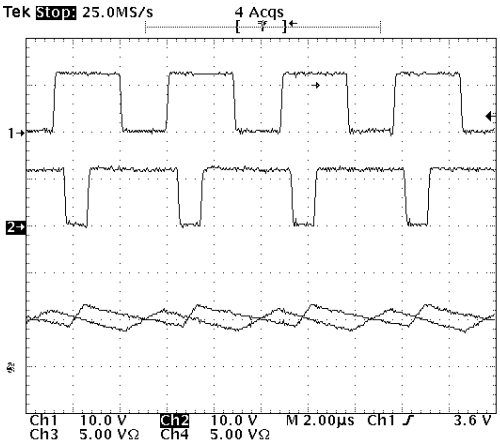


Figure 15 - Inductors current matching.

Ch1: Gate signal for sync FET(master) (10V/div).
Ch2: Gate signal for sync FET(slave) (10V/div).
Ch3: Inductor current for master channel (5A/div).
Ch4: Inductor current for slave channel (5A/div).
V_{MASTER}=5V, V_{SLAVE}=12V, I_{OUT}=10A

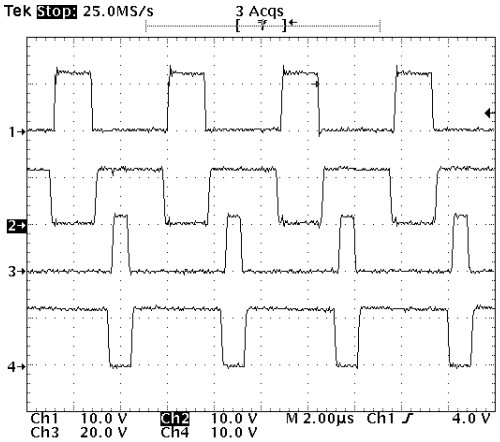


Figure 16 - Gate signals.

Ch1: Gate signal for control FET(master) (10V/div).
Ch2: Gate signal for sync FET(master) (10V/div).
Ch3: Gate signal for control FET(slave) (20V/div).
Ch4: Gate signal for sync FET(slave) (10V/div).

WAVEFORMS

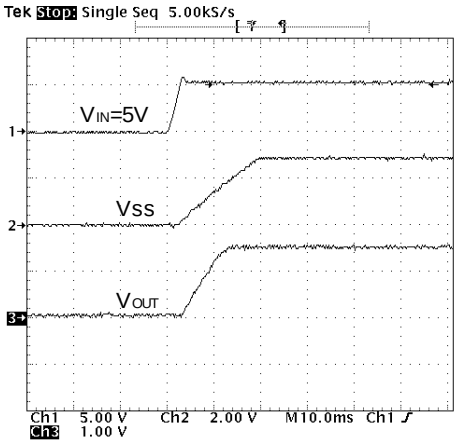


Figure 17 - Start-up @ I_{OUT} = 10A.

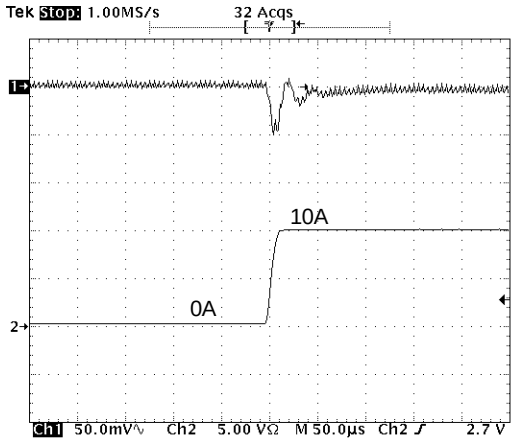


Figure 18 - Transient response @ I_{OUT} = 0 to 10A.

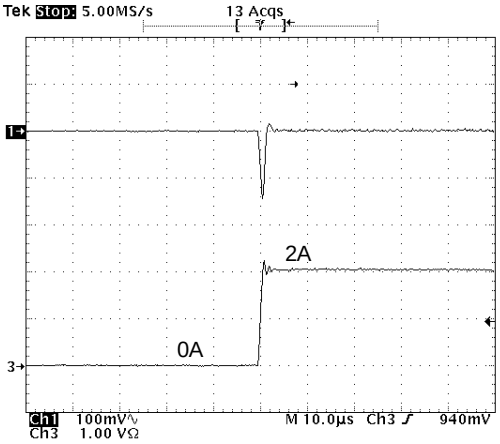


Figure 19 - Transient response for LDO @ I_{OUT} = 0 to 2A.

International
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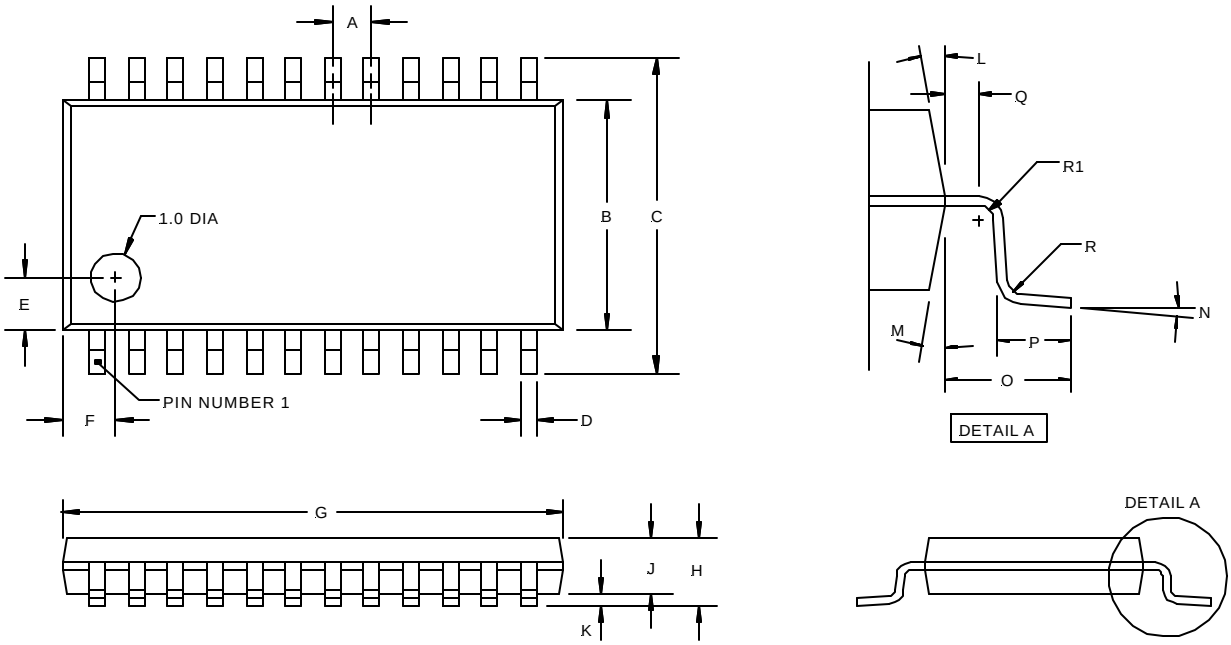
(F) TSSOP Package
24-Pin

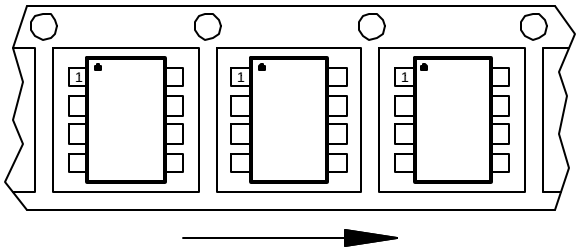


SYMBOL DESIG	24-PIN		
	MIN	NOM	MAX
A		0.65 BSC	
B	4.30	4.40	4.50
C		6.40 BSC	
D	0.19	---	0.30
E		1.00	
F		1.00	
G	7.70	7.80	7.90
H	---	---	1.10
J	0.85	0.90	0.95
K	0.05	---	0.15
L		12° REF	
M		12° REF	
N	0°	---	8°
O		1.00 REF	
P	0.50	0.60	0.75
Q		0.20	
R	0.09	---	---
R1	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
F	TSSOP Plastic	24	74	2500	Fig A



Feed Direction
Figure A

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IRU3047

DUAL SYNCHRONOUS PWM CONTROLLER WITH CURRENT SHARING CIRCUITRY AND LDO CONTROLLER

PRELIMINARY DATA SHEET

FEATURES

- Dual Synchronous Controller in 20-Pin Package with 180° out-of-phase operation
- LDO Controller with 40mA drive
- Can be configured as 2-Independent or 2-Phase PWM Controller
- Programmable Current Sharing in 2-Phase Configuration
- Flexible, Same or Separate Supply Operation
- Operation from 4V to 25V Input
- Internal 200KHz Oscillator per phase
- Soft-Start controls all outputs
- Fixed Frequency Voltage Mode
- 500mA Peak Output Drive Capability
- Short Circuit Protection for All Outputs
- Power Good Output

DESCRIPTION

The IRU3047 IC combines a Dual synchronous Buck controller and a linear regulator controller, providing a cost-effective, high performance and flexible solution for multi-output applications. The Dual synchronous controller can be configured as 2-independent or 2-phase controller. In 2-phase configuration, the IRU3047 provides a programmable current sharing which is ideal when the output power exceeds any single input power budget. IRU3047 provides a separate adjustable output by driving a switch as a linear regulator. This device features an internal 200KHz oscillator, under-voltage lockout for all input supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

APPLICATIONS

- Dual-Phase Power Supply
- DDR Memory Source Sink Vtt Application
- Graphic Card
- Hard Disk Drive
- Power supplies requiring multiple outputs

TYPICAL APPLICATION

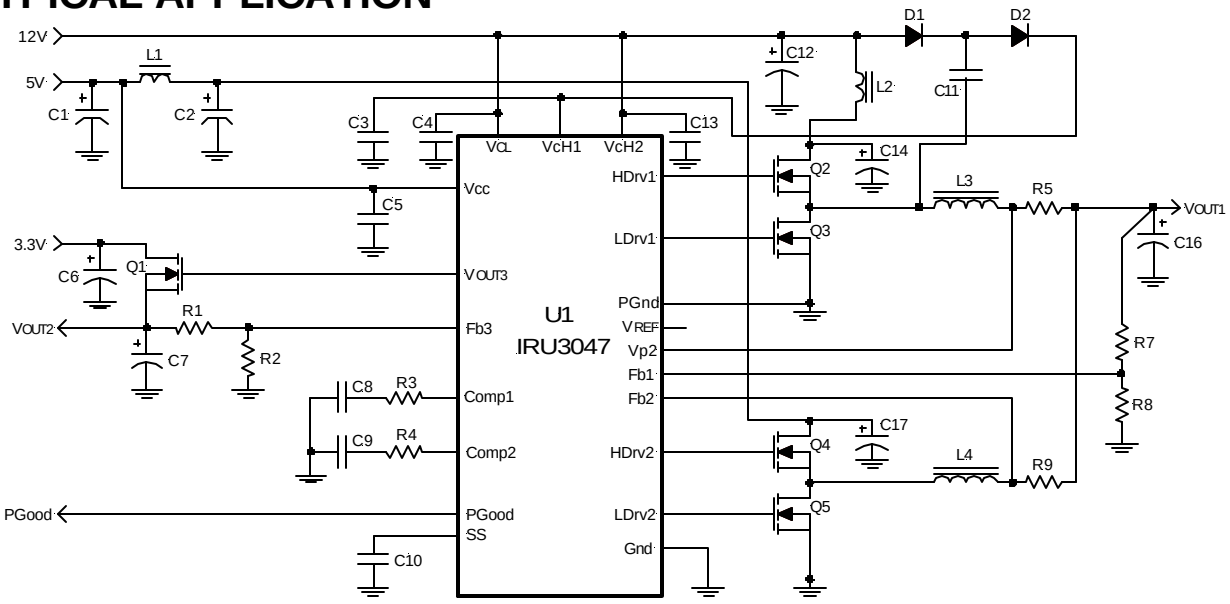


Figure 1 - Typical application of IRU3047 configured as 2-phase converter.

PACKAGE ORDER INFORMATION

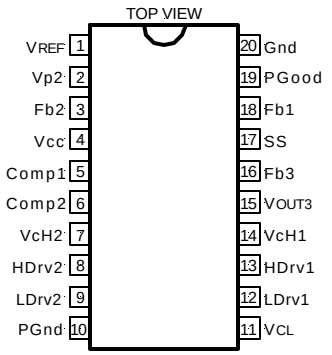
T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3047CW	20-Pin Plastic SOIC (W)

ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage 25V
V_{CH1}, V_{CH2} and V_{CL} Supply Voltage ..... 30V (not rated for inductive load)
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

20-PIN PLASTIC SOIC WB (W)



θ_{JA}=75°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=5V, VcH1=VcH2=V_{CL}=12V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage Section						
Fb Voltage	V_{FB}		1.225	1.250	1.275	V
Fb Voltage Line Regulation	L_{REG}	5<Vcc<12		0.2		%
UVLO Section						
UVLO Threshold - Vcc	$UVLO_{VCC}$	Supply Ramping Up		4.2		V
UVLO Hysteresis - Vcc				0.25		V
UVLO Threshold - VccLDO	$UVLO_{VCCLDO}$	Supply Ramping Up		4.2		V
UVLO Hysteresis - VccLDO				0.25		V
UVLO Threshold - VcH1	$UVLO_{VCH1}$	Supply Ramping Up		3.5		V
UVLO Hysteresis - VcH1				0.2		V
UVLO Threshold - VcH2	$UVLO_{VCH2}$	Supply Ramping Up		3.5		V
UVLO Hysteresis - VcH2				0.2		V
UVLO Threshold - Fb	$UVLO_{Fb}$	Fb Ramping Down		0.6		V
UVLO Hysteresis - Fb				0.1		V
Supply Current Section						
Vcc Dynamic Supply Current	Dyn I_{CC}	Freq=200KHz, C_L=1500pF		5		mA
VcH1 Dynamic Supply Current	Dyn I_{CH1}	Freq=200KHz, C_L=1500pF		7		mA
VcH2 Dynamic Supply Current	Dyn I_{CH2}	Freq=200KHz, C_L=1500pF		7		mA
Vcc Static Supply Current	I_{CCQ}	SS=0V		3.5		mA
VcH1 Static Supply Current	I_{CH1Q}	SS=0V		2		mA
VcH2 Static Supply Current	I_{CH2Q}	SS=0V		2		mA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Soft-Start Section						
Charge Current	SS_{IB}	SS=0V	15	25	30	µA
Power Good Section						
Fb1 Lower Trip Point	PG_{FB1L}	Fb1 Ramping Down		$0.9V_{REF}$		V
Fb1 Upper Trip Point	PG_{FB1H}	Fb1 Ramping Up		$1.1V_{REF}$		V
Fb2 Lower Trip Point	PG_{FB2L}	Fb2 Ramping Down		$0.9V_{REF}$		V
Fb2 Upper Trip Point	PG_{FB2H}	Fb2 Ramping Up		$1.1V_{REF}$		V
Fb3 Lower Trip Point	PG_{FB3L}	Fb3 Ramping Down		$0.9V_{REF}$		V
Fb3 Upper Trip Point	PG_{FB3H}	Fb3 Ramping Up		$1.1V_{REF}$		V
Power Good Voltage OK	V_{PG}	5K resistor pulled up to 5V	4.5	4.8	5	V
Error Amp Section						
Fb Voltage Input Bias Current	I_{FB1}	SS=3V		-0.1		µA
Fb Voltage Input Bias Current	I_{FB2}	SS=0V		-64		µA
Transconductance 1	g_{m1}			400		µmho
Transconductance 2	g_{m2}			600		µmho
Input Offset Voltage for PWM2	$V_{OS(ERR)2}$	Fb2 to V_{P2}	-2	0	+2	mV
Oscillator Section						
Frequency	Freq	Rt=Open	180	200	220	KHz
Ramp Amplitude	V_{RAMP}			1.25		V
Output Drivers Section						
Rise Time	Tr	C_L=1500pF		35	100	ns
Fall Time	Tf	C_L=1500pF		50	100	ns
Dead Band Time	T_{DB}		50	150	250	ns
Max Duty Cycle	T_{ON}	Fb=1V, Freq=200KHz	85	90		%
Min Duty Cycle	T_{OFF}	Fb=1.5V	0	0		%
LDO Controller Section						
Drive Current	I_{LDO}		30	45		mA
Fb Voltage	V_{FB}LDO		1.225	1.25	1.275	V
Input Bias Current	$I_{LDO(BIAS)}$			0.5	2	µA

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	V_{REF}	Reference Voltage.
2	Vp2	Non-inverting input to the second error amplifier, in the current sharing mode it is connected to the programming resistor. In independent two channel mode it is connected to the reference voltage (Pin1) when Fb2 is connected to the resistor divider to set the output voltage.
3,18	Fb2, Fb1	Inverting inputs to the error amplifiers, in current sharing mode Fb1 is connected to a resistor divider to set the output voltage and Fb2 is connected to programming resistor to achieve current sharing. In independent two channel mode, these pins work as feedback inputs for each channel.
4	Vcc	Supply voltage for the internal blocks of the IC.
5,6	Comp1, Comp2	Compensation pins for the error amplifiers.
7,14	VcH2, VcH1	Supply voltage for the high side output drivers. These are connected to voltages that must be at least 4V higher than their bus voltages (assuming 5V threshold MOSFET). A minimum of 1µF high frequency capacitor must be connected from these pins to PGnd pin to provide peak drive current capability.
8,13	HDrv2, HDrv1	Output driver for high side power MOSFET. Connect a diode, such as BAT54 or 1N4148, from these pins to ground for the application when the inductor current goes negative (Source/Sink), soft-start at no load and for fast load transient from full load to no load.

PIN#	PIN SYMBOL	PIN DESCRIPTION
9,12	LDrv2, LDrv1	Output driver for the synchronous power MOSFET.
10	PGnd	This pin serves as the separate ground for MOSFET's driver and should be connected to the system's ground plane.
11	V_{CL}	Supply voltage for the low side output drivers.
15	V_{OUT3}	Driver signal for the LDO's external transistor.
16	Fb3	LDO's feedback pin, connected to a resistor divider to set the output voltage of LDO.
17	SS	Soft-Start pin. The converter can be shutdown by pulling this pin below 0.5V.
19	PGood	Power Good pin. This pin is a collector output that switches Low when any of the outputs are outside of the specified under voltage trip point.
20	Gnd	Ground pin.

BLOCK DIAGRAM

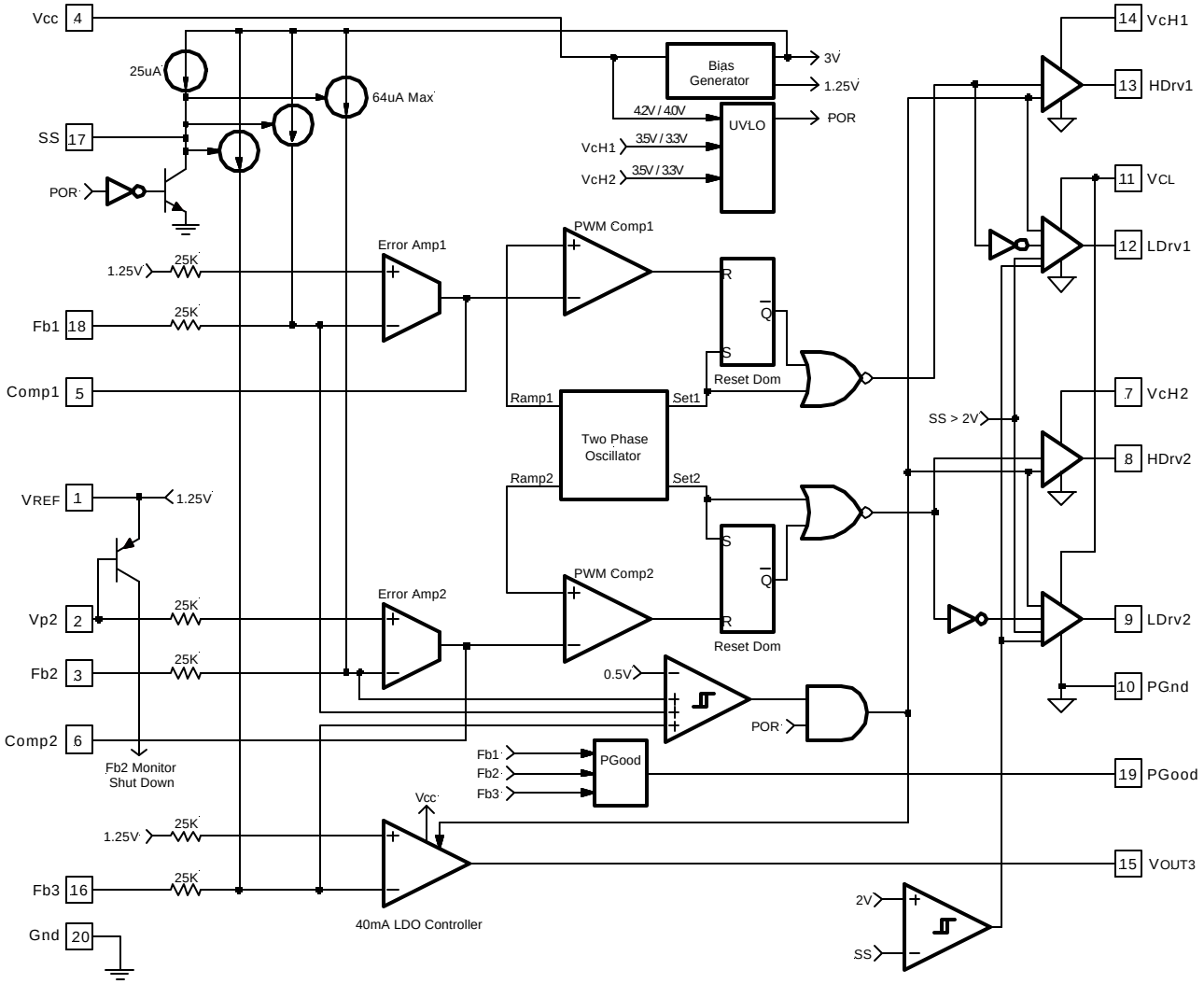


Figure 2 - Block diagram of the IRU3047.

THEORY OF OPERATION

Introduction
The IRU3047 is designed for multi-outputs applications. It includes two synchronous buck controllers and a linear regulator controller. The two synchronous controller operates with fixed frequency voltage mode and can be configured as two independent controller or 2-phase controller with current sharing. The timing of the IC is provided through an internal oscillator circuit. These are two out of phase oscillators with 200KHz switching frequency.

Independent Mode
In this mode the IRU3047 provides two independent outputs with either common or different input voltages. The output voltage of the individual channel is set and controlled by the output of the error amplifier, this is the amplified error signal from the sensed output voltage and the reference voltage. This voltage is compared to the ramp signal and generates fixed frequency pulses of variable duty-cycle, which drives the two N-channel external MOSFETs.

Current Sharing Mode
In the current sharing mode, the two converter's outputs tied together and provide one single output (see Figure 1). In this mode, one control loop acts as a master and sets the output voltage as a regular Voltage Mode buck controller and the other control loop acts as a slave and monitors the current information for current sharing. The current sharing is programmable and sets by using two external resistors in output currents' path. The slave's error amplifier, error amplifier 2 (see the block diagram) measures the voltage drops across the current sense resistors, the differential of these signals is amplified and compared with the ramp signal and generate the fixed frequency pulses of variable duty cycle to match the output currents.

Out of Phase Operation
The IRU3047 drives its two output stages 180^{o} out of phase. In 2-phase configuration, the two inductor ripple currents cancel each other and result to a reduction of the output current ripple and contributes to a smaller output capacitors for the same ripple voltage requirement.

In application with single input voltage, the 2-phase configuration reduces the input ripple current. This results in much smaller RMS current in the input capacitor and reduction of input capacitor.

Soft-Start
The IRU3047 has a programmable soft start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vcc, VcH1 and VcH2 rise above their threshold and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter. As the charging voltage of the external capacitor ramps up, the PWM signals increase from zero to the point the feedback loop takes control.

Shutdown
The converter can be shutdown by pulling the soft-start pin below 0.5V. This can be easily done by using an external small signal transistor. During shutdown the MOSFET drivers and the LDO controller turn off.

Power Good
The IRU3047 provides a power good signal. This is an open collector output and it is pulled low if the output voltages are not within the specified threshold. This pin can be left floating if not used.

Short-Circuit Protection
The outputs are protected against the short circuit. The IRU3047 protects the circuit for shorted output by sensing the output voltages. The IRU3047 shuts down the PWM signals and LDO controller, when the output voltages drops below the set values.

Under-Voltage Lockout
The under-voltage lockout circuit assures that the MOSFET driver outputs and LDO controller remain in the off state whenever the supply voltages drop below set parameters. Normal operation resumes once the supply voltages rise above the set values.

APPLICATION INFORMATION

Design Example:
The following example is a typical application for IRU3047 in current sharing mode. The schematic is Figure 12 on page 16.

$V_{IN1(MASTER)}$ = 12V
$V_{IN2(SLAVE)}$ = 5V
V_{OUT1} = 1.5V
I_{OUT} = 12A
ΔV_{OUT} = 75mV
f_S = 200KHz

PWM Section

Output Voltage Programming
Output voltage is programmed by reference voltage and external voltage divider. The Fb1 pin is the inverting input of the error amplifier, which is internally referenced to 1.25V. The divider is ratioed to provide 1.25V at the Fb1 pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT1} = V_{REF} \times \left(1+\frac{R_6}{R_5}\right) \qquad ---(1)$$

When an external resistor divider is connected to the output as shown in Figure 3.

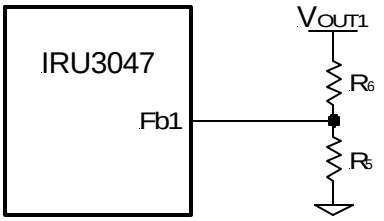


Figure 3 - Typical application of the IRU3047 for programming the output voltage.

Equation (1) can be rewritten as:

$$R_6 = R_5 \times \left(\frac{V_{OUT1}}{V_{REF}} - 1\right)$$

Will result to:
V_{OUT1} = 2.5V
V_{REF} = 1.25V
R_5 = 1K
R_6 = 1K

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-Start Programming
The soft-start timing can be programmed by selecting the soft start capacitance value. The start up time of the converter can be calculated by using:

$$t_{START} = 75 \times Css \quad (ms) \qquad ---(2)$$

Where:
C_{SS} is the soft-start capacitor (μF)

For a start-up time of 75ms, the soft-start capacitor will be 1μF. Choose a ceramic capacitor at 1μF.

Boost Supply Vc
To drive the high-side switch it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 1. The capacitor is charged up to approximately twice the bus voltage. A capacitor in the range of 0.1μF to 1μF is generally adequate for most applications.

Sense Resistor Selection
These resistors will determine the current sharing between two channels. The relationship between the Master and Slave output currents is expressed by:

$$R_{SEN1} \times I_{MASTER} = R_{SEN2} \times I_{SLAVE} \qquad ---(3)$$

For an equal current sharing, R_{SEN1}=R_{SEN1}
Choose R_{SEN1}=R_{SEN2}=5mΩ

Input Capacitor selection
The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of control MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_{OUT} \sqrt{D \times (1-D)} \qquad ---(4)$$

Where:
D is the Duty Cycle, simply D=V_{OUT}/V_{IN}.
I_{RMS} is the RMS value of the input capacitor current.
I_{OUT} is the output current for each channel.

For V_{IN1}=12V, I_{OUT1}=6A and D1=0.208
Results to: I_{RMS1}=2.43A

And for V_{IN2}=5V, I_{OUT2}=6A and D2=0.5
Results to: I_{RMS2}=3A

For higher efficiency, a low ESR capacitor is recommended.

For V_{IN1}=12V, choose two Poscap from Sanyo 16TPB47M (16V, 47µF, 70mΩ, 1.4A)

For V_{IN2}=5V, choose two 6TPB330M (6.3V, 330µF, 40mΩ, 3A).

Output Capacitor Selection

The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$ESR \le \frac{\Delta V_O}{\Delta I_O} \qquad ---(5)$$

Where:
ΔV_O = Output Voltage Ripple
ΔI_O = Output Current
ΔV_O=100mV and ΔI_O=5A, results to ESR=20mΩ

The Sanyo TPC series, PosCap capacitor is a good choice. The 6TPB470M 470µF, 6.3V has an ESR 40mΩ. Selecting two of these capacitors in parallel, results to an ESR of ≅ 20mΩ which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

The resulting output ripple current is smaller then each channel ripple current due to the 180° phase shift. These currents cancel each other. The cancellation is not the maximum because of the different duty cycle for each channel.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi); the optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \; ; \; \Delta t = D \times \frac{1}{f_S} \; ; \; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \qquad ---(6)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OUT} = Output Voltage
Δi = Inductor Ripple Current
f_S = Switching Frequency
Δt = Turn On Time
D = Duty Cycle

For Δi_1=30% of I_1, we get L_3=5.46µH
For Δi_2=30% of I_2, we get: L_4=3.47µH

The Coilcraft DO5022HC series provides a range of inductors in different values and low profile for large currents.
For L_3 choose DO5022P-602HC (6µH, 7.5A)
For L_4 choose DO5022P-472HC (4.7µH, 8.4A)

Power MOSFET Selection

The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{IN}).

The gate drive requirement is almost the same for both MOSFETs. Caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{COND}(\text{Upper Switch}) = I^2_{LOAD} \times R_{DS(ON)} \times D \times \vartheta$$

$$P_{COND}(\text{Lower Switch}) = I^2_{LOAD} \times R_{DS(ON)} \times (1 - D) \times \vartheta$$

ϑ = $R_{DS(ON)}$ Temperature Dependency

The total conduction loss is defined as:

$$P_{CON(TOTAL)} = P_{CON}(\text{Upper Switch})\vartheta + P_{CON}(\text{Lower Switch})\vartheta$$

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

Choose IRF7811A for control MOSFET and IRF7809A for synchronous MOSFET. These devices provide low on-resistance in a compact SOIC 8-Pin package.

The MOSFETs have the following data:

IRF7811A	IRF7809A
V_{DSS} = 28V	V_{DSS} = 20V
I_D = 11.2A @ 90°C	I_D = 14.2A @ 90°C
$R_{DS(ON)}$ = 12mΩ @	$R_{DS(ON)}$ = 8.5mΩ @
V_{GS} = 4.5V	V_{GS} = 4.5V

For both: ϑ = 1.5 for 150°C
(Junction Temperature)

The total conduction losses for the master channel is:

$P_{CON(MASTER)}$ = 0.498W

The total conduction losses for the slave channel is:

$P_{CON(SLAVE)}$ = 0.5535W

The control MOSFET contributes to the majority of the switching losses in synchronous Buck converter. The synchronous MOSFET turns on under zero-voltage condition, therefore the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \qquad ---(7)$$

Where:
$V_{DS(OFF)}$ = Drain to Source Voltage at off time
t_r = Rise Time
t_f = Fall Time
T = Switching Period
I_{LOAD} = Load Current

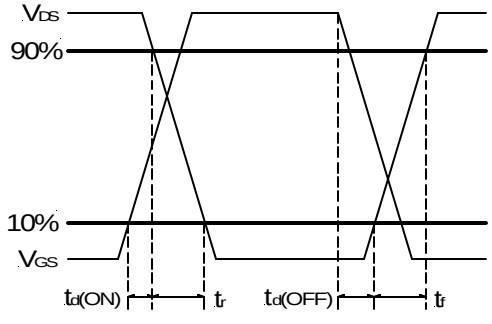


Figure 4 - Switching time waveforms.

From IRF7811A data sheet we obtain:

IRF7811A
t_r = 4ns
t_f = 8ns

These values are taken under a certain condition test. For more detail please refer to the IRF7811A and IRF7809A data sheets.

By using equation (7), we can calculate the switching losses.

$P_{SW(MASTER)}$ = 86.4mW
$P_{SW(SLAVE)}$ = 36mW

Feedback Compensation

The control scheme for master and slave channels is based on voltage mode control, but the compensation of these two feedback loops is slightly different.

The Master channel sets the output voltage and its feedback loop should take care of double pole introduced by the output filter as a regular voltage mode control loop. The goal is to provide a close loop transfer function with the highest 0dB crossing frequency and adequate phase margin. The slave feedback loop acts slightly different and its goal is using the current information for current sharing.

The master feedback loop sees the output filter. The output LC filter introduces a double pole, -40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 5). The Resonant frequency of the LC filter expressed as follows:

$$F_{LC(MASTER)} = \frac{1}{2\pi\sqrt{Lo \times Co}} \qquad ---(8)$$

Figure 5 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

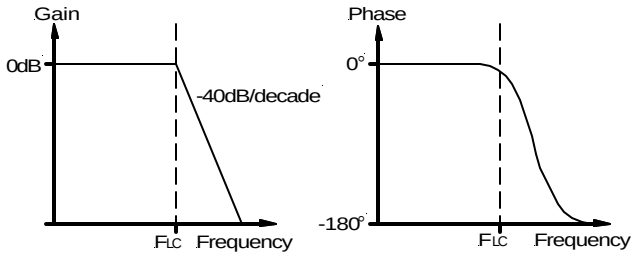


Figure 5 - Gain and phase of LC filter.

The master error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp1 pin to ground as shown in Figure 6.

The ESR zero of the LC filter expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \qquad ---(9)$$

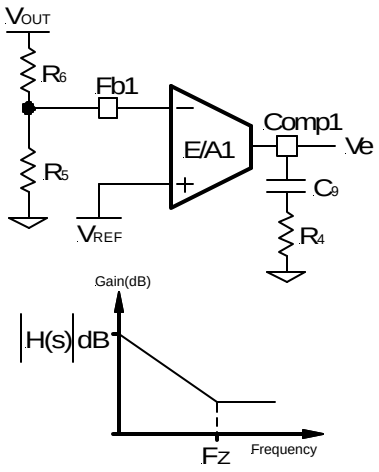


Figure 6 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / V_{OUT}) is given by:

$$H(s) = \left(g_m \times \frac{R_5}{R_6 + R_5}\right) \times \frac{1 + sR_4C_9}{sC_9} \qquad ---(10)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = g_m \times \frac{R_5}{R_6 \times R_5} \times R_4 \qquad ---(11)$$

$$F_Z = \frac{1}{2\pi \times R_4 \times C_9} \qquad ---(12)$$

The gain is determined by the voltage divider and E/A's transconductance gain.

First select the desired zero-crossover frequency (Fo):

$F_{O1} > F_{ESR}$ and $F_{O1} \leq (1/5 \sim 1/10) \times f_S$

Use the following equation to calculate R4:

$$R_4 = \frac{V_{OSC}}{V_{IN(MASTER)}} \times \frac{F_{O1} \times F_{ESR}}{F_{LC}^2} \times \frac{R_5 + R_6}{R_5} \times \frac{1}{g_m} \qquad ---(13)$$

Where:
$V_{IN(MASTER)}$ = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
F_{O1} = Crossover Frequency for the master E/A
F_{ESR} = Zero Frequency of the Output Capacitor
$F_{LC(MASTER)}$ = Resonant Frequency of Output Filter
g_m = Error Amplifier Transconductance
R_5 and R_6 = Resistor Dividers for Output Voltage Programming

For:
$V_{IN(MASTER)}$ = 12V
V_{OSC} = 1.25V
F_{O1} = 15KHz
F_{ESR} = 8.4KHz
$F_{LC(MASTER)}$ = 2.1KHz
$R_5 = R_6 = 1K\Omega$
g_m = 600µmho

This results to R_4=9.8KΩ. Choose R_4=10KΩ

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$F_Z \cong 75\% F_{LC(MASTER)}$

$$F_Z \cong 0.75 \times \frac{1}{2\pi\sqrt{L_O \times C_O}} \qquad ---(14)$$

For:
Lo = 6µH
Co = 940µF
Fz = 1.57KHz
$R_4 = 10K\Omega$

Using equations (12) and (14) to calculate C_9, we get:

C_9 = 10000pF
Choose C_9 = 10000pF

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to supress the switching noise. The additional pole is given by:

$$F_P = \frac{1}{2\pi \times R_4 \times \frac{C_9 \times C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi \times R_4 \times f_S - \frac{1}{C_9}} \cong \frac{1}{\pi \times R_4 \times f_S}$$

For $F_P << \frac{f_S}{2}$

For a general solution for unconditionally stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 7.

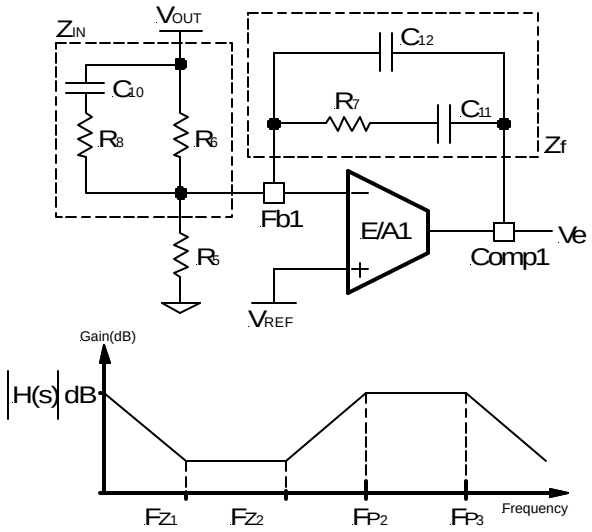


Figure 7 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m Z_f >> 1 \quad \text{and} \quad g_m Z_{IN} >> 1 \qquad \text{---(15)}$$

By replacing Z_{IN} and Z_f according to figure 7, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11}) \times [1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12}C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+sR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_{O1} = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \qquad \text{---(16)}$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Lo = Output Inductor
Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition (15) regarding transconductance error amplifier.

1) Select the crossover frequency:

   $Fo < F_{ESR}$ and $Fo \leq (1/10 \sim 1/6) \times f_S$

2) Select R_7, so that $R_7 >> \frac{2}{g_m}$

3) Place first zero before LC's resonant frequency pole.

   $F_{Z1} \cong 75\% F_{LC}$

   $$C_{11} = \frac{1}{2\pi \times F_{Z1} \times R_7}$$

4) Place third pole at the half of the switching frequency.

$$F_{P3} = \frac{f_S}{2}$$

$$C_{12} = \frac{1}{2\pi \times R_7 \times F_{P3}}$$

$C_{12} > 50pF$
If not, change R_7 selection.

5) Place R_7 in equation (16) and calculate C_{10}:

$$C_{10} \leq \frac{2\pi \times Lo \times F_O \times Co}{R_7} \times \frac{V_{OSC}}{V_{IN}}$$

6) Place second pole at ESR zero.
$F_{P2} = F_{ESR}$

$$R_8 = \frac{1}{2\pi \times C10 \times F_{P2}}$$

Check if $R_8 > \frac{1}{g_m}$

If R_8 is too small, increase R_7 and start from step 2.

7) Place second zero around the resonant frequency.
$F_{Z2} = F_{LC}$

$$R_6 = \frac{1}{2\pi \times C10 \times F_{Z2}} - R_8$$

8) Use equation (1) to calculate R_5:

$$R_5 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_6$$

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

The slave error amplifier is a differential-input transconductance amplifier as well, the main goal for the slave feed back loop is to control the inductor current to match the masters inductor current as well provides highest bandwidth and adequate phase margin for overall stability.

The transfer function of power stage is expressed by:

$$G(s) = \frac{I_{L2}(s)}{Ve(s)} = \frac{V_{IN} - V_{OUT}}{sL_2 \times V_{OSC}} \quad ---(17)$$

Where:
V_{IN} = Input Voltage
V_{OUT} = Output Voltage
L_2 = Output Inductor
V_{OSC} = Oscillator Peak Voltage

As shown the transfer function is a function of inductor current.

The transfer function for the compensation network is given by equation (18), when using a series RC circuit as shown in Figure 8.

$$D(s) = \frac{Ve(s)}{R_{S2} \times I_{L2}(s)} = \left(g_m \times \frac{R_{S1}}{R_{S2}}\right) \times \left(\frac{1 + sC_2R_2}{sC_2}\right) \quad ---(18)$$

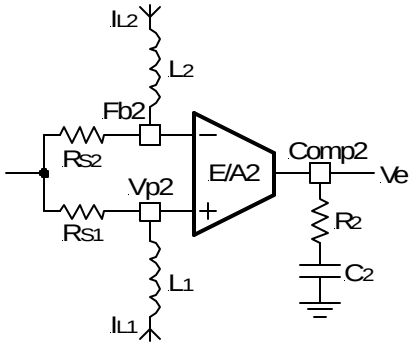


Figure 8 - The PI compensation network for slave channel.

The loop gain function is:

$$H(s) = [G(s) \times D(s) \times R_{S2}]$$

$$H(s) = R_{S2} \times \left(g_m \times \frac{R_{S1}}{R_{S2}}\right) \times \left(\frac{1 + sR_2C_2}{sC_2}\right) \times \left(\frac{V_{IN} - V_{OUT}}{sL_2 \times V_{OSC}}\right)$$

Select a zero crossover frequency (F_{O2}) one-tenth of the switching frequency:

$$F_{O2} = \frac{f_S}{10}$$

F_{O2} = 20KHz

$$H(Fo)=g_m \times R_{S1} \times R_2 \times \frac{V_{IN} - V_{OUT}}{2\pi \times Fo \times L_2 \times V_{OSC}} = 1 \quad ---(19)$$

From (19), R_2 can be express as:

$$R_2 = \frac{1}{g_m \times R_{S1}} \times \frac{2\pi \times F_{O2} \times L_2 \times V_{OSC}}{V_{IN(SLAVE)} - V_{OUT}} \quad ---(20)$$

Set the zero of compensator to be half of $F_{LC(SLAVE)}$, the compensator capacitor, C_2, can be calculated as:

$$F_{LC(SLAVE)} = \frac{1}{2\pi \sqrt{L_2 \times C_{OUT}}}$$

$$Fz = \frac{F_{LC(SLAVE)}}{2}$$

$$C_2 = \frac{1}{2\pi \times R_2 \times Fz} \quad ---(21)$$

Using equations (20) and (21) we get the following values for R_2 and C_2.

R_2 = 123K; Choose R_2= 130K

C_2 = 1023pF; Choose C_2= 1000pF

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

TYPICAL APPLICATION

Dual Input: 5V and 12V to 1.5V @ 16A
3.3V to 2.5V @ 2A

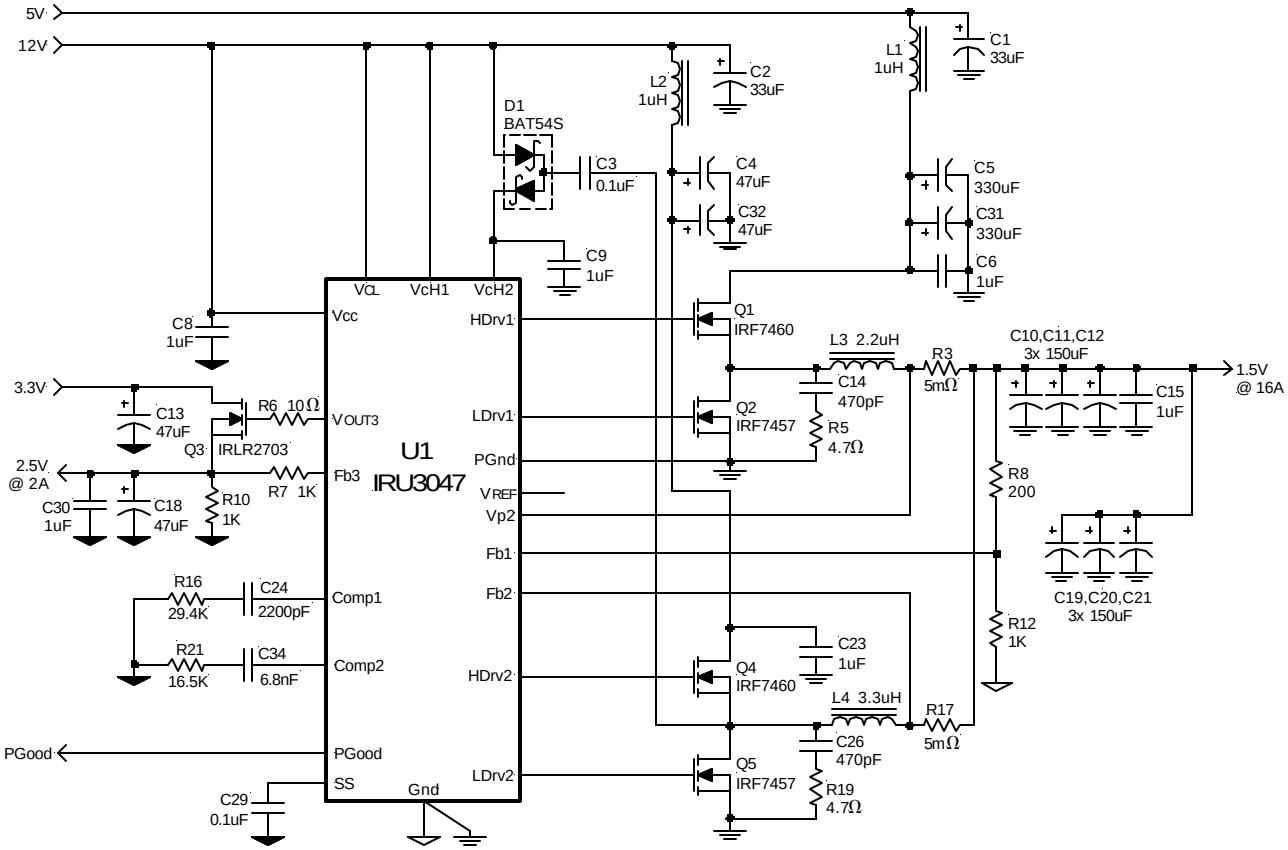


Figure 9 - Typical application of IRU3047, configured as a 2-phase converter in current sharing mode.

TYPICAL APPLICATION

12V to 1.8V @ 8A
5V to 2.5V @ 8A
3.3V to 2.5V @ 2A

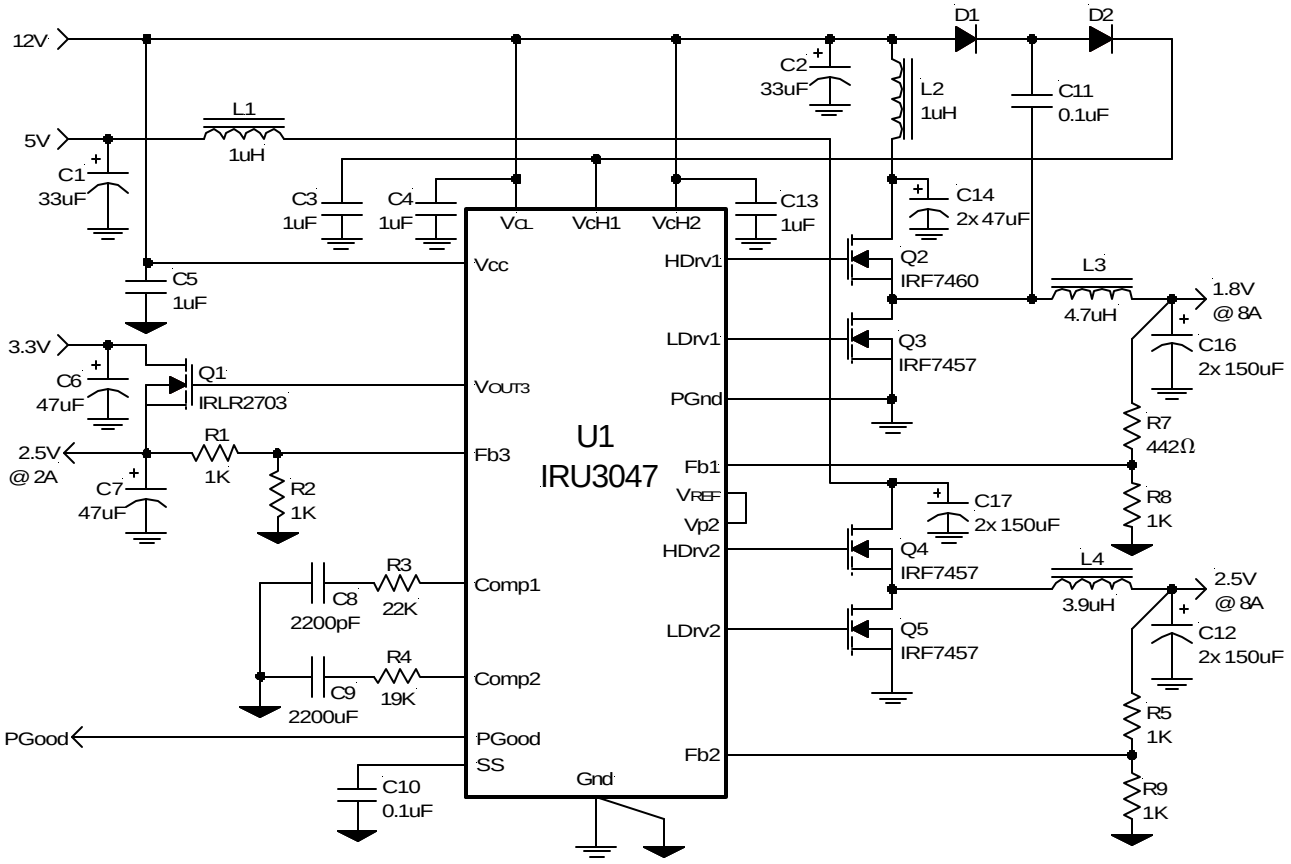


Figure 10 - Typical application for IRU3047 configured as two independent controllers.

TYPICAL APPLICATION

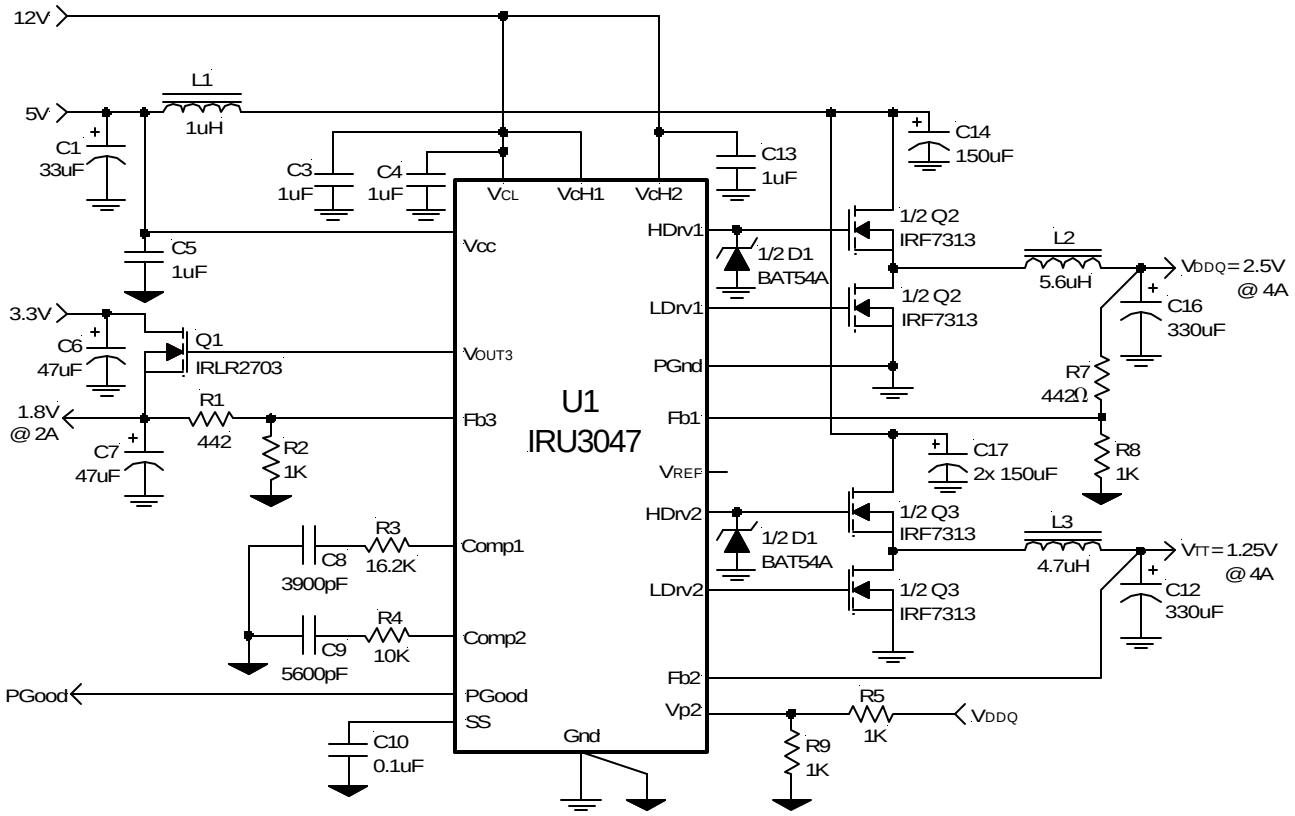


Figure 11 - Typical application for IRU3047 configured for DDR memory application.

DEMO-BOARD APPLICATION

Dual Input: 5V and 12V to 1.5V @ 12A

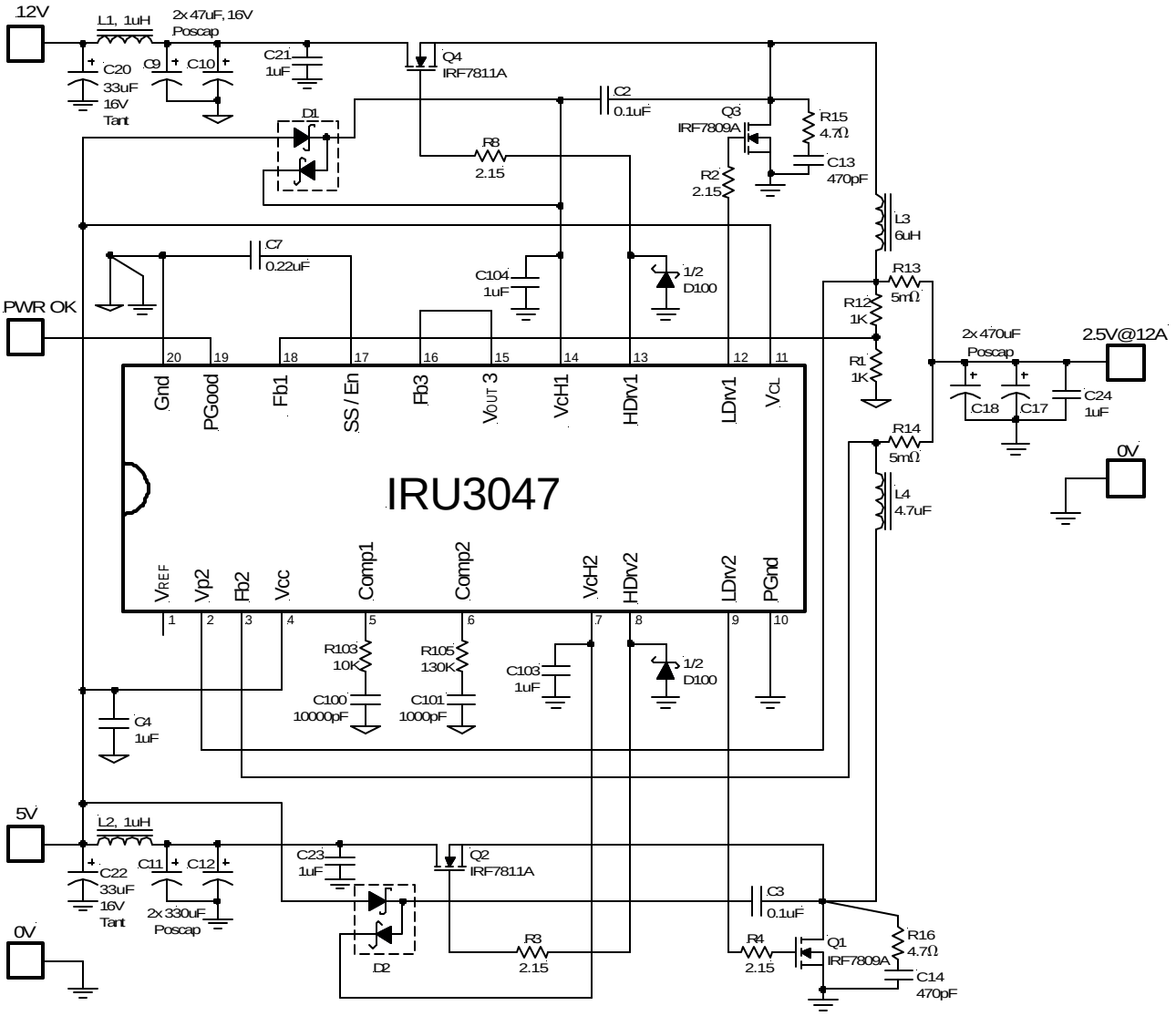


Figure 12 - Typical application for IRU3047 configured as 2-phase converter in current sharing mode.

DEMO-BOARD APPLICATION

Application Parts List

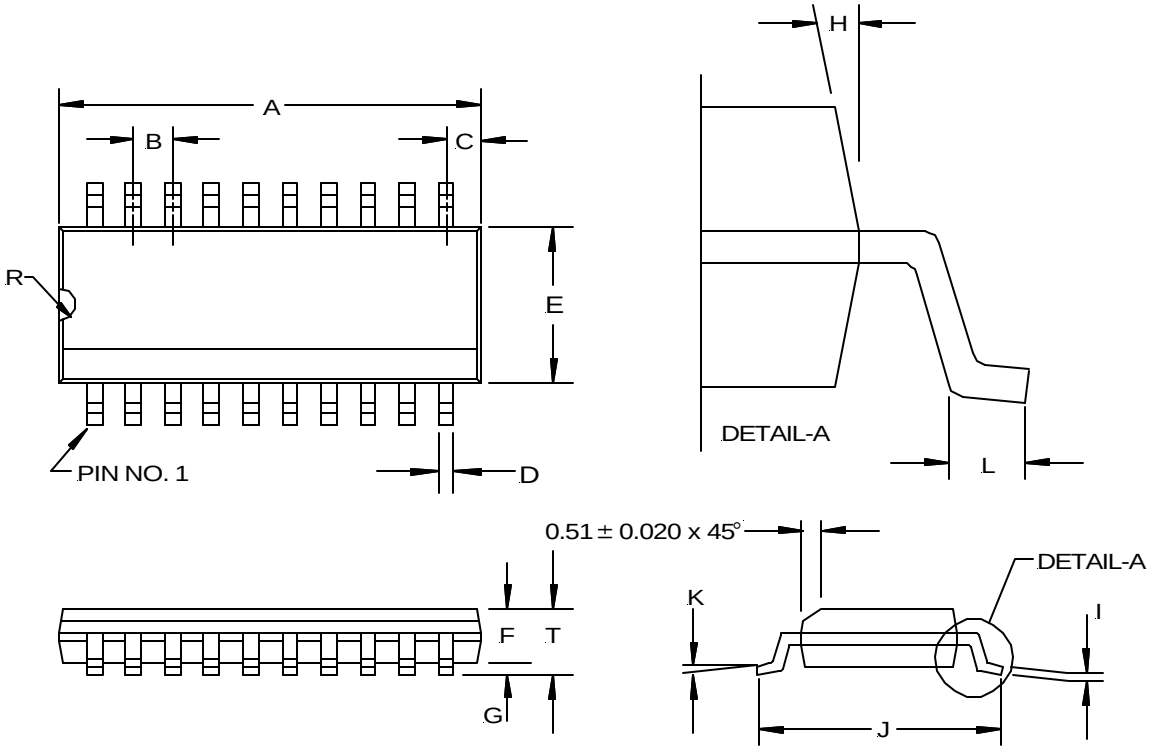
Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1, Q3	MOSFET	20V, 8.5mΩ, 14A	2	IRF7809A	IR	irf.com
Q2, Q4	MOSFET	28V, 12mΩ, 11A	2	IRF7811A	IR	
U1	Controller	Synchronous PWM	1	IRU3047	IR	
D1, D2	Diode	Fast Switching	2	BAT54S	IR	
D100 *	Diode	Fast Switching	1	BAT54A or 1N4148	IR Any	
L1, L2	Inductor	1μH, 3A	2	DS1608C-102	Coilcraft	coilcraft.com
L3	Inductor	6μH, 7.5A	1	D05022P-602HC	Coilcraft	
L4	Inductor	4.7μH, 8.4A	1	D05022P-472HC	Coilcraft	
C2,C3	Cap, Ceramic	0.1μF, Y5V, 25V	2	ECJ-3YB1E105K	Panasonic	maco.panasonic.co.jp
C4,21,23,24, 103,104	Cap, Ceramic	1μF, Y5V, 16V	6	ECJ-2VF1C105Z	Panasonic	
C7	Cap, Ceramic	0.22μF, Y5V, 25V	1	ECJ-3YB1E225K	Panasonic	
C101	Cap, Ceramic	1000pF, X7R, 50V	1	ECJ-2VB1H102K	Panasonic	
C9,C10	Cap, Poscap	47μF, 16V	2	16TPB47M	Sanyo	sanyo.com/industrial
C11,C12	Cap, Poscap	330μF, 6.3V	2	6TPB330M	Sanyo	
C13,C14	Cap, Poscap	470pF, X7R, 50V	2	ECJ-2VC1H471J	Panasonic	maco.panasonic.co.jp
C17,C18	Cap, Poscap	470μF, 6V, 40mΩ	2	6TPB470M	Sanyo	sanyo.com/industrial
C20,C22	Cap, Tantulum	33μF, 16V	2	EC-T1CD336R	Panasonic	maco.panasonic.co.jp
C100	Cap, Ceramic	10000pF	1			
R1,R12	Resistor	1K, 1%	2			
R2,3,4,8	Resistor	2.15Ω	4			
R13,R14	Resistor	5mΩ, 1W, 1%	2	ERJ-M1WSF5MOU		
R15,R16	Resistor	4.7Ω	2			
R103	Resistor	10K	1			
R105	Resistor	130K	1			

***** Use this diode for (source/sink, no load) applications when the inductor current goes negative and for the fast load transient from full output load to no load.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information

(W) SOIC Package
20-Pin Surface Mount, Wide Body

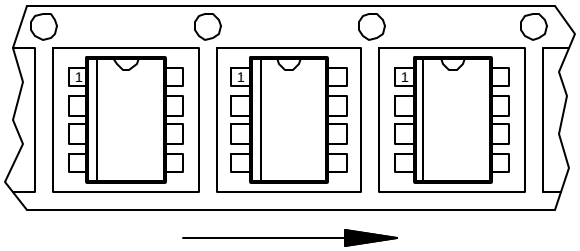


SYMBOL	20-PIN	
	MIN	MAX
A	12.598	12.979
B	1.018	1.524
C	0.66 REF	
D	0.33	0.508
E	7.40	7.60
F	2.032	2.64
G	0.10	0.30
I	0.229	0.32
J	10.008	10.654
K	0°	8°
L	0.406	1.270
R	0.63	0.89
T	2.337	2.642

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
W	SOIC, Wide Body	20	38	1000	Fig A



Feed Direction
Figure A

IRU3048

DUAL SYNCHRONOUS PWM CONTROLLER CIRCUITRY AND LDO CONTROLLER

PRELIMINARY DATA SHEET

FEATURES

- Dual Synchronous Controller in 16-Pin Package with 180° out-of-phase operation
- LDO Controller with 40mA drive
- Configured as 2-Independent PWM Controller
- Flexible, Same or Separate Supply Operation
- Operation from 4V to 25V Input
- Internal 200KHz Oscillator
- Soft-Start controls all outputs
- Fixed Frequency Voltage Mode
- 500mA Peak Output Drive Capability
- Programmable Outputs

DESCRIPTION

The IRU3048 IC combines a Dual synchronous Buck controller and a linear regulator controller, providing a cost-effective, high performance and flexible solution for multi-output applications. The Dual synchronous controller is configured as 2-independent PWM controller. IRU3048 provides a separate adjustable output by driving a switch as a linear regulator. This device features an internal 200KHz oscillator, under-voltage lockout for all input supplies, an external programmable soft start function as well as output under-voltage detection that latches off the device when an output short is detected.

APPLICATIONS

- DDR Memory Source Sink Vtt Application
- Graphic Card
- Hard Disk Drive
- Power supplies requiring multiple outputs

TYPICAL APPLICATION

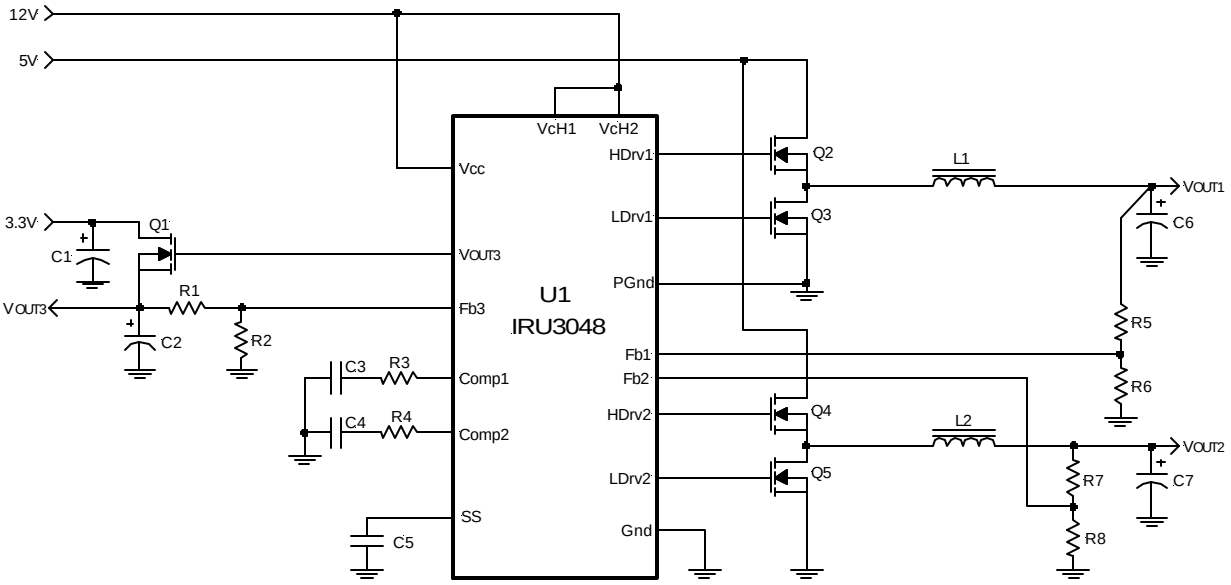


Figure 1 - Typical application of IRU3048 configured as 2-independent converter.

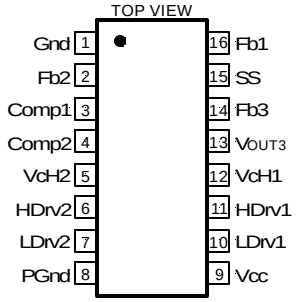
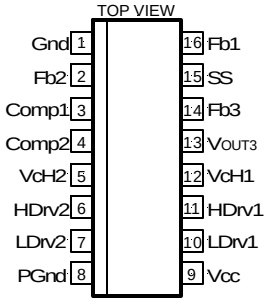
PACKAGE ORDER INFORMATION

T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3048CF	16-Pin TSSOP (F)
0 To 70	IRU3048CS	16-Pin SOIC NB (S)

ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage 25V
VcH1=VcH2 Supply Voltage ..... 30V (not rated for inductive load)
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

16-PIN PLASTIC TSSOP (F)	16-PIN PLASTIC SOIC NB (S)
	
θ_{JA}=90°C/W	θ_{JA}=85°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=5V, VcH1=VcH2=12V, T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage						
Fb Voltage	V_{FB}		1.225	1.250	1.275	V
Fb Voltage Line Regulation	L_{REG}	5<Vcc<12		0.2		%
UVLO						
UVLO Threshold - Vcc	$UVLO_{VCC}$	Supply Ramping Up		4.2		V
UVLO Hysteresis - Vcc				0.25		V
UVLO Threshold - VcH1	$UVLO_{VcH1}$	Supply Ramping Up		3.5		V
UVLO Hysteresis - VcH1				0.2		V
UVLO Threshold - VcH2	$UVLO_{VcH2}$	Supply Ramping Up		3.5		V
UVLO Hysteresis - VcH2				0.2		V
UVLO Threshold - Fb	$UVLO_{FB}$	Fb Ramping Down		0.6		V
UVLO Hysteresis - Fb				0.1		V
Supply Current						
Vcc Dynamic Supply Current	Dyn I_{CC}	Freq=200KHz, C_L=1500pF		5		mA
VcH1 Dynamic Supply Current	Dyn I_{cH1}	Freq=200KHz, C_L=1500pF		7		mA
VcH2 Dynamic Supply Current	Dyn I_{cH2}	Freq=200KHz, C_L=1500pF		7		mA
Vcc Static Supply Current	I_{CCQ}	SS=0V		3.5		mA
VcH1 Static Supply Current	I_{cH1Q}	SS=0V		2		mA
VcH2 Static Supply Current	I_{cH2Q}	SS=0V		2		mA
Soft-Start Section						
Charge Current	SS_{IB}	SS=0V	15	25	30	µA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Amp						
Fb Voltage Input Bias Current	I_{FB1}	SS=3V		-0.1		µA
Fb Voltage Input Bias Current	I_{FB2}	SS=0V		-64		µA
Transconductance 1	g_{m1}			400		µmho
Transconductance 2	g_{m2}			600		µmho
Oscillator						
Frequency	Freq		180	200	220	KHz
Ramp Amplitude	V_{RAMP}			1.25		V_{PP}
Output Drivers						
Rise Time	Tr	C_L=1500pF		35	100	ns
Fall Time	Tf	C_L=1500pF		50	100	ns
Dead Band Time	T_{DB}		50	150	250	ns
Max Duty Cycle	T_{ON}	Fb=1V, Freq=200KHz	85	90		%
Min Duty Cycle	T_{OFF}	Fb=1.5V	0	0		%
LDO Controller						
Drive Current	I_{LDO}		30	45		mA
Fb Voltage	V_{FB}LDO		1.225	1.25	1.275	V
Input Bias Current	$I_{LDO(BIAS)}$			0.5	2	µA

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Gnd	Ground pin.
2 16	Fb2 Fb1	Inverting inputs to the error amplifiers. These pins work as feedback inputs for each channel, and are connected directly to the output of the switching regulator via a resistor divider to set the output voltages.
3 4	Comp1 Comp2	Compensation pins for the error amplifiers.
5 12	VcH2 VcH1	Supply voltage for the high side output drivers. These are connected to voltages that must be at least 4V higher than their bus voltages (assuming 5V threshold MOSFET). A minimum of 1µF high frequency capacitor must be connected from these pins to PGnd pin to provide peak drive current capability.
6 11	HDrv2 HDrv1	Output driver for the high side power MOSFET. Connect a diode, such as BAT54 or 1N4148, from these pins to ground for the application when the inductor current goes negative (Source/Sink), soft-start at no load and for the fast load transient from full load to no load.
7 10	LDrv2 LDrv1	Output driver for the synchronous power MOSFET.
8	PGnd	This pin serves as the separate ground for MOSFET's driver and should be connected to the system's ground plane.
9	Vcc	Supply voltage for the internal blocks of the IC.
13	V_{OUT3}	Driver signal for the LDO's external transistor.
14	Fb3	LDO's feedback pin, connected to a resistor divider to set the output voltage of LDO.
15	SS	Soft-Start pin. The converter can be shutdown by pulling this pin below 0.5V.

BLOCK DIAGRAM

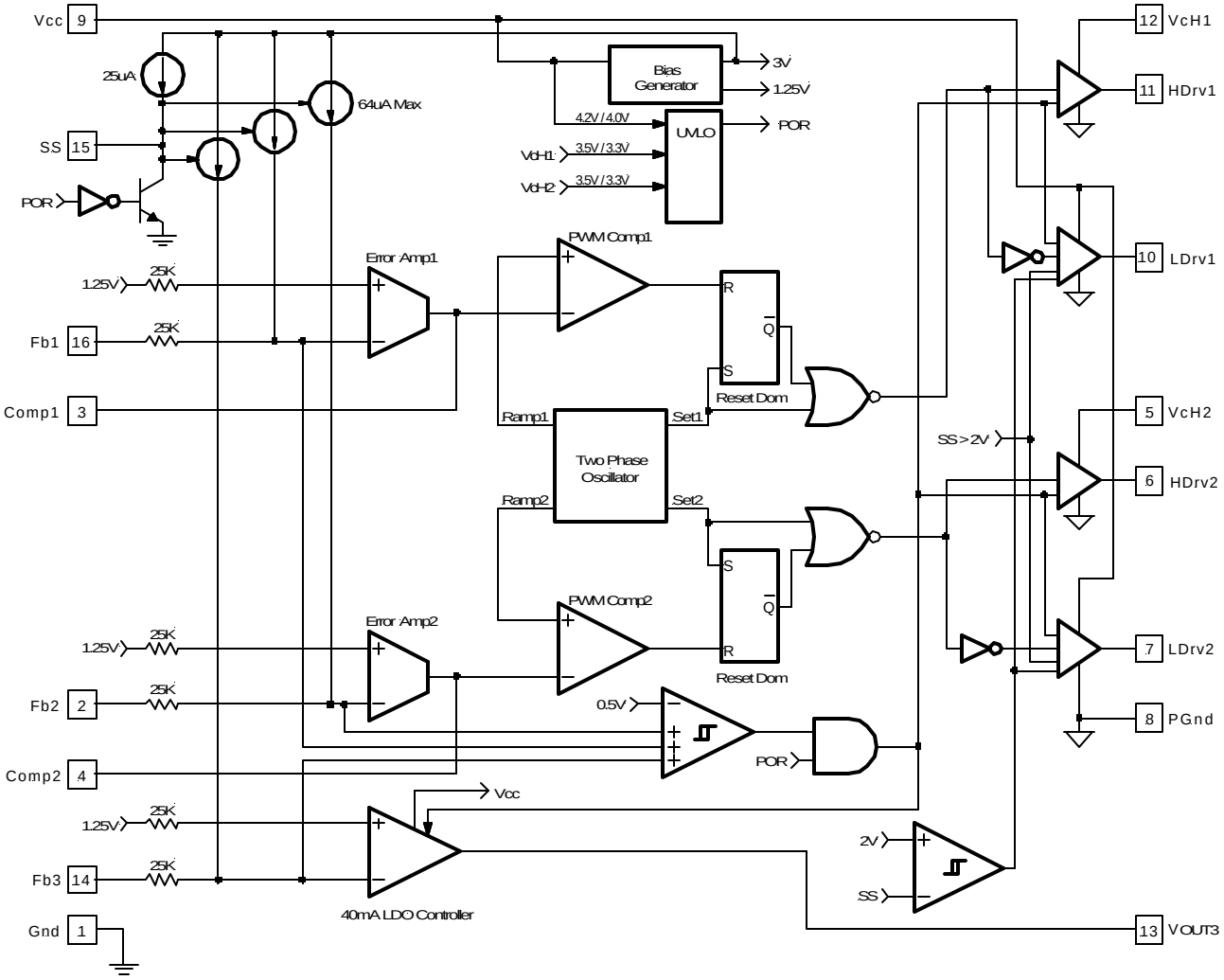


Figure 2 - Block diagram of the IRU3048.

THEORY OF OPERATION

Introduction
The IRU3048 is designed for multi-outputs applications. It includes two synchronous buck controllers and a linear regulator controller. The two synchronous controller operates with fixed frequency voltage mode and is configured as two independent controllers. The timing of the IC is provided through an internal oscillator circuit. These are two out of phase oscillators.

Soft-Start
The IRU3048 has a programmable soft start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vcc, VcH1 and VcH2 rise above their threshold and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter. As the charging voltage of the external capacitor ramps up, the PWM signals increase from zero to the point the feedback loop takes control.

Out of Phase Operation
The IRU3048 drives its two output stages 180° out of phase. In application with single input voltage, the out of phase operation reduces the input ripple current. This results in much smaller RMS current in the input capacitor and reduction of input capacitors.

Shutdown
The converter can be shutdown by pulling the soft-start pin below 0.5V. This can be easily done by using an external small signal transistor. During shutdown the MOSFET drivers and the LDO controller turn off.

Short-Circuit Protection
The outputs are protected against the short circuit. The IRU3048 protects the circuit for shorted output by sensing the output voltages. The IRU3048 shuts down the PWM signals and LDO controller, when the output voltages drops below the set values.

Under-Voltage Lockout
The under-voltage lockout circuit assures that the MOSFET driver outputs and LDO controller remain in the off state whenever the supply voltages drop below set parameters. Normal operation resumes once the supply voltages rise above the set values.

APPLICATION INFORMATION

Design Example:
The following example is a typical application for IRU3048 in current sharing mode. The schematic is Figure 9 on page 12.

For Switcher	For Linear Regulator
V_{IN1} = 12V	V_{IN3} = 3.3V
V_{OUT1} = 3.3V	V_{OUT3} = 2.5V
I_{OUT1} = 4A	I_{OUT3} = 2A
V_{IN2} = 5V	
V_{OUT2} = 1.8V	
I_{OUT2} = 4A	
ΔV_{OUT} = 75mV	
f_S = 200KHz	

PWM Section

Output Voltage Programming
Output voltage is programmed by reference voltage and external voltage divider. The Fb1 pin is the inverting input of the error amplifier, which is internally referenced to 1.25V. The divider is ratioed to provide 1.25V at the Fb1 pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT1} = V_{REF} \times \left(1 + \frac{R_6}{R_8}\right) \qquad \text{---(1)}$$

When an external resistor divider is connected to the output as shown in Figure 3.

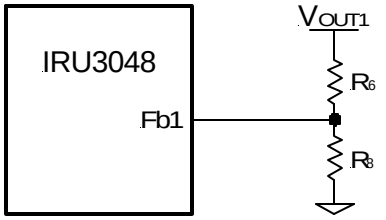


Figure 3 - Typical application of the IRU3048 for programming the output voltage.

Equation (1) can be rewritten as:

$$R_6 = R_8 \times \left(\frac{V_{OUT1}}{V_{REF}} - 1\right)$$

Will result to:

V_{OUT1}=3.3V	V_{OUT2}=1.8V
V_{REF}=1.25V	V_{REF}=1.25V
R_8=1K, R_6=1.64K	R_{15}=1K, R_{14}=442Ω

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft start capacitance value. The start up time of the converter can be calculated by using:

$$t_{START} = 75 \times Css \quad (ms) \qquad ---(2)$$

Where:
C_{SS} is the soft-start capacitor (μF)

For a start-up time of 7.5ms, the soft-start capacitor will be 0.1μF. Choose a ceramic capacitor at 0.1μF.

Boost Supply Vc

To drive the high-side switch it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 9. The capacitor is charged up to approximately twice the bus voltage. A capacitor in the range of 0.1μF to 1μF is generally adequate for most applications.

Input Capacitor selection

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of control MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_{OUT} \sqrt{D \times (1-D)} \qquad ---(3)$$

Where:
D is the Duty Cycle, simply $D=V_{OUT}/V_{IN}$.
I_{RMS} is the RMS value of the input capacitor current.
I_{OUT} is the output current for each channel.

For V_{IN1}=12V, I_{OUT1}=4A and D1=0.275
Results to: I_{RMS1}=1.78A

And for V_{IN2}=5V, I_{OUT2}=4A and D2=0.36
Results to: I_{RMS2}=1.92A

For higher efficiency, a low ESR capacitor is recommended.

For V_{IN1}=12V, choose one Poscap from Sanyo 16TPB47M (16V, 47μF, 70mΩ, 1.4A)

For V_{IN2}=5V, choose one 6TPC150M (6.3V, 150μF, 40mΩ, 1.9A).

Output Capacitor Selection

The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$ESR \le \frac{\Delta V_O}{\Delta I_O} \qquad ---(4)$$

Where:
ΔV_O = Output Voltage Ripple
ΔI_O = Output Current
ΔV_O=75mV and ΔI_O=3A, results to: ESR=25mΩ

The Sanyo TPC series, PosCap capacitor is a good choice. The 6TPC150M 150μF, 6.3V has an ESR 40mΩ. Selecting two of these capacitors in parallel for each output, results to an ESR of $\cong$ 20mΩ which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

The resulting output ripple current is smaller then each channel ripple current due to the 180° phase shift. These currents cancel each other. The cancellation is not the maximum because of the different duty cycle for each channel.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi); the optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \; ; \; \Delta t = D \times \frac{1}{f_S} \; ; \; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \qquad ---(5)$$

Where:
V_{IN} = Max Input Voltage
V_{OUT} = Output Voltage
Δi = Inductor Ripple Current
f_S = Switching Frequency
Δt = Turn On Time
D = Duty Cycle

For Δi_1=25% of I_1, we get L_1=9.9µH
For Δi_2=25% of I_2, we get: L_2=5.7µH

Panasonic provides a range of inductors in different values and low profile for large currents.

For L_1 choose ETQP6F102HFA (10.2µH, 4A)
For L_2 choose ELLATV6R8M (6.8µH, 4A)

Power MOSFET Selection
The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{IN}).

The gate drive requirement is almost the same for both MOSFETs. Caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{COND}(\text{Upper Switch}) = I_{LOAD}^2 \times R_{DS(ON)} \times D \times \vartheta$$

$$P_{COND}(\text{Lower Switch}) = I_{LOAD}^2 \times R_{DS(ON)} \times (1 - D) \times \vartheta$$

ϑ = $R_{DS(ON)}$ Temperature Dependency

The total conduction loss is defined as:

$$P_{CON(TOTAL)} = P_{CON}(\text{Upper Switch})\vartheta + P_{CON}(\text{Lower Switch})\vartheta$$

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

For this design, IRF7313 is a good choice. These devices provide low on-resistance in a compact SOIC 8-Pin package.

The MOSFETs have the following data:

IRF7313
V_{DSS} = 30V
I_D = 5.2A @ 70°C
$R_{DS(ON)}$ = 46mΩ @ V_{GS}=4.5V
ϑ = 1.5 for 150°C (Junction Temperature)

The total conduction losses for channel 1 is:

P_{CON1} = 1.1W

The total conduction losses for channel 2 is:

P_{CON2} = 1.1W

The control MOSFET contributes to the majority of the switching losses in synchronous Buck converter. The synchronous MOSFET turns on under zero-voltage condition, therefore the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \qquad \text{---(6)}$$

Where:
$V_{DS(OFF)}$ = Drain to Source Voltage at off time
t_r = Rise Time
t_f = Fall Time
T = Switching Period
I_{LOAD} = Load Current

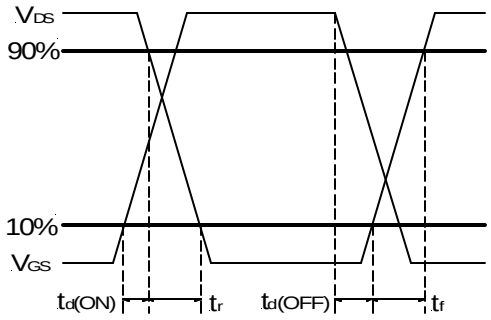


Figure 4 - Switching time waveforms.

From IRF7313 data sheet we obtain:

IRF7313
t_r = 13ns
t_f = 26ns

These values are taken under a certain condition test. For more detail please refer to the IRF7313 data sheet.

By using equation (6), we can calculate the switching losses.

P_{SW1} = 187.2mW
P_{SW2} = 78mW

Feedback Compensation

The IRU3048 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 5). The Resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2\pi\sqrt{Lo \times Co}} \qquad ---(7)$$

Figure 5 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

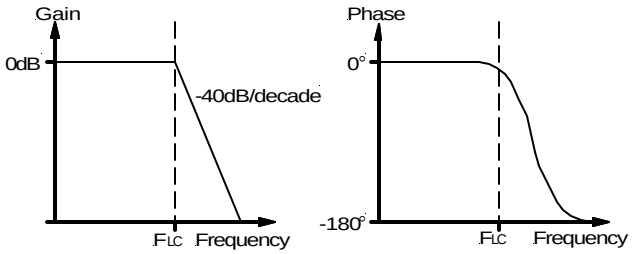


Figure 5 - Gain and phase of LC filter.

The IRU3048's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp1 pin to ground as shown in Figure 6.

The ESR zero of the LC filter expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \qquad ---(8)$$

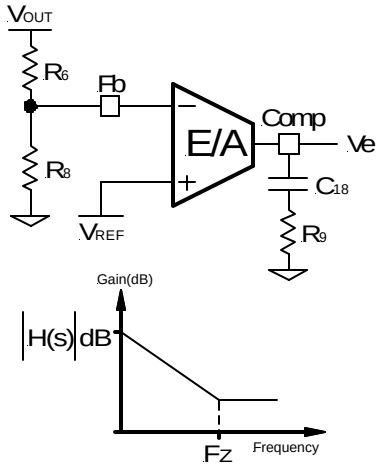


Figure 6 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / V_{OUT}) is given by:

$$H(s) = \left(g_m \times \frac{R_8}{R_6 + R_8}\right) \times \frac{1 + sR_9C_{18}}{sC_{18}} \qquad ---(9)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = g_m \times \frac{R_8}{R_6 \times R_8} \times R_9 \qquad ---(10)$$

$$F_Z = \frac{1}{2\pi \times R_9 \times C_{18}} \qquad ---(11)$$

The gain is determined by the voltage divider and E/A's transconductance gain.

First select the desired zero-crossover frequency (Fo):

$F_{O1} > F_{ESR}$ and $F_{O1} \leq (1/5 \sim 1/10) \times f_S$

Use the following equation to calculate R4:

$$R_9 = \frac{V_{OSC}}{V_{IN1}} \times \frac{F_{O1} \times F_{ESR1}}{F_{LC1}^2} \times \frac{R_8 + R_6}{R_8} \times \frac{1}{g_m} \qquad ---(12)$$

Where:
V_{IN1} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
F_{O1} = Crossover Frequency for the master E/A
F_{ESR1} = Zero Frequency of the Output Capacitor
F_{LC1} = Resonant Frequency of Output Filter
g_m = Error Amplifier Transconductance
R_8 and R_6 = Resistor Dividers for Output Voltage Programming

For:

V_{IN1} = 12V
V_{OSC} = 1.25V
F_{O1} = 30KHz
F_{ESR1} = 26.5KHz
F_{LC1} = 2.8KHz
R_8 = 1K
R_6 = 1.64K
gm = 600µmho

This results to R_9=46.4KΩ; Choose R_9=46.4KΩ

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_Z \cong 75\% F_{LC1}$$

$$F_Z \cong 0.75 \times \frac{1}{2\pi\sqrt{L_3 \times C_O}} \qquad ---(13)$$

For:

L_3 = 10.2µH
Co = 300µF
Fz = 2.1KHz
R_9 = 46.4KΩ

Using equations (11) and (13) to calculate C_9, we get:

C_9= 1630pF; Choose C_9 = 1800pF

Using equations (11),(12) and (13) for Ch2, where:

V_{IN2} = 5V
V_{OSC} = 1.25V
F_{O2} = 30KHz
F_{ESR2} = 26.5KHz
F_{LC2} = 3.5KHz
R_{15} = 1K
R_{14} = 442Ω
gm = 600µhmo

We get:

R_{11} = 38.9KΩ; Choose R_{11} = 39.2KΩ
C_{19} = 1554pF; Choose C_{19} = 1800pF

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to supress the switching noise. The additional pole is given by:

$$F_P = \frac{1}{2\pi \times R_9 \times \frac{C_{18} \times C_{POLE}}{C_{18} + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi \times R_9 \times f_S - \frac{1}{C_{18}}} \cong \frac{1}{\pi \times R_9 \times f_S}$$

For $F_P << \frac{f_S}{2}$

For a general solution for unconditionally stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 7.

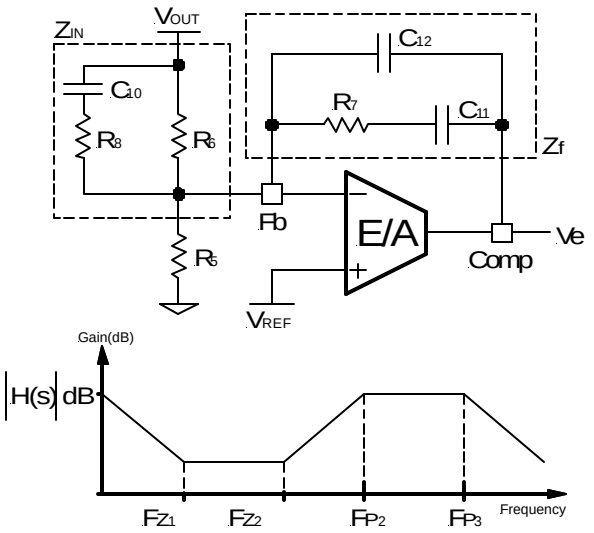


Figure 7 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - gmZ_f}{1 + gmZ_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$gmZ_f >> 1 \quad \text{and} \quad gmZ_{IN} >> 1 \qquad ---(14)$$

By replacing Z_{IN} and Z_f according to figure 7, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11}) \times [1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12}C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+sR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0 \qquad F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_{O1} = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \quad \text{---(15)}$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Lo = Output Inductor
Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition 14 regarding transconductance error amplifier.

1) Select the crossover frequency:

$F_O < F_{ESR}$ and $F_O \leq (1/10 \sim 1/6) \times f_S$

2) Select R_7, so that $R_7 >> \frac{2}{gm}$

3) Place first zero before LC's resonant frequency pole.

$F_{Z1} \cong 75\% F_{LC}$

$$C_{11} = \frac{1}{2\pi \times F_{Z1} \times R_7}$$

4) Place third pole at the half of the switching frequency.

$$F_{P3} = \frac{f_S}{2}$$

$$C_{12} = \frac{1}{2\pi \times R_7 \times F_{P3}}$$

$C_{12} > 50pF$
If not, change R_7 selection.

5) Place R_7 in (15) and calculate C_{10}:

$$C_{10} \leq \frac{2\pi \times Lo \times F_O \times Co}{R_7} \times \frac{V_{OSC}}{V_{IN}}$$

6) Place second pole at ESR zero.
$F_{P2} = F_{ESR}$

$$R_8 = \frac{1}{2\pi \times C10 \times F_{P2}}$$

Check if $R_8 > \frac{1}{gm}$

If R_8 is too small, increase R_7 and start from step 2.

7) Place second zero around the resonant frequency.
$F_{Z2} = F_{LC}$

$$R_6 = \frac{1}{2\pi \times C10 \times F_{Z2}} - R_8$$

8) Use equation (1) to calculate R_5:

$$R_5 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_6$$

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

LDO Section

Output Voltage Programming

Output voltage for LDO is programmed by reference voltage and external voltage divider. The Fb3 pin is the inverting input of the error amplifier, which is internally referenced to 1.25V. The divider is ratioed to provide 1.25V at the Fb3 pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT2} = V_{REF} \times \left(1 + \frac{R_{HIGH}}{R_{LOW}}\right)$$

For:
V_{OUT2} = 2.5V
V_{REF} = 1.25V
R_{LOW} = 1K

Results to: R_{HIGH}=1K

LDO Power MOSFET Selection

The first step in selecting the power MOSFET for the linear regulator is to select the maximum $R_{DS(ON)}$ based on the input to the dropout voltage and the maximum load current.

$$R_{DS(ON)} = \frac{V_{IN3} - V_{OUT2}}{I_{OUT2}}$$

For:
V_{IN3} = 3.3V
V_{OUT2} = 2.5V
I_{OUT2} = 2A

Results to: $R_{DS(ON)(MAX)} = 0.4\Omega$

Note that since the MOSFET $R_{DS(ON)}$ increases with temperature, this number must be divided by ~1.5 in order to find the $R_{DS(ON)(MAX)}$ at room temperature. The IRLR2703 has a maximum of 0.065Ω $R_{DS(ON)}$ at room temperature, which meets our requirements.

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

TYPICAL APPLICATION

12V to 3.3V @ 4A
12V to 1.8V @ 4A
3.3V to 2.5V @ 2A

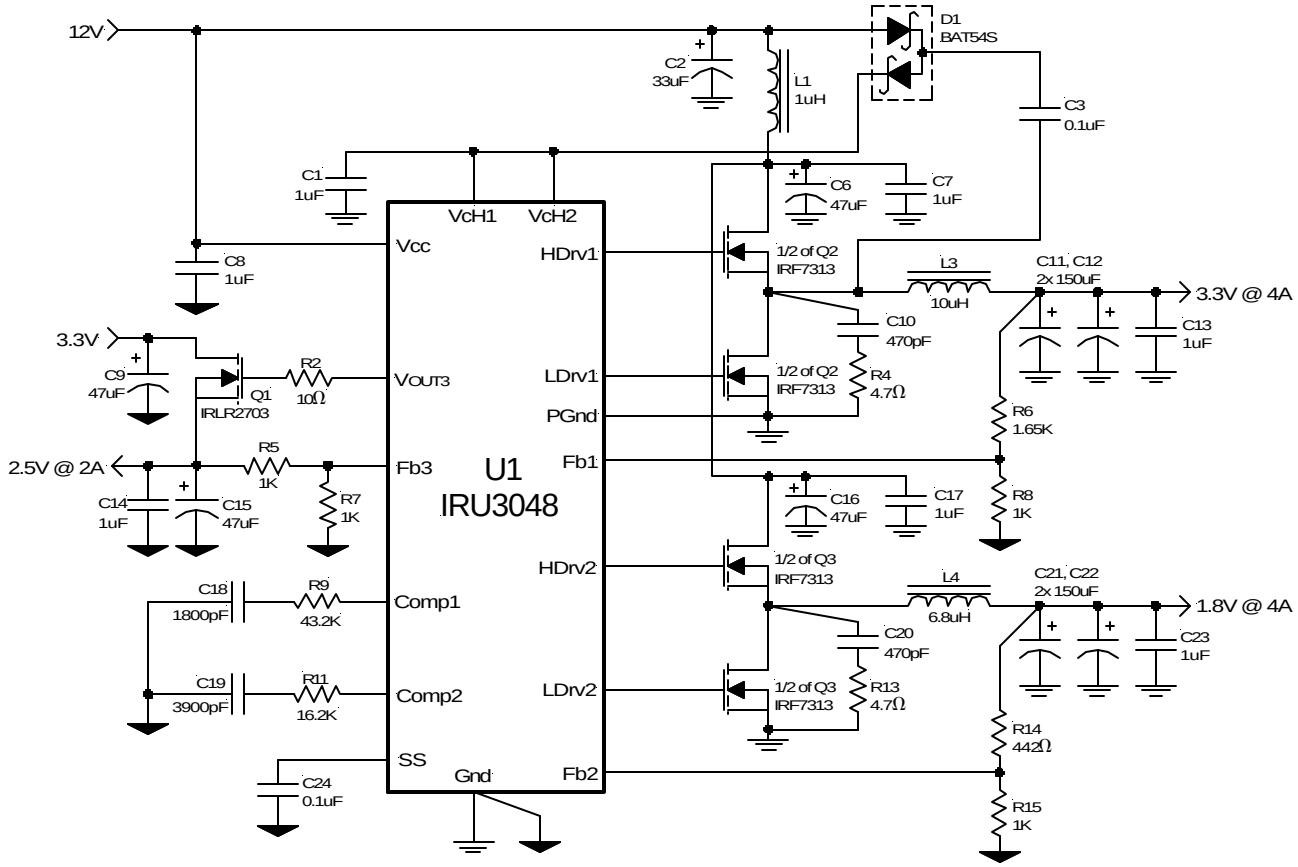


Figure 8 - Typical application of IRU3048 in an on-board DC-DC converter using a single 12V supply for switcher.

DEMO-BOARD APPLICATION

12V to 3.3V @ 4A
5V to 1.8V @ 4A
3.3V to 2.5V @ 2A

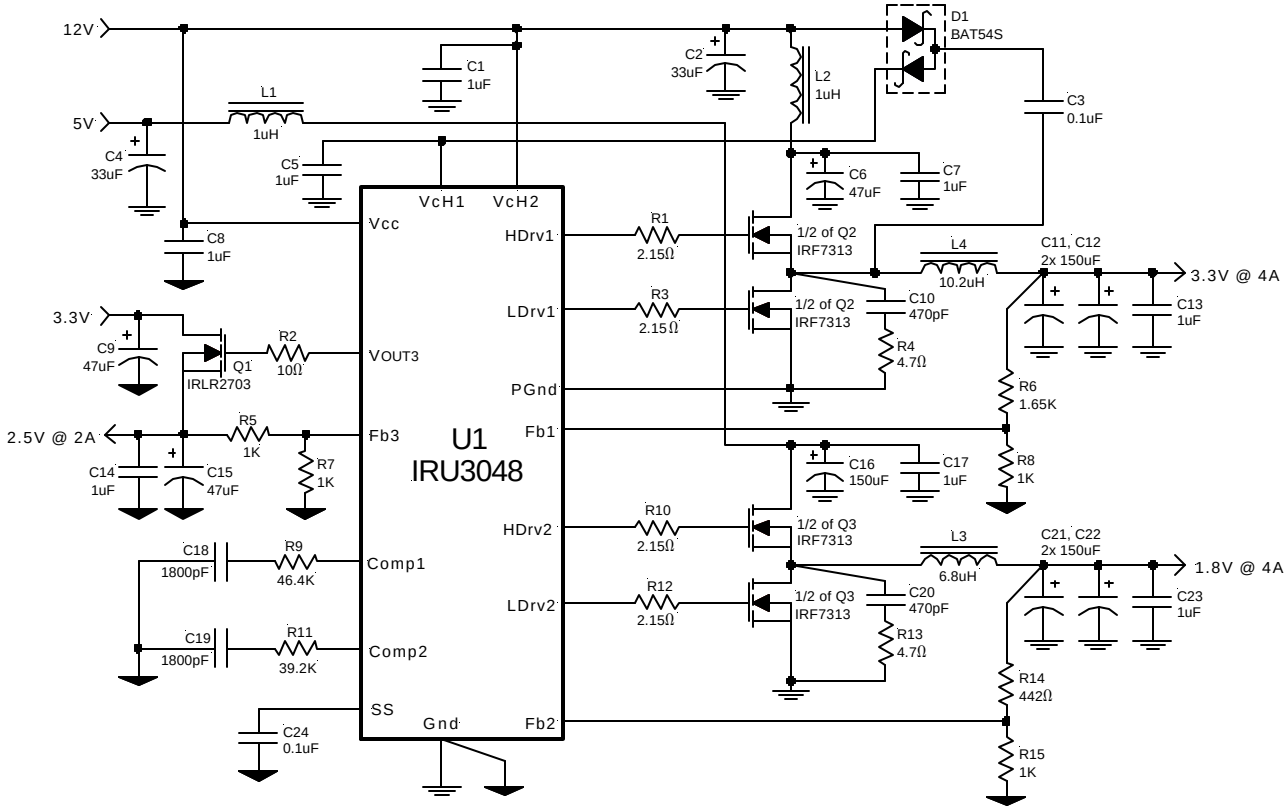


Figure 9 - Demo-board application of IRU3048.

DEMO-BOARD APPLICATION

12V to 3.3V @ 4A
5V to 1.8V @ 4A
3.3V to 2.5V @ 2A

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1	MOSFET	30V, 45mΩ	1	IRLR2703	IR	irf.com
Q2, Q3	MOSFET	30V, 29mΩ, 5.2A	2	IRF7313	IR	
U1	Controller	Synchronous PWM	1	IRU3048CF	IR	
D1	Diode	Fast Switching	1	BAT54S	IR	
L1, L2	Inductor	1μH, 2.9A	2	ELL6SH1R0M	Panasonic	maco.panasonic.co.jp
L3	Inductor	6.8μH, 4A	1	ELLATV6R8M	Panasonic	
L4	Inductor	10.2μH, 4A	1	ETQP6F102HFA	Panasonic	
C1,7,8,13, 14,17,23	Cap, Ceramic	1μF, Y5V, 16V	7	ECJ-2VF1C105Z	Panasonic	
C2, C4	Cap, Tantalum	33μF, 16V	2	ECS-T1CD336R	Panasonic	
C3, C24	Cap, Ceramic	0.1μF, Y5V, 25V	2	ECJ-2VF1E104Z	Panasonic	
C5	Cap, Ceramic	1μF, X7R, 25V	1	ECJ-3YB1E105K	Panasonic	
C9, C15	Cap, Tantalum	47μF, 10V	2	ECS-T1AD476R	Panasonic	
C10, C20	Cap, Ceramic	470pF, X7R, 50V	2	ECJ-2VC1H471J	Panasonic	
C18, C19	Cap, Ceramic	1800pF, X7R, 50V	2	ECJ-2VB1H182K	Panasonic	
C6	Cap, Poscap	47μF, 16V, 70mΩ	1	16TPB47M	Sanyo	sanyo.com/industrial
C11,12,16 21,22	Cap, Poscap	150μF, 6.3V, 40mΩ	5	6TPC150M	Sanyo	
R1,3,10,12	Resistor	2.15Ω	4			
R2	Resistor	10Ω	1			
R4, R13	Resistor	4.7Ω	2			
R5,7,8,15	Resistor	1K, 1%	4			
R6	Resistor	1.65K, 1%	1			
R9	Resistor	46.4K	1			
R11	Resistor	39.2K	1			
R14	Resistor	442Ω, 1%	1			

WAVEFORMS

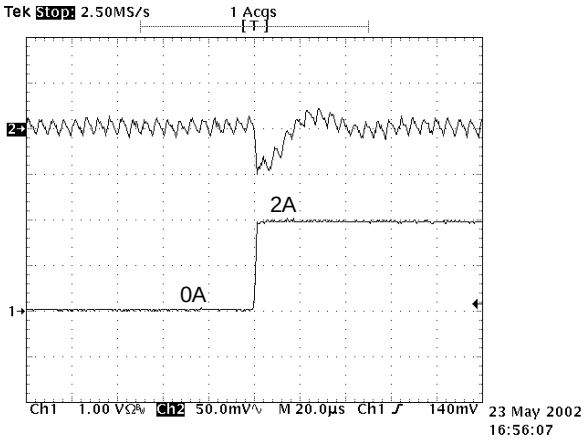


Figure 4 - Transient response @ I_{OUT} = 0 to 2A for 3.3V output.

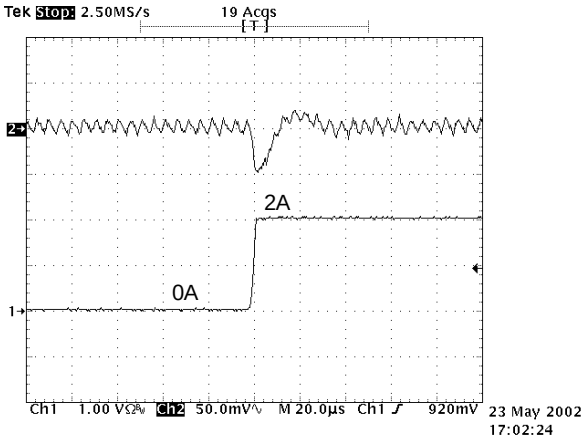


Figure 5 - Transient response @ I_{OUT} = 0 to 2A for 1.8V output.

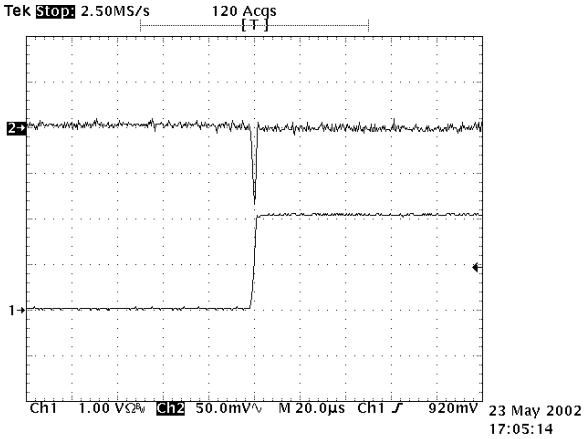


Figure 6 - Transient response @ I_{OUT} = 0 to 2A for 2.5V output.

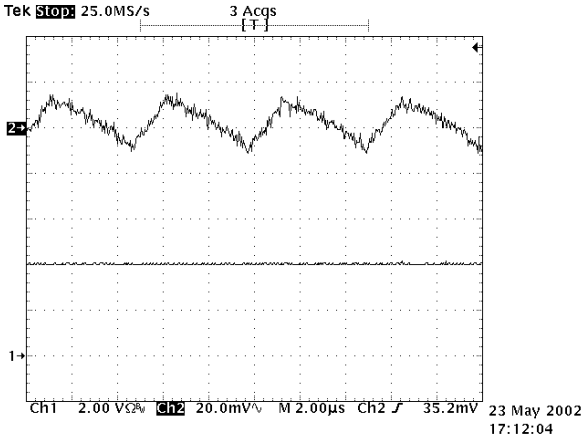


Figure 7 - Output voltage ripple for 3.3V @ 4A.

WAVEFORMS

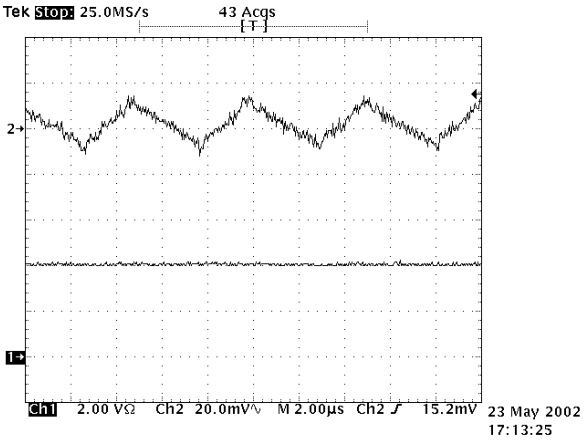


Figure 8 - Output voltage ripple for 1.8V @ 4A.

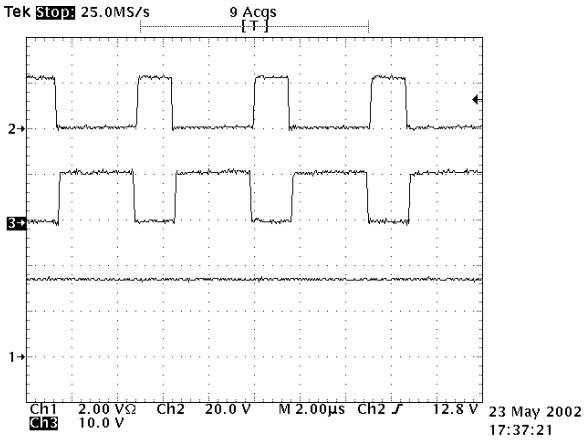


Figure 9 - Gate signals for 3.3V output.
Ch1: Output current 2A/div.
Ch2: Gate signal for control FET 20V/div.
Ch3: Gate signal for sync FET 10V/div.

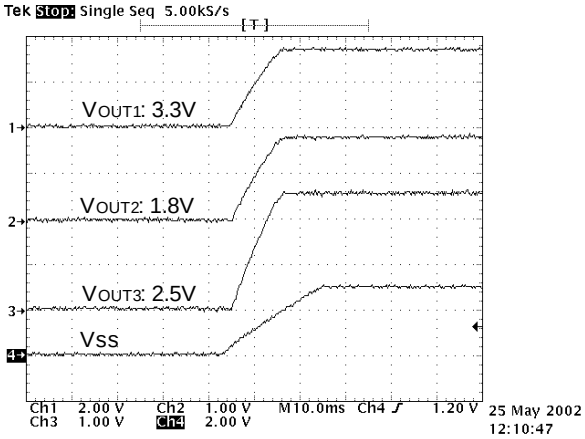


Figure 10 - Soft-start voltage Vs. output voltages.

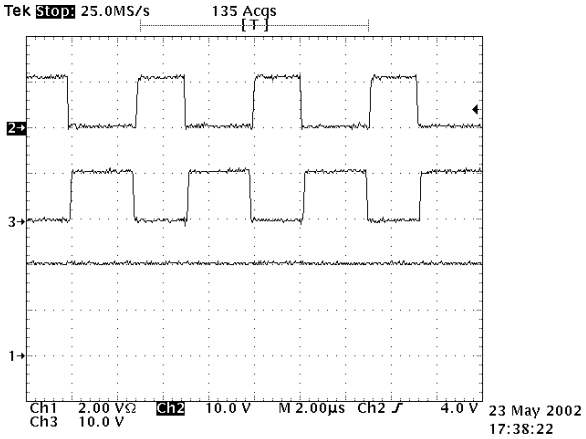


Figure 11 - Gate signals for 1.8V output.
Ch1: Output current 2A/div.
Ch2: Gate signal for control FET 10V/div.
Ch3: Gate signal for sync FET 10V/div.

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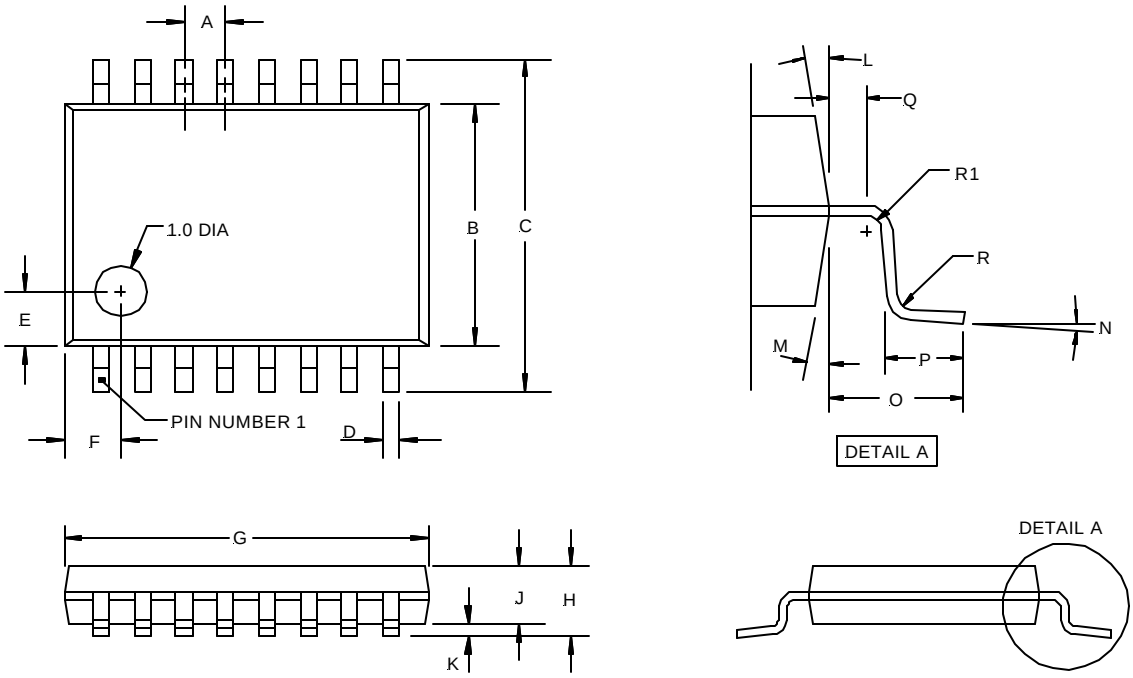
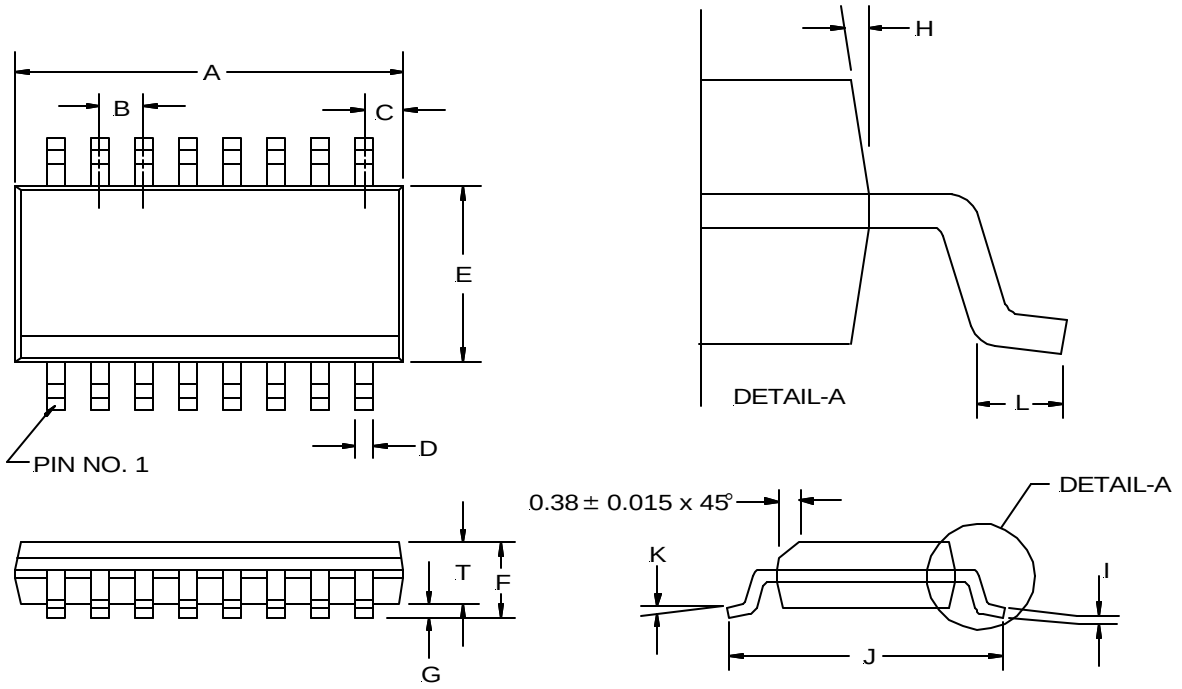
(F) TSSOP Package
16-Pin



SYMBOL DESIG	16-PIN		
	MIN	NOM	MAX
A		0.65 BSC	
B	4.30	4.40	4.50
C		6.40 BSC	
D	0.19	---	0.30
E		1.00	
F		1.00	
G	4.90	5.00	5.10
H	---	---	1.10
J	0.85	0.90	0.95
K	0.05	---	0.15
L		12° REF	
M		12° REF	
N	0°	---	8°
O		1.00 REF	
P	0.50	0.60	0.75
Q		0.20	
R	0.09	---	---
R1	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

(S) SOIC Package
16-Pin Surface Mount, Narrow Body



16-PIN		
SYMBOL	**MIN**	**MAX**
A	9.80	9.98
B	1.27 BSC	
C	0.51 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
F	TSSOP Plastic	16	---	2500	Fig A
S	SOIC, Narrow Body	16	50	2500	Fig B

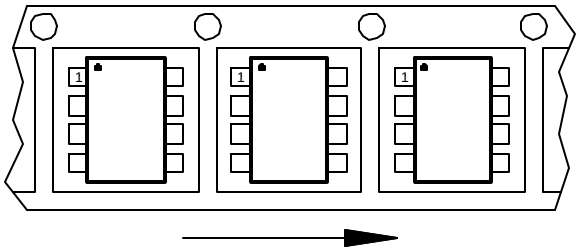


Figure A

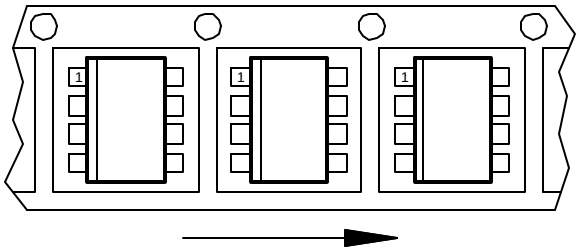


Figure B

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IRU3055

5-BIT PROGRAMMABLE 3-PHASE SYNCHRONOUS BUCK CONTROLLER IC

PRELIMINARY DATA SHEET TEST SPEC

FEATURES

- Meets VRM 9.0 Specification
- 3-Phase Controller with On-Board MOSFET Driver
- On-Board DAC programs the output voltage from 1.075V to 1.850V
- Loss-less Short Circuit Protection
- Programmable Frequency
- Synchronous operation allows maximum efficiency
- Minimum Part Count
- Soft-Start
- Power Good Function
- Hiccup Mode Current Limit

APPLICATIONS

- Intel Pentium 4 and AMD K7

DESCRIPTION

The IRU3055 is a 3-phase synchronous Buck controller which provides high performance DC to DC converter for high current applications.

The IRU3055 controller IC is specifically designed to meet Intel and AMD specifications for the new microprocessor requiring low voltage and high current.

The IRU3055 features under-voltage lockout for both 5V and 12V supplies, an external and programmable soft-start function as well as programming the oscillator frequency by using an external resistor.

TYPICAL APPLICATION

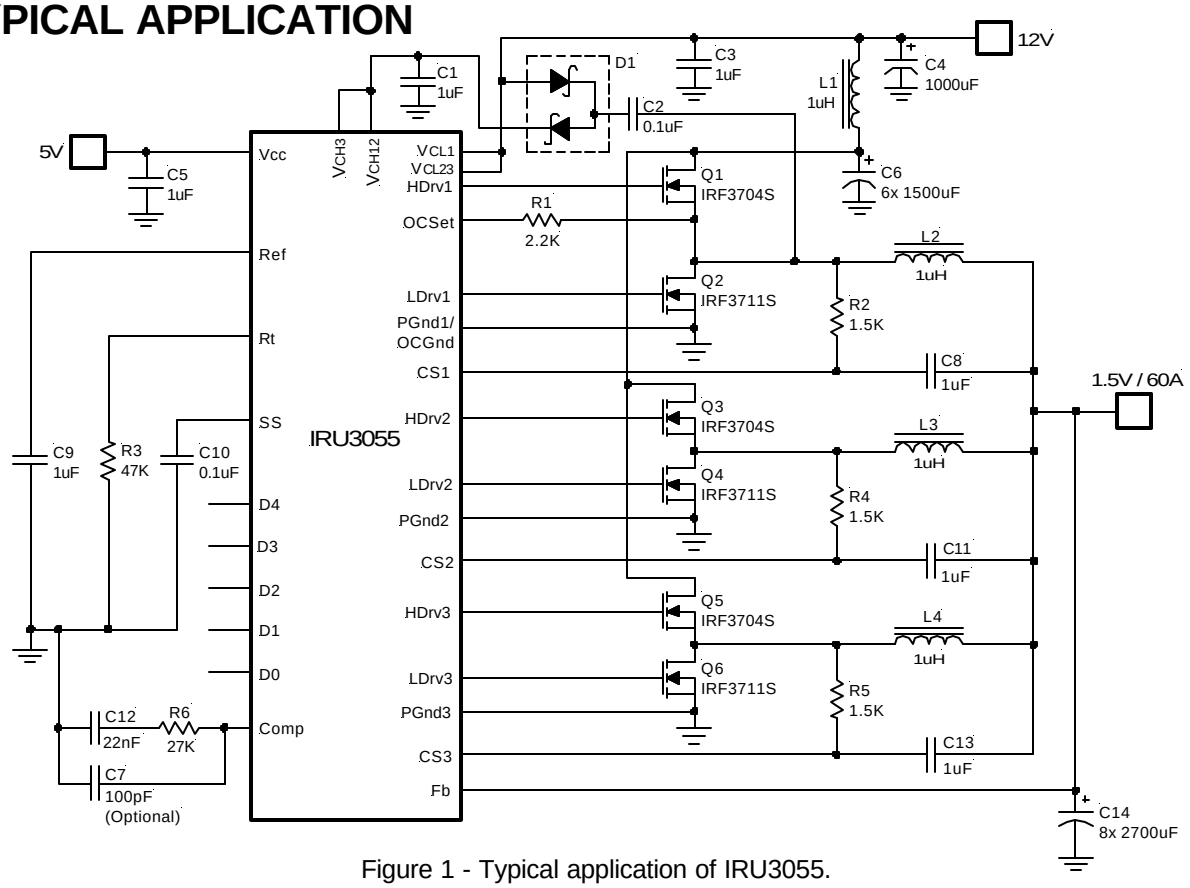


Figure 1 - Typical application of IRU3055.

PACKAGE ORDER INFORMATION

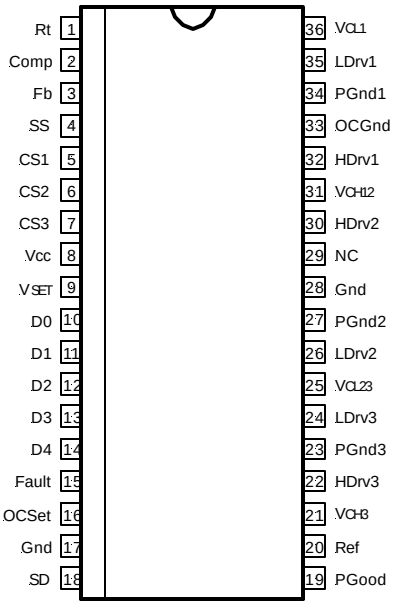
T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3055CQ	36-Pin Plastic QSOP WB (Q)

ABSOLUTE MAXIMUM RATINGS

V_{CH12} and V_{CH3} Supply Voltage ..... 30V (not rated for inductor load)
V_{CL1} and V_{CL23} Supply Voltage 20V
V_{CC} Supply Voltage 7V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

36-PIN WIDE BODY PLASTIC QSOP (Q)



θ_{JA} =60°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V_{CL1}=V_{CL23}=V_{CH12}=V_{CH3}=12V, Vcc=5V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Current Section						
Operating Supply Current		C_L High Side=3000pF C_L Low Side=6000pF				
	I_{CC}	V5	17	19	21	
	I_{CLH}	V12 (150KHz frequency)	30	50	70	mA
VID Section						
DAC Output Voltage (Note 1)	V_{DAC}		-1.5	Vs	+1.5	%
DAC Output Line Regulation	L_{REG}	4.5 < Vcc < 5.5V	-0.7	-0.06	+0.7	%
DAC Output Temp Variation	T_{REG}	0°C < temp < 70°C		1.4	2	%
VID Input LO					0.4	V
VID Input HI			2			V
VID Input Internal Pull-Up Resistor to 3.3V	VID_R		12.4	16.4	20.4	KΩ

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Power Good Section						
Under-Voltage Lower Trip Point	PG_{UVL}	V_{OUT} Ramping Down	0.88Vs	0.90Vs	0.92Vs	V
Under-Voltage Upper Trip Point	PG_{UVH}	V_{OUT} Ramping Up	0.89Vs	0.91Vs	0.93Vs	V
UV Hysteresis	PG_{HYST}		0.001Vs	0.01Vs	0.02Vs	V
Over-Voltage Upper Trip Point	OV_L	V_{OUT} Ramping Up	1.10Vs	1.11Vs	1.12Vs	V
Over-Voltage Lower Trip Point	OV_H	V_{OUT} Ramping Down	1.09Vs	1.10Vs	1.11Vs	V
OV Hysteresis	OV_{HYST}		0.001Vs	0.01Vs	0.02Vs	V
Power Good Output LO	PG_L	R_L=3mA	0	0.04	0.4	V
Power Good Output HI	PG_H	R_L=5K Pull-Up to 5V	4.8	4.9	5	V
UVLO Threshold - 5V	$UVLO_{5UP}$	Supply Ramping Up	4.2	4.34	4.5	V
UVLO Hysteresis - 5V	$UVLO_{5HYST}$	Supply Ramping Down	0.22	0.32	0.42	V
UVLO Threshold - 12V	$UVLO_{12UP}$	Supply Ramping Up	10.2	10.5	10.8	V
UVLO Hysteresis - 12V	$UVLO_{12HYST}$	Supply Ramping Down	0.5	0.7	0.9	V
Over-Voltage Section						
OVP Threshold	OVP_{TH}	Fault Pin	1.1Vs	1.15Vs	1.2Vs	V
Error Amp Section						
Transconductance	g_m			720		µmho
Input Bias Current	IB_{ERR}	CS1, CS2, CS3	0.5	2.5	5	µA
Input Offset Voltage	VOS_{ERR}	Fb to V_{SET}		3	6	mV
Current Sense Section						
Input Bias Current	IB_{CS}	CS1, CS2, CS3		0.9		µA
Input Offset Voltage	VOS_{CS}	CS1 to CS2, CS1 to CS3		2	4	mV
CS Matching	CS_{MATCH}	Difference between any CS		2	4	mV
Current Limit Section						
OC Threshold Set Current	IB_{OC}	OCSet @ 0V	120	160	200	µA
OC Comp Offset Voltage	VOS_{OC}	OCSet @ OC Threshold	-8	-3	+2	mV
Hiccup Duty Cycle	H_{IC}	Css=0.1uF	1	2.4		%
Soft-Start Section						
Charge Current	I_{SS}	Soft-Start @ 0V	7	10	13	µA
Output Drivers Section						
Rise Time	TR_L TR_H	C_L High Side=3000pF, C_L Low Side=6000pF	25	50	75	ns
Fall Time	TF_L TF_H	C_L High Side=3000pF, C_L Low Side=6000pF	25	50	75	ns
Dead Band	DB_{LH} DB_{HL}	C_L High Side=3000pF, C_L Low Side=6000pF, (Both Measured @ 10%)		130		ns
Oscillator Section						
Osc Frequency per Phase	f_{OSC}	Rt = 50KΩ	100	150	200	KHz
PWM Ramping Voltage	V_{OSC}	Peak to Peak	1.98	2.02	2.06	V
Duty cycle Matching	OSC_{MATCH}	LDrv or HDrv		0.03		%

Note 1: Vs refers to the set point voltage given in Table 1

D4	D3	D2	D1	D0	Vs
1	1	1	1	1	1.075
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450

D4	D3	D2	D1	D0	Vs
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.475
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

Table 1 - Set point voltage (Vs) vs. VID codes.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Rt	This pin programs the oscillator frequency in the range of 50KHz to 500KHz with an external resistor connected from this pin to the ground.
2	Comp	Compensation for error amplifier.
3	Fb	This pin is connected directly to the output of the Core supply to provide feedback to the Error amplifier.
4	SS	This pin provides the soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to the ground which ramps up the outputs of the switching regulator, preventing the outputs from overshooting as well as limiting the input current. The second function of the Soft-Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting.
5 6 7	CS1 CS2 CS3	Current sense feedback for channel 1, 2, 3.
8	Vcc	5V supply voltage.
9	V_{SET}	Output of the DAC.
10	D0	LSB input to the DAC that programs the output voltage. This pin is internally connected to 3.3V by a 16K resistor. This pin can be pulled up externally by a 10K resistor to 5V supply. This pin programs the output voltage in 25mV steps based on the VID table.
11	D1	Input to the DAC that programs the output voltage. This pin is internally connected to 3.3V by a 16K resistor. This pin can be pulled up externally by a 10K resistor to 5V supply.
12	D2	Input to the DAC that programs the output voltage. This pin is internally connected to 3.3V by a 16K resistor. This pin can be pulled up externally by a 10K resistor to 5V supply.
13	D3	Input to the DAC that programs the output voltage. This pin is internally connected to 3.3V by a 16K resistor. This pin can be pulled up externally by a 10K resistor to 5V supply.
14	D4	MSB input to the DAC that programs the output voltage. This pin is internally connected to 3.3V by a 16K resistor. This pin can be pulled up externally by a 10K resistor to 5V supply.

PIN#	PIN SYMBOL	PIN DESCRIPTION
15	Fault	Fault detector. When the output exceeds the OVP trip point, the fault pin switches to 2.8V and pulls down the soft-start.
16	OCSet	This pin is connected to the drain of the synchronous MOSFET in channel 1 of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the over current threshold depending on the $R_{DS(ON)}$ of the power MOSFET.
17 28	Gnd	Analog ground for internal reference and control circuitry. Connect to PGnd with a short trace.
18	SD	Shut down pin. Pulling-up this pin disables the outputs.
19	PGood	Power good pin. This pin is a collector output that switches Low when the output of the converter is not within $\pm$10%(typ) of the nominal output voltage.
20	Ref	2V reference output.
21 31	V_{CH3} V_{CH12}	These pins power the high side MOSFET driver. A minmum 1μF ceramic cap must be connected from these pins to ground to provide peak drive current capability.
22 30 32	HDrv3 HDrv2 HDrv1	Output drivers for the high side power MOSFET.
23 27 34	PGnd3 PGnd2 PGnd1	These pins serve as the ground pins and must be connected directly to the ground plane. A high frequency capacitor (0.1 to 1μF) must be connected from pins V_{CL1}, V_{CL23} and V_{CH3}, V_{CH12} to PGnd1, 2 and 3 for noise free operation.
24 26 35	LDrv3 LDrv2 LDrv1	Output driver for the synchronous power MOSFET.
25 36	V_{CL23} V_{CL1}	These pins are connected to the 12V supply and serves as the power Vcc pin for the low side output drivers. A high frequency capacitor (0.1 to 1μF) must be connected directly from these pins to PGnd1, PGnd2 and PGnd3 pins in order to supply the peak current to the power MOSFET during the transitions.
29	NC	No connection.
33	OCGnd	This pin is connected from the source of the synchronous MOSFET in channal 1 of the Core supply and it provides the reference point for the internal current sensing circuitry.

BLOCK DIAGRAM

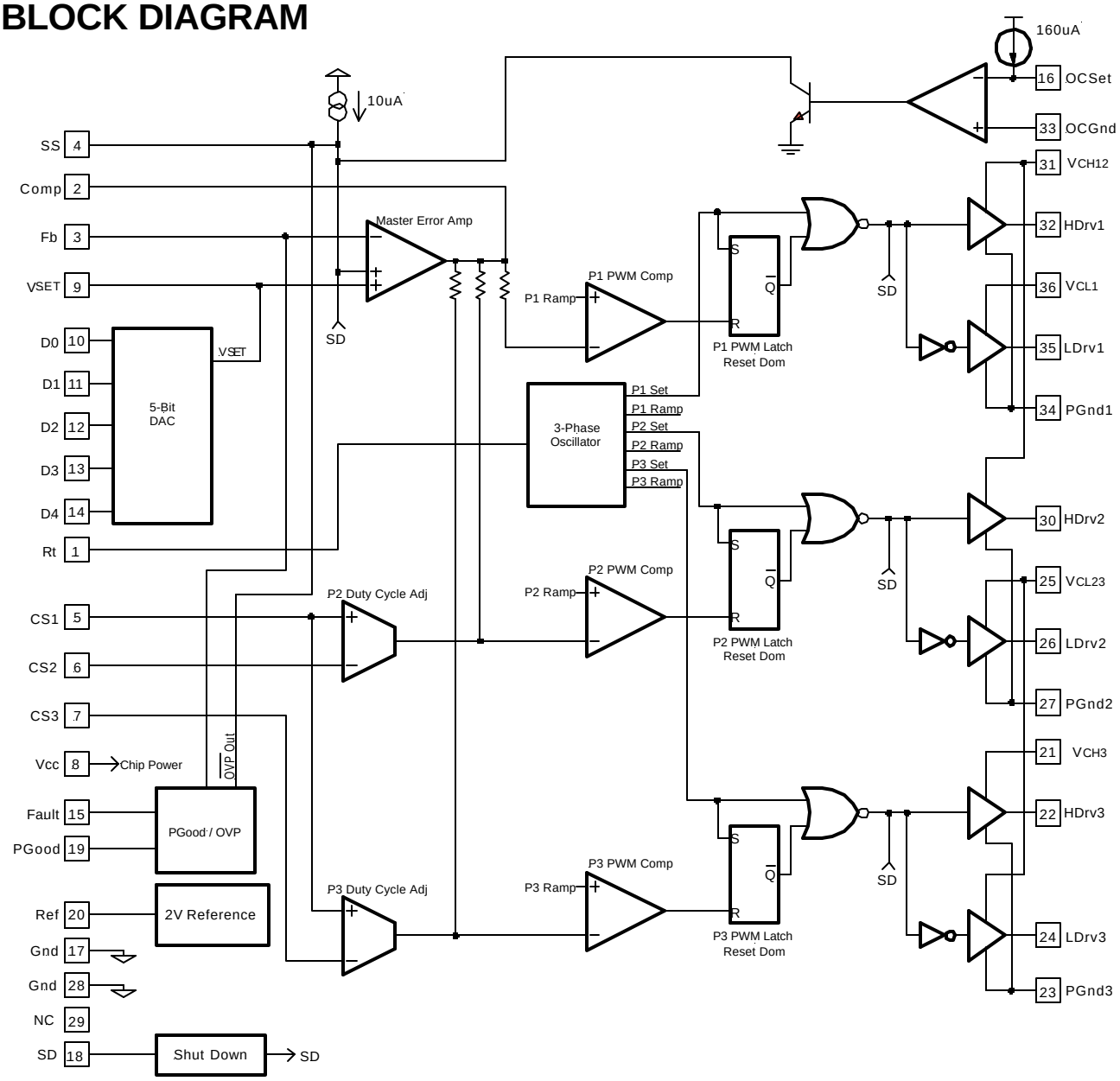


Figure 2 - Simplified block diagram of the IRU3055.

TYPICAL APPLICATION (1)

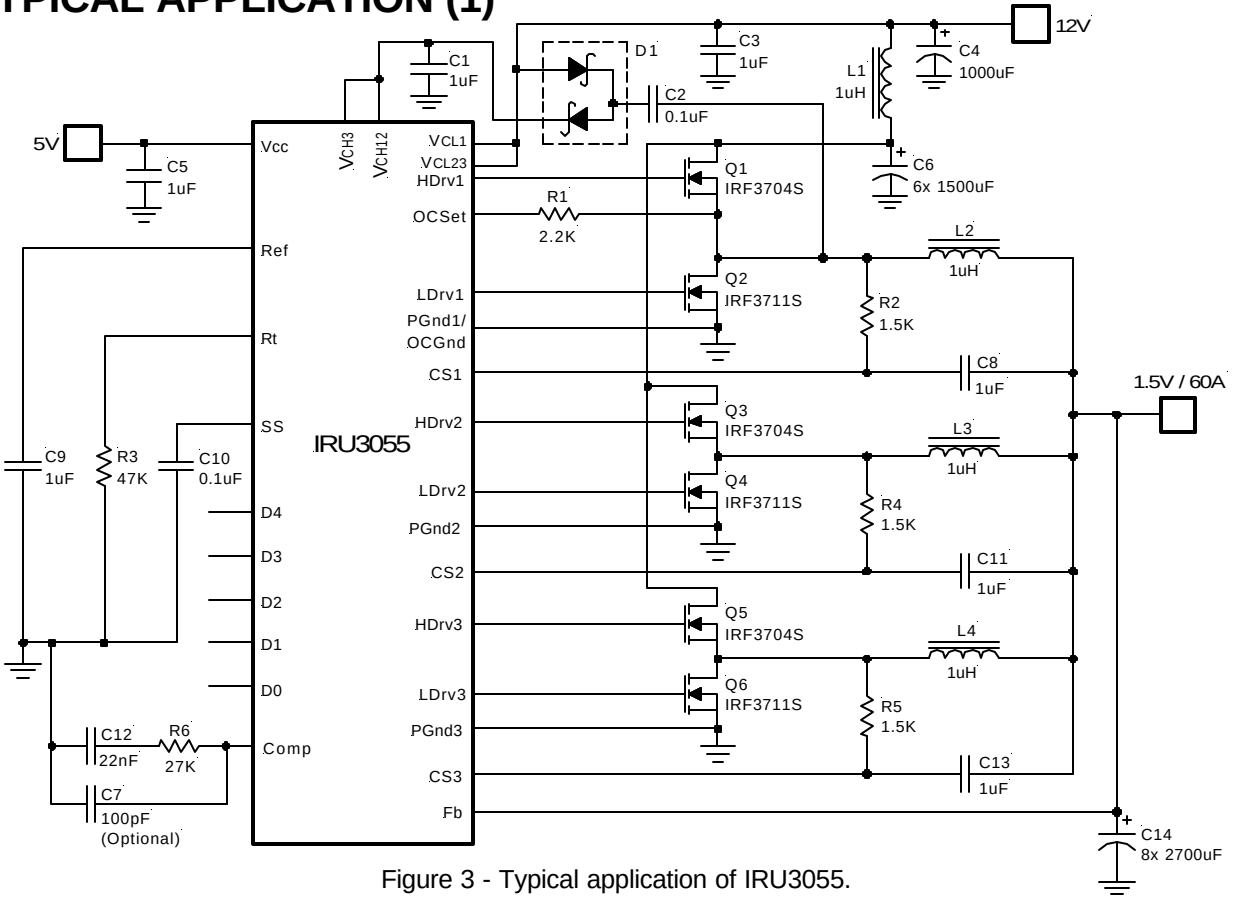


Figure 3 - Typical application of IRU3055.

Parts List

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1,Q3,Q5	MOSFET	20V, 9mΩ	3	IRF3704S	IR	irf.com
Q2,Q4,Q6	MOSFET	20V, 6mΩ	3	IRF3711S	IR	
U1	Controller	Synchronous PWM	1	IRU3055	IR	
D1	Schottky Diode	In Series	1	BAT54S	IR	
L1	Inductor	1μH	1	Z9479-A	Coilcraft	coilcraft.com
L2,L3,L4	Inductor	1μH	3	T60-18 Core, 6-turns #14 AWG wire		
C1	Cap, Ceramic	1μF, X7R, 25V	1	ECJ-3YB1E105K	Panosonic	maco.panasonic.co.jp
C2,C10	Cap, Ceramic	0.1μF, Y5V, 25V	2	ECJ-2VF1E104Z	Panosonic	
C3,C5,C9, C8,C11,C13	Cap, Ceramic	1μF, Y5V, 16V	6	ECJ-3VF1C105Z	Panosonic	
C4	Cap,Electrolytic	1000μF, 16V	1		Any	
C6	Cap,Electrolytic	1500μF, 16V	6	EEU-FJ1C152U	Panosonic	maco.panasonic.co.jp
C7	Cap (Optional)	100pF, X7R, 50V	1	ECU-V1H101KBN	Panosonic	
C12	Cap, Ceramic	22nF, X7R, 50V	1	ECU-V1H223KBG	Panosonic	
C14	Cap,Electrolytic	2700μF,6.3V,13mΩ	8	EEU-FJ0J272U	Panosonic	
R1	Resistor	2.2K, 1%	1		Any	
R2,R4,R5	Resistor	1.5K, 1%	3		Any	
R3	Resistor	47K, 1%	1		Any	
R6	Resistor	27K, 1%	1		Any	

APPLICATION INFORMATION

Constant Switching Frequency 3-Phase Controller

IRU3055 is a 3-phase buck converter controller. For high current applications, multiple converters are usually connected in parallel to reduce the power capability for each individual converter as well as alleviate the thermal stress on each of the power devices. These individual converters share a common output, but may have different input sources. Each individual converter operates at the same switching frequency but at a different phase. As a result, the effective input current and output current ripple are much smaller compared with a single-phase converter. Another benefit will be faster dynamic load responses.

The block diagram of IRU3055 is shown in Figure 2. The 3-phase oscillator provides a constant frequency and the three PWMs ramp signals with 120 degree phase shift. The three comparators and three PWM latches will generate three PWM outputs to the drivers which are built inside the IC. A typical 3-phase PWM signal is shown in Figure 4.

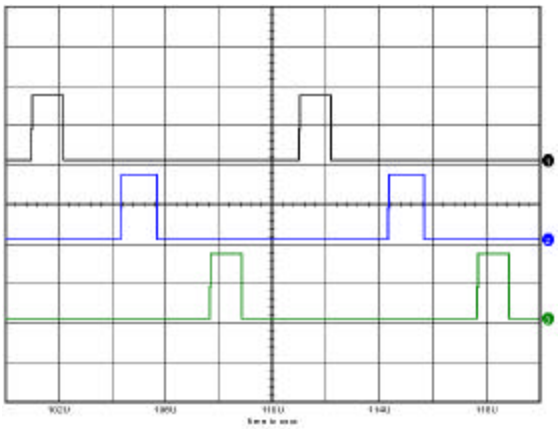


Figure 4 - The 3-phase PWM signal.

Voltage and Current Loop

IRU3055 has three transconductance error amplifiers. The master Error amplifier is used to regulate the output voltage. The output voltage can connect directly, or through a resistor divider, to the Fb pin of the error amplifier. The compensation network at the output of the amplifier (Comp Pin) helps to stabilize the voltage loop. The non-inverting pin of the master amplifier is connected to the output of the DAC which interfaces with the micro processor core and determines the desired output voltage. Two additional transconductance amplifiers are used to balance the output inductor current among 3-phases.

Output Current Ripple Reduction

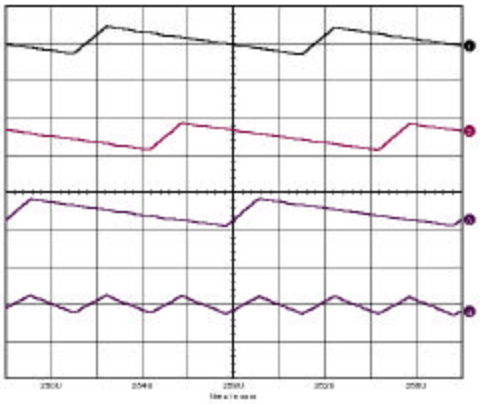


Figure 5 - Output inductor currents and output capacitor ripple current.

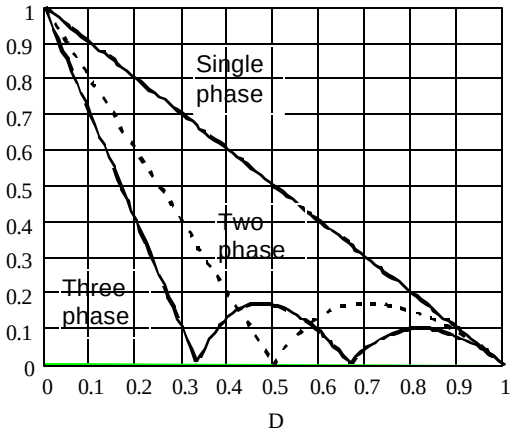


Figure 6 - Normalized output current across output capacitor.
(Peak to peak current normalized to the Vo/(L × Fs)).

One of advantages of the multi-phase converter is that the output current ripple is significantly reduced. The current from multiple converters tend to cancel each other so that the total output current flowing into the output capacitor is reduced. In this case, the output inductor in each individual buck converter can be selected smaller to improve the load transient response without sacrificing the output current ripple. Figure 5 shows a 3-phase inductor current and current ripple in the capacitor for 12V input 1.5V, 50A, 3-phase buck converter. The effective output ripple has three times frequency and a smaller amplitude compared with each individual converter. Figure 6 indicates the total ripple current, as a function of duty cycle, normalized to the parameter Vo/(L × Fs) at zero duty cycle.

It is shown that the output current ripple is greatly reduced by multi-phase operation. At the certain duty cycle D=1/m, where m is the phase number, the output ripple will be near zero due to complete cancelation of inductor current ripple. The optimum number of phases exists for different applications.

Output Inductor Current Sensing

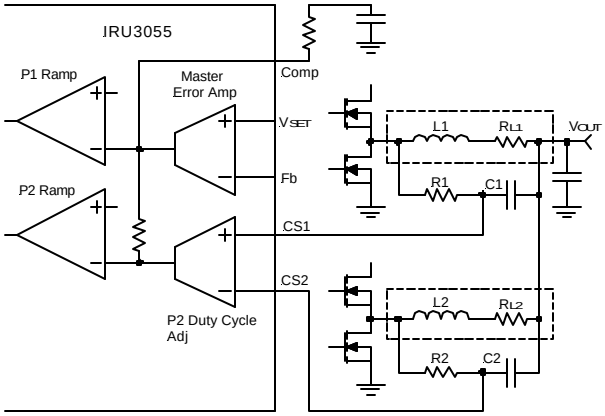


Figure 7 - Loss-less inductive current sensing and current sharing.

The loss-less sensing current is achieved by sensing the voltage across the inductor. In Figure 7, L1 and L2 are inductors. R_{L1} and R_{L2} are inherent inductor resistance. The resistor R1 and capacitor C1 are used to sense the average inductor current. The voltage across the capacitors C1 and C2 represent the average current flowing into resistance R_{L1} and R_{L2}. The time constant of the RC network should be equal or at most three times larger than the time constant L/R_L.

$$R1 \times C1 = (1\sim3) \times \frac{L}{R_L} \qquad \text{---(1)}$$

In order to minimize the effect of the bias current in IRU3055, the sensing resistor should be as small as possible. However, a small resistor will result in high power dissipation and a high value capacitor, a trade off has to be chosen. Typically, a 1µF ceramic capacitor is a good start. In the Application Circuit (1), L=1µH and R_L=1.6mΩ. The sensing resistor and capacitor is chosen as:

R1= 1.5K and C1= 1µF

The voltage across the sensing capacitors are sent to the pins CS1 and CS2. Suppose the inductor current in the inductor L2 is smaller than in inductor L1 and the voltage across capacitor C1 will be greater than that across C2. The transconductance amplifier in IRU3055 will generate a positive current flowing into node Comp. Through an internal resistor, there will be an additional voltage drop above the node Comp and then the voltage sent to the PWM comparator will be higher and the generated duty cycle for phase-2 will be larger. As a result, the inductor (L2) current will go up until the current balance is achieved. For accurate current sharing, the current sense from each inductor should be as symmetrical as possible. The layout is critical and the layout of the RC network should be as follows:

Connect the node from Resistor R1 (or R2) directly to the pad of inductor. Connect the other node of capacitor C1 and C2 together and connect to the output voltage terminal. In this case, the voltage at node C1 and C2 will have a common reference voltage that is output voltage. If the inductor inherent resistance as well as PCB trace are almost identical or symmetrical, almost perfect current sharing can be obtained. The PCB connection from three inductors to the output capacitor should have the same length and width. The feedback point from the output should be located such that the effect impedances from the three inductors to the output feedback sensing point are almost symmetrical or identical so that the noise will cancel each other. The current sharing accuracy is dependent upon the mismatch among the values of current sensing components and the current amplifier offset. It is recommended that all the inductors be from the same manufacturer and also be the same model so that mismatch will be minimized and the cost reduced. In most cases, with a good layout, the difference between 3-channel currents can be limited to be below 2A.

Operation of IRU3055

Over Current Protection

The IRU3055 senses the MOSFET switching current to achieve the over current protection. The diagram is shown in Figure 8. A resistor (R_{SET}) is connected between pin OCSet and the drain of the low side MOSFET for phase1. Inside the IC, there is an internal 160µA current source connected to OCSet pin. When the upper switch is turned off, the inductor current flows through the low side switch. The voltage at OCSet pin is given as:

$$V_{OCSet} = 160\mu A \times R_{SET} - R_{DS(ON)} \times i_{L1} \qquad \text{---(2)}$$

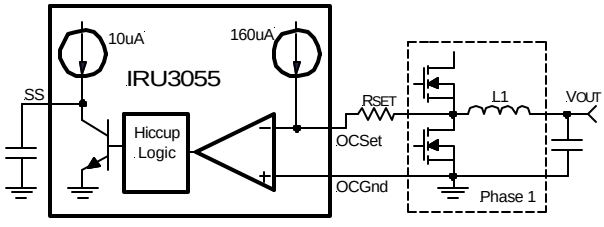


Figure 8 - Diagram of the over current sensing.

When the inductor current is large enough, the voltage across the low side switch is low enough so that the voltage at OCSet node is below zero and the comparator will flip and trigger a switch to discharge the soft-start capacitor at a certain slope rate. The system enters into a hiccup mode. The over current threshold can be set by resistor R_{SET}. Suppose the current sharing is perfect, then the current flowing into phase 1 will be one third of the total output current. The maximum allowed output current can be represented as:

$$I_{MAX} = 160\mu A \times R_{SET} / (R_{DS(ON)}/3)$$

$$R_{SET} = I_{MAX} \times R_{DS(ON)}/3/160\mu A \quad ---(3)$$

Where $R_{DS(ON)}$ is the ON resistance of low side MOSFET. In practice, the $R_{DS(ON)}$ of MOSFET is temperature dependent. The overhead has to be considered. For practice, over current threshold has to be at least 50% higher than the nominal current plus ripple. In the demo-board, the maximum output current is set to be:

$$I_{MAX} = (1+50\%) \times I_{OUT} = 1.5 \times 60A = 90A$$

Consider ripple current, select I_{MAX}=100A

For each phase, the maximum current is one third (33A), assuming good current sharing. The low side of MOSFET is IRF3711S. The On resistor at 150 degrees is given from the data sheet:

$$R_{DS(ON)} = 1.5 \times 6m\Omega = 9m\Omega$$

The over current setting resistor can be set as

$$R_{SET} = 33A \times 0.009/160\mu A = 1.86K$$

Select R_{SET} = 2.2K

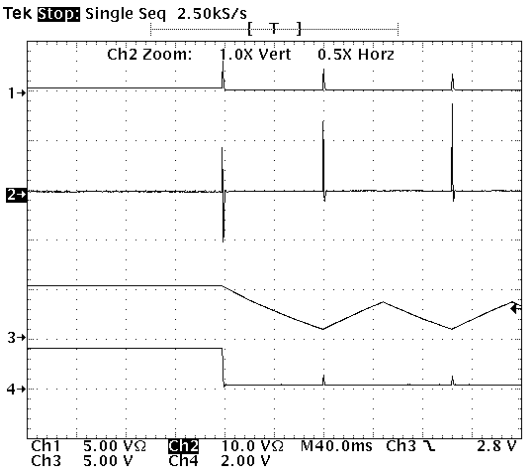


Figure 9 - Operation waveforms at short circuit. (Hiccup mode)

Ch1: Input current, 5A/div.
Ch2: Phase 1 inductor current, 10A/div.
Ch3: Soft-start capacitor voltage, 5V/div.
Ch4: Output voltage, 2V/div.

Over Voltage Protection

The Fb pin is connected to the output voltage. An overvoltage condition is detected when the voltage at Fb pin is 15% higher than the programmed voltage by DAC. When the overvoltage occurs, the soft-start capacitor is discharged. The high side MOSFETs are turned off and the low side MOSFETs are turned on. As a result, the low side MOSFET of synchronous rectifier conduct and shunt the output voltage to ground and protect the load. In the meantime, the PGood pin is held to low.

Soft-Start

The IRU3055 has a soft-start function to limit the current surge at the start-up. An external capacitor which is charged by a 10μA internal current source is used to program the soft-start timing. The voltage of the external capacitor linearly increases, which forces the output voltage to go up linearly until the voltage at soft-start reaches the desired voltage. The following equation can be used to calculate the start up time.

$$10\mu A \times t_{START}/Css = V_{SET}+0.7V$$

$$t_{START} = (V_{SET}+0.7V) \times Css/10\mu A \quad ---(4)$$

Where:

Css is the soft-start capacitor (μF).

V_{SET} is the voltage from DAC and equal to the desired output voltage.

For a 7.5ms start-up time and 1.5V output, the required capacitor will be 33nF.

Operation Frequency Selection

The operation switching frequency is determined by an external resistor (Rt). The switching frequency is approximately inversely proportioned to resistance (see Fig.10). The switching frequency can also be estimated by:

$$Fs \cong 7500/Rt \quad ---(5)$$

Where Rt is in KΩ and Fs is in KHz.

For example, if the 150KHz switching frequency is selected, the required Rt is calculated as:

$$Rt \cong 7500/150 = 50K\Omega$$

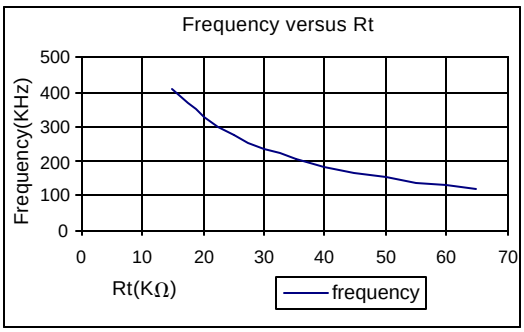


Figure 10 - The operation frequency vs. Rt.

Synchronous-Rectifier Driver

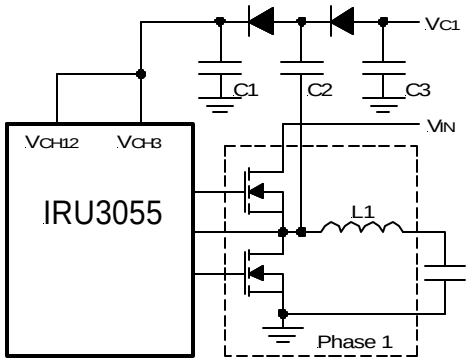


Figure 11 - Supply V_{CH12}, V_{CH3} with charge bump configuration.

Synchronous rectification reduces conduction losses in the rectifier by shunting the normal Schottky diode or MOSFET body diode with a low on-resistance MOSFET switch. The synchronous rectification also ensures good transient dynamic. For IRU3055, the 3-phase synchronous rectifier MOSFET drivers are built inside. To drive the high-side MOSFET, it is necessary to supply a gate voltage at least 4V greater than the bus voltage. In IRU3055, the driver supply voltage for high side MOSFET driver is supplied through the V_{CH12} and V_{CH3} pins. If the input voltage for DC-DC converter is 5V, the V_{CH12} and V_{CH3} pins can be connected to 12V or supplied by using charge pump configuration as shown in Figure 11.

If the voltage Vc1 and V_{IN} in Figure 11 is connected to input voltage 12V, the voltage at V_{CH12} and V_{CH3} pins are charged up to almost twice the input voltage. The high side driver can be enabled. A capacitor in the range of 0.1µF to 1µF is generally adequate for capacitor C2. For high current applications, a large ceramic capacitor such as 2.2µF is recommended. The diode can be a Schottky diode such as BAT54S.

With the charge bump configuration, shown in Figure 11, the voltage at pins V_{CH12} and V_{CH3} can be boosted up. When the low side MOSFET is on, the capacitor C2 is charged to voltage Vc1. When the high side MOSFET is ON, the energy in the capacitor C2 is discharged to the bypass capacitor C1 next to pins V_{CH12} and V_{CH3}. The voltage at V_{CH12} and V_{CH3} pins is approximately the sum of the voltage Vc1 and V_{IN}. The high side driver signal should be at least 4V higher than the input voltage (V_{IN}). The voltage Vc1 has to be 5V or higher. For the demo-board, Vc1 is equal to input voltage (V_{IN}=12V). If the low power dissipation of IC is preferred, especially at higher frequency, Vc1 can be connected to 5V instead.

Component Selection Guide

Output Inductor Selection

The inductor is selected based on the inductor current ripple, operation frequency and efficiency consideration. In general, a large inductor results in small output ripple and higher efficiency but big size. A small value inductor causes large current ripple and poor efficiency but small size. Generally, the inductor is selected based on the output current ripple. The optimum point is usually found between 20% and 50% ripple of output inductor current. For each phase synchronous buck converter, the output peak-to-peak current ripple is given by:

$$\Delta i_{(PEAK - PEAK)} = (V_{IN}-V_{OUT}) \times V_{OUT}/(L \times Fs \times V_{IN}) \quad ---(6)$$

Assuming the output current is evenly distributed in each phase, we can define the ratio of the ripple current and nominal output current as:

$$LIR = \Delta i_{(PEAK - PEAK)} / I_{OUT} / m$$

Where LIR is typically between 20% to 50% and m is the phase number. In this case m=3. Then the inductor can be selected by:

$$L > V_{OUT} \times (V_{IN}-V_{OUT})/(Fs \times V_{IN} \times LIR \times I_{OUT}/m) \quad ---(7)$$

For example, in the application circuit, the ripple is selected as LIR=40%, the inductor is selected as:

$$L > 1.5 \times (12-1.5)/(150K \times 12 \times 40\% \times 60A/3) = 1.1\mu H$$

Select L=1µH

The RMS current of the inductor will be approximately equal to average current:

$$I_{OUT}/m = 60/3 = 20A.$$

The peak inductor current is about:

$$I_{L(PEAK)} = (1+LIR/2) \times I_{OUT}/m = 1.2 \times 20 = 24A$$

Output capacitor selection

The voltage rating of the output capacitor is the same as output voltage. Typical available capacitors on the market are electrolytic, tantalum and ceramic. If electrolytic or tantalum capacitors are employed, the criteria is normally based on the value of Effective Series Resistance (ESR) of total output capacitor. In most cases, the ESR of the output capacitor is calculated based on the following relationship:

$$ESR < \Delta V/\Delta i \quad ---(8)$$

Where ΔV is the maximum allowed output voltage drop during the transient and Δi is the maximum output current variation. In the worst case, Δi is the maximum output current minus zero.

Power MOSFET Selection

The IRU3055 is a controller for 3-phase synchronous buck converter. For each phase, the average inductor current will be one third of the total output current in an ideal case, which will greatly alleviate the thermal management for power switch. In general, the MOSFET selection criteria depends on the maximum drain-source voltage, RMS current and ON resistance ($R_{DS(ON)}$). For both high side and low side MOSFET, a drain-source voltage rating higher than maximum input voltage is necessary. In the demo-board, 20V rating should be satisfied. The gate drive requirement for each MOSFET is almost the same. If logic-level MOSFET is used, some caution should be taken with devices at very low VGS to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through circuit.

If output inductor current ripple is neglected, the RMS current of high side switch is given by:

$$I_{RMS(HI)} = \sqrt{D} \times I_{OUT}/m$$

$$I_{RMS(HI)} = \sqrt{(V_{OUT}/V_{IN})} \times I_{OUT}/m \quad \text{---(9)}$$

The RMS current of low side switch is given as:

$$I_{RMS(LO)} = \sqrt{(1 - D)} \times I_{OUT}/m$$

$$I_{RMS(LO)} = \sqrt{(1 - V_{OUT}/V_{IN})} \times I_{OUT}/m$$

In the demo board, RMS current of high side switch is:

$$I_{RMS(HI)} = \sqrt{(1.5/12)} \times 60/3 = 7.1A$$

RMS current of low side switch is:

$$I_{RMS(LO)} = \sqrt{(1 - 1.5/12)} \times 60/3 = 18.7A$$

For $R_{DS(ON)}$ of MOSFET, it should be as small as possible in order to get highest efficiency. The MOSFET from International rectifier IRF3704S with a $R_{DS(ON)}$=9mΩ, 20V drain source voltage rating and 77A I_D is selected for high side MOSFET.

For a high input and low output case, the low side switch conducts most of output current and handles most of the thermal management. Two MOSFETs can be put in parallel to further reduce the effect $R_{DS(ON)}$ and conduction losses. In the demo-board, MOSFET from International Rectifier IRF3711S with $R_{DS(ON)}$=6mΩ, 20V V_{DS} and 110A I_D is selected as synchronous MOSFET. The power dissipation includes conduction loss and switching loss.

The conduction loss for high side switch in each phase can be estimated by the following equation:

$$P_{CON(HI)} = R_{DS(ON)} \times q \times (I_{OUT}/m) \times (I_{OUT}/m) \times (V_{OUT}/V_{IN})$$

The low side switch power dissipation is:

$$P_{CON(LO)} = R_{DS(ON)} \times q \times (I_{OUT}/m) \times (I_{OUT}/m) \times (1\text{-}V_{OUT}/V_{IN})$$

Where q is the temperature coefficient of ON resistor of MOSFET $R_{DS(ON)}$ and can be found in MOSFET data sheet (typically between 1 and 2).

In this example, the MOSFET IRF3704S is chosen to be the high side switch with:

$R_{DS(ON)}$ = 9mΩ
q = 1.5 @ 150°C

The conduction loss for high side MOSFET is given as:

$$P_{CON(HI)} = 9m\Omega \times 1.5 \times (60/3) \times (60/3) \times 1.5/12 = 0.68W$$

Low side switch is configured with one IRF3711 with 6mΩ $R_{DS(ON)}$. The conduction loss is calculated as:

$$P_{CON(LO)} = 6m\Omega \times 1.5 \times (60/3) \times (60/3) \times (1\text{-}1.5/12)$$
$$P_{CON(LO)} = 3.15W$$

The switching loss for MOSFET is more difficult to calculate due to effect of the parasitic components, etc. The switching loss can be estimated by the following equation:

$$P_{SW} = V_{DS(OFF)} \times (tr+tf) \times F_S \times I_{SW}/2$$

Where:
$V_{DS(OFF)}$ is the Drain to Source voltage when switch is turned off.
tr is the rising time.
tf is the fall time.
F_S is the switching frequency.
I_{SW} is the current in MOSFET when MOSFET is turned off. It can be estimated by:

I_{SW} = I_{LOAD}/m + half of the ripple current

In this example, for low side MOSFET, the body diode is turned on before MOSFET is on. Therefore, the switching losses for low side MOSFET is almost zero due to zero voltage switching. For high side MOSFET, from data sheet, we have:

tr = 50ns
tf = 50ns
Select F_S = 150KHz
$V_{DS(OFF)}$ = 12V
I_{SW} = Peak Inductor Current = 24A
$P_{SW(HI)} = 12V \times (50ns+50ns) \times 150KHz \times 24A/2$
$P_{SW(HI)}$ = 2.1W

The total power dissipation is:

$P_{D(HI)} = P_{CON(HI)} + P_{SW(HI)}$
$P_{D(HI)}$ = 0.68W+2.16W = 2.84W
$P_{D(LO)} \cong P_{CON(LO)}$ = 3.15W

Heat Sink Selection

The criteria of selecting heat sink is based on the maximum allowable junction temperature of the MOSFETs. That is:

$$T_A + P_D \times (R_{\theta JC}+R_{\theta CS}+R_{\theta SA}) < T_{J(MAX)}$$

Where:

T_A = The Ambient Temperature

P_D = Power Dissipation of each MOSFET

$R_{\theta JC}$ = The Thermal Resistance from junction to case

$R_{\theta CS}$ = the thermal resistance from case to heat sink

$R_{\theta SA}$ = the heat-sink-to-air thermal resistance

$T_{J(MAX)}$ = maximum allowable junction temperature of MOSFET, for example 150°C.

The maximum heat-sink-to-air thermal resistance is calculated as:

$$R_{\theta SA} < (T_{J(MAX)}-T_A)/P_D-R_{\theta JC}+R_{\theta CS}$$

In this example, the MOSFET is mounted in the PCB board with more than 1" square PCB board. Therefore, the junction temperature for MOSFET can be calculated as:

$$T_J = T_A + P_D \times R_{\theta JA}$$

Where $R_{\theta JA}$ is the junction-to-ambient thermal resistance with MOSFET on 1" square PCB board and it is available from MOSFET data sheet.

For MOSFET IRF3704S with D2 package, $R_{\theta JA}$ = 40°C/W. Assume ambient temperature is T_A=35°C. For high side MOSFET, the junction temperature is given as:

$$35°C + 2.84W \times 40°C/W = 149°C$$

For low side MOSFET, IRF3711s, the maximum junction temperature can be calculated as:

$$35°C + 3.15W \times 40°C/W = 161°C$$

This is the worst case. For conservative consideration, two IRF3711 can be put in parallel.

Input Filter Selection

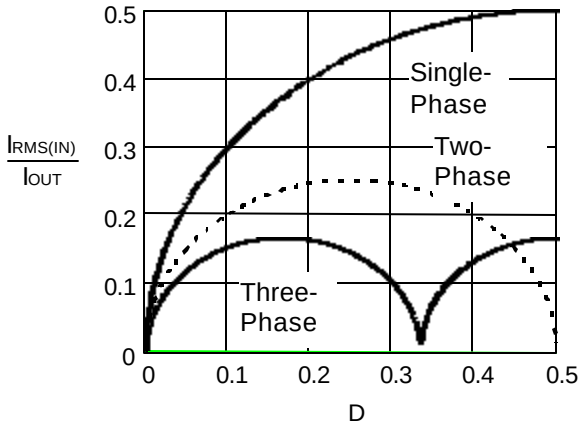


Figure 12 - Normalized input RMS current vs. duty cycle.

The selection criteria of input capacitor are voltage rating and the RMS current rating. For conservative consideration, the capacitor voltage rating should be 1.5 times higher than the maximum input voltage. The RMS current rating of the input capacitor for multi-phase converter can be estimated from the above Figure 12.

First, determine the duty cycle of the converter (V_O/V_{IN}). The ratio of input RMS current over output current can be obtained. Then the total input RMS current can be calculated. From this figure, it is obvious that a multi-phase converter can have a much smaller input RMS current, which results in a lower amount of input capacitors that are required.

For high current applications, multiple bulk input capacitors in parallel may be necessary. Some electrolytic capacitors, such as Panasonic HFQ series, Sanyo MV-WX or equivalent may be put in parallel to provide a large current. In addition, ceramic bypass capacitors for high frequency de-coupling are recommended. Furthermore, some small ceramic capacitors should be put very close to the drain of the high side MOSFET and source of the low side switch to suppress the voltage spike caused by parasitic circuit parameters.

For high current applications, a 1µH input inductor is recommended to slow down the input current transient.

Design Example

In the demo-board, the condition is as follows:

V_{IN}=12V, V_{OUT}=1.5V and I_{OUT}=60A

Output voltage regulation is within 100mV during transient.

(1) Select Switching Frequency

Fs = 150KHz for each phase

According to Figure 10 and equation (5), the oscillator selection resistor is given by:

$Rt \cong 7500/150 = 50K$

From Figure 10, select Rt=47K

(2) Soft-Start Capacitor

For 1.5V output, V_{SET}=1.5V. The soft-start time of the converter can be estimated from equation (4):

$t_{START} = (V_{SET}+0.7V) \times Css/10\mu A$

If t_{START}=20ms, then:

$Css = 20ms \times 10\mu A/(1.5V+0.7V) = 95nF$

Choose Css=0.1μF

(3) Output Inductor and Capacitor

Select the current ripple LIR=40%, by equation (7):

$L>V_{OUT} \times (V_{IN}-V_{OUT})/(Fs \times V_{IN} \times LIR \times I_{OUT}/m)$

$L>1.5 \times (12-1.5)/(150K \times 12 \times 40\% \times 60A/3)=1.1\mu H$

Select core from Micrometal, T60-18 with 6 turns #14 AWG wire, which gives 1μH inductor, 15A RMS and 25A saturation current. The DC resistor of inductor is 1.6mΩ.

$L = 1\mu H$ and $R_L = 1.6m\Omega$

The output capacitor is based on ESR. Suppose the maximum allowed voltage droop for 60A load is:

$\Delta V = 100mV$

$ESR < \Delta V/\Delta i = 100mV/60A = 1.66m\Omega$

Select 8 Panasonic capacitors. EEUFJ0J272U with 2700μF and 13mΩ ESR each. The total:

$C_{OUT} = 8 \times 2700\mu F = 21600\mu F$

$ESR = 13m\Omega/8 = 1.6m\Omega$

(4) Senseless Inductor Current Sensing

With equation (1), we select the inductor sensing network which has a time constant:

$R2 \times C8 = 2 \times L/R_L$

Select: C8 = 1μF

$R2 = 2 \times 1\mu H/(1.6m\Omega \times 1uF) = 1.25K$

Select R2, R4 and R5 = 1.5K

(5) MOSFET Selection

By equation (9), the RMS current of high side MOSFET is given as:

$I_{RMS(HI)} = \sqrt{D} \times I_{OUT}/m$

$I_{RMS(HI)} = \sqrt{(V_{OUT}/V_{IN})} \times I_{OUT}/m$

$D = 1.5/12 = 0.125$

$I_{RMS} = \sqrt{0.125} \times 60A/3 = 7.1A$

Select MOSFET from International Rectifier IRF3704S with D-2 pak, which will result to:

$R_{RDS(ON)} = 9m\Omega$ and 110A I_{DS} current

For low side MOSFET:

$I_{RMS(LO)} = \sqrt{(1-D)} \times I_{OUT}/m$

$D = V_{OUT}/V_{IN} = 1.5/12 = 0.125$

$I_{RMS(LO)} = \sqrt{(1-0.125)} \times 60/3 = 19A$

Select MOSFET from International Rectifier IRF3711S with D-2 package, which will result to:

$R_{DS(ON)(LO)} = 6m\Omega$ and 110A current

(6) Over Current Setting

By equation (3), over current limit is set by R_{SET}. The current limit should be at least 150% of the nominal output current. Set I_{MAX}=90A and 30A for each phase. For low side MOSFET, $R_{DS(ON)}$=6mΩ and 9mΩ at 150°C. The over current setting resistor is given by:

$R_{SET} = I_{MAX} \times R_{DS(ON)}/3/160\mu A$

$R_{SET} = 90A \times 9m\Omega/3/160\mu A = 1.7K\Omega$

Select $R_{SET} = 2.2K\Omega$

(7) Compensation Design

For detailed explanation, please see IRU3037 data sheet. Select bandwidth of the system to be 1/10 of switching frequency that is 15KHz:

$Fo = 2 \times 3.14 \times 15KHz = 94KHz$

The compensation resistor can be calculated as:

$Rc = Vosc \times Fo \times L/(V_{IN} \times ESR \times g_m)$

Where Vosc is the ramp peak voltage and g_m is the transconductance of the error amplifier. From the data sheet:

Vosc = 2V

$g_m = 720\mu mho$

$Rc = 2 \times 94KHz \times 1\mu H/(12 \times 1.6m\Omega \times 720\mu mho)$

$Rc = 12K\Omega$. Select R6=Rc=12.7KΩ

The compensator capacitor is given as:

$Cc = \sqrt{(L \times C_{OUT})} /0.75/Rc$

$Cc = \sqrt{(1\mu H \times 21600\mu F)} /0.75/12K\Omega = 16.3nF$

Select C12=Cc=22nF

In practice, the resistor Rc (R6 in Fig.3) can be tuned for a better dynamic load response. Higher Rc will result in a fast transient response. Cc (C12 in Fig.3) can be kept unchanged. In Fig.3. R6=27KΩ.

(8) Input Capacitor Selection

From the Figure 12, according to the duty ratio, pick up the normalized input RMS current. For this example:

$I_{RMS(IN)}/I_{OUT} = 0.15$

$I_{RMS(IN)} = 0.15 \times 60A = 9A$

Select Panosonic capacitor. Four EEUFJ1C152U with1500μF give results to:

$4 \times 2.5 = 10A$ RMS current.

Layout Considerations

For any switching converter, the current transition from one power device to another usually causes voltage spikes across the power component due to parasitic inductance and capacitance. These voltage spikes will result in reduction of efficiency, increased voltage stress of power components and radiated noise to circuit. A good layout can minimize these effects.

There are several critical loops for IRU3055 controlled multi-phase converter. The loop by synchronous MOSFETs and input capacitor is the most critical loop and it should be minimized as small as possible. Put a small ceramic capacitor next to the drain of high side switch and source of low side switch. Put the input capacitors to the high and low side switch as close as possible. The second loop is the gate of MOSFETs and the drivers from IRU3055. Because the IRU3055 includes the MOSFETs drivers inside, the signal path between driver to the gate of MOSFETs should be minimized. The trace should handle 1A transient current ability.

The following is a guideline of how to place the critical components and the connections between components in order to minimize the switching noises.

Start the layout by first placing the power components:

(1) Place the high side MOSFET Q1 and low side MOSFET Q2 as close to each other as possible so that the source of Q1 and drain of Q2 has the most possible shortest length.

(2) Place a capacitor (Electrolytic or ceramic or both) close to the drain of Q1 and source of Q2.

(3). If needed, place a snubber RC circuit next to Q2.

(4). Place the other 2-phase Q3, Q4 and Q5, Q6 following the same rule.

(5) Place output inductor Lo1, Lo2, Lo3 and output capacitor C_{OUT}. Make sure the output capacitors are evenly distributed among 3-phases and close to the output slot.

(6) Place IC IRU3055 such that the driver pins, HDrv1, HDrv2, Hdrv3 and LDrv1, LDrv2, LDrv3, have a relatively short distance from the corresponding MOSFET gate. In addition, make the 3-phase driving signal path as symmetrical as possible. If the length of the gate signal path is more than 1cm long, a 2 to 10Ω gate resistor is recommended to be in series in the gate signal path.

(7) Place bypass capacitor close to Vcc pin, V_{REF} pin and V_{CH12},V_{CH3} pins and also soft-start capacitor to SS pin.

(8) Place a frequency selection resistor (Rt) close to Rt pin.

(9) Connect output inductor current sensing network such as R2, C8 close to IRU3055. One example of the layout is shown as follows:

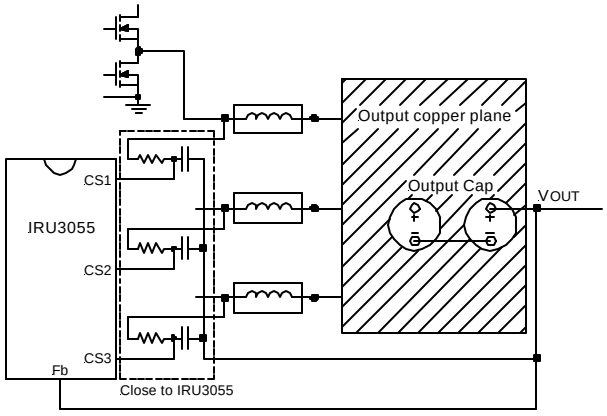


Figure 13 - An example of layout connection for inductor current sensing.

Connect current sensing resistors Rs1,Rs2,Rs3 right to the pads of output inductor Lo1,Lo2,Lo3. Connect the other node of current sensing capacitors Cs1,Cs2,Cs3 together and directly connect to the output voltage terminal, which is also the sensing point for output voltage feedback sensing.

(10) Place feedback resistors (R_{FB1} and R_{FB2}) close to IC and place compensator network close to Comp pin. Note that the resistor R_{FB1} and R_{FB2}, can be used to set the outputs slightly higher to account for the output drop at the load due to the trace resistance.

Component Connection

• No data bus should be passing through the switching regulator especially close to the fast transition nodes such as PWM drivers or the inductor voltage.

• If possible, using four layer board, dedicate one layer to ground, another layer as power layer for the constant power input and output such as 5V, 12V, and 1.5V output. Connect all grounds to the ground plane using direct vias to the ground plane.

• Use large and low impedance/low inductance PCB plane to connect the high current path connections either using component side or the solder side. These connections include:

(a) Input capacitor to the drain of high side MOSFET Q1, Q3 and Q5.

(b) The interconnection between source of high side MOSFET such as Q1 and low side MOSFET such as Q2.

(c) From drain of low side MOSFET to output Inductor .

(d) From output inductor to output capacitor. Make sure the impedance from output inductor to output voltage slot (also the voltage feedback sensing point) are as identical or symmetrical as possible.

(e) From each output capacitor to output slot.

(f) From input inductor to input capacitor.

Connect the rest of the components using the shortest trace possible.

TEST WAVEFORMS FOR TYPICAL APPLICATION (1)

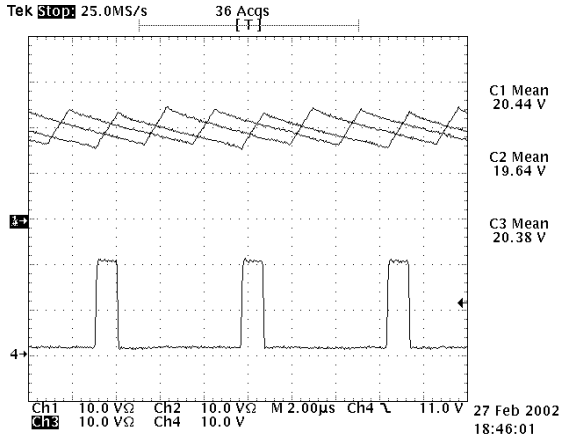


Figure 14 - 3-Phase inductor current at 60A load, Ch1, Ch2 and Ch3: 10A/div. Ch4: gate signal.

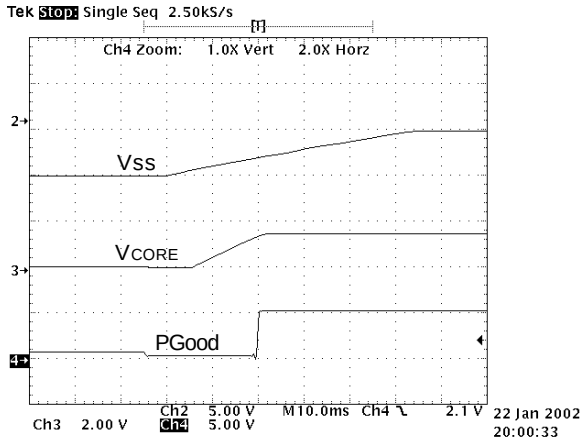


Figure 15 - Soft-start, Vcore and PGood.

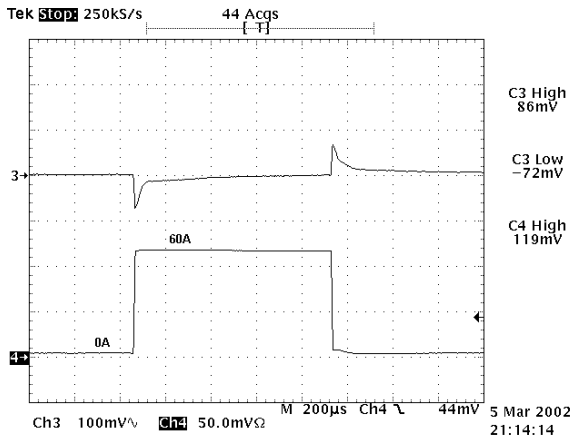


Figure 16 - 60A Dynamic load response with 20A/µs slew rate.
Ch3: Output voltage, 100mV/div, AC.
Ch4: Load current, 20A/us, sensed by 2mΩ resistor, 25A/div.

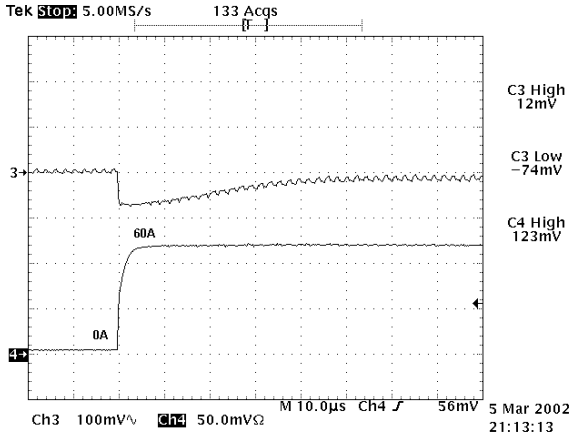


Figure 17 - Zoomed 60A Load dynamic (rising).
Ch3: Output voltage, 100mV/div, AC.
Ch4: Load current, 20A/us, sensed by 2mΩ resistor, 25A/div.

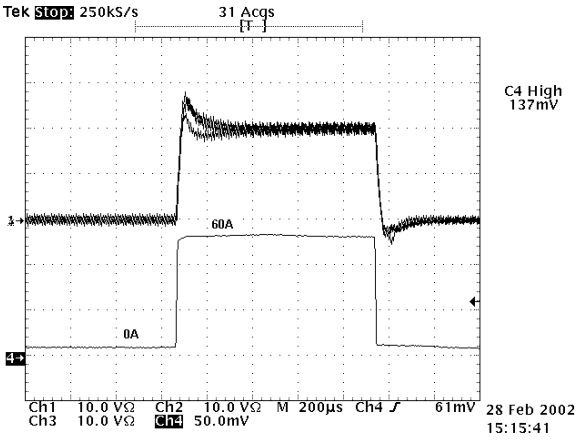


Figure 18 - 60A load dynamic waveforms with three-phase inductor current.
Ch1, Ch2 and Ch3: Inductor current, 10A/div.
Ch4: Load current, 20A/us, sensed by 2mΩ resistor, 25A/div.

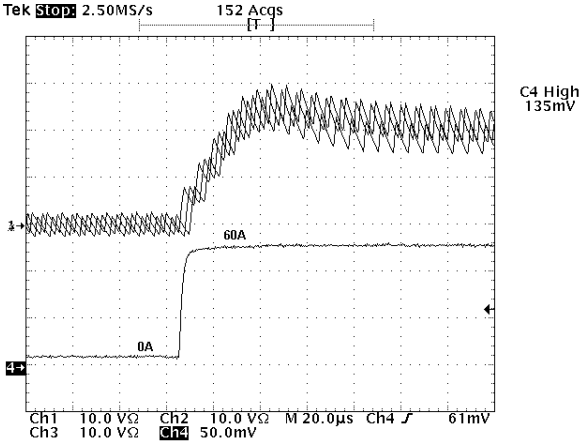


Figure 19 - 60A load dynamic waveforms with three-phase inductor current. (Zoomed)
Ch1, Ch2 and Ch3: Inductor current, 10A/div.
Ch4: Load current, 20A/us, sensed by 2mΩ resistor, 25A/div.

TYPICAL APPLICATION (2)

For Intel Pentium 4 processor with Vcc VID generation and active voltage droop

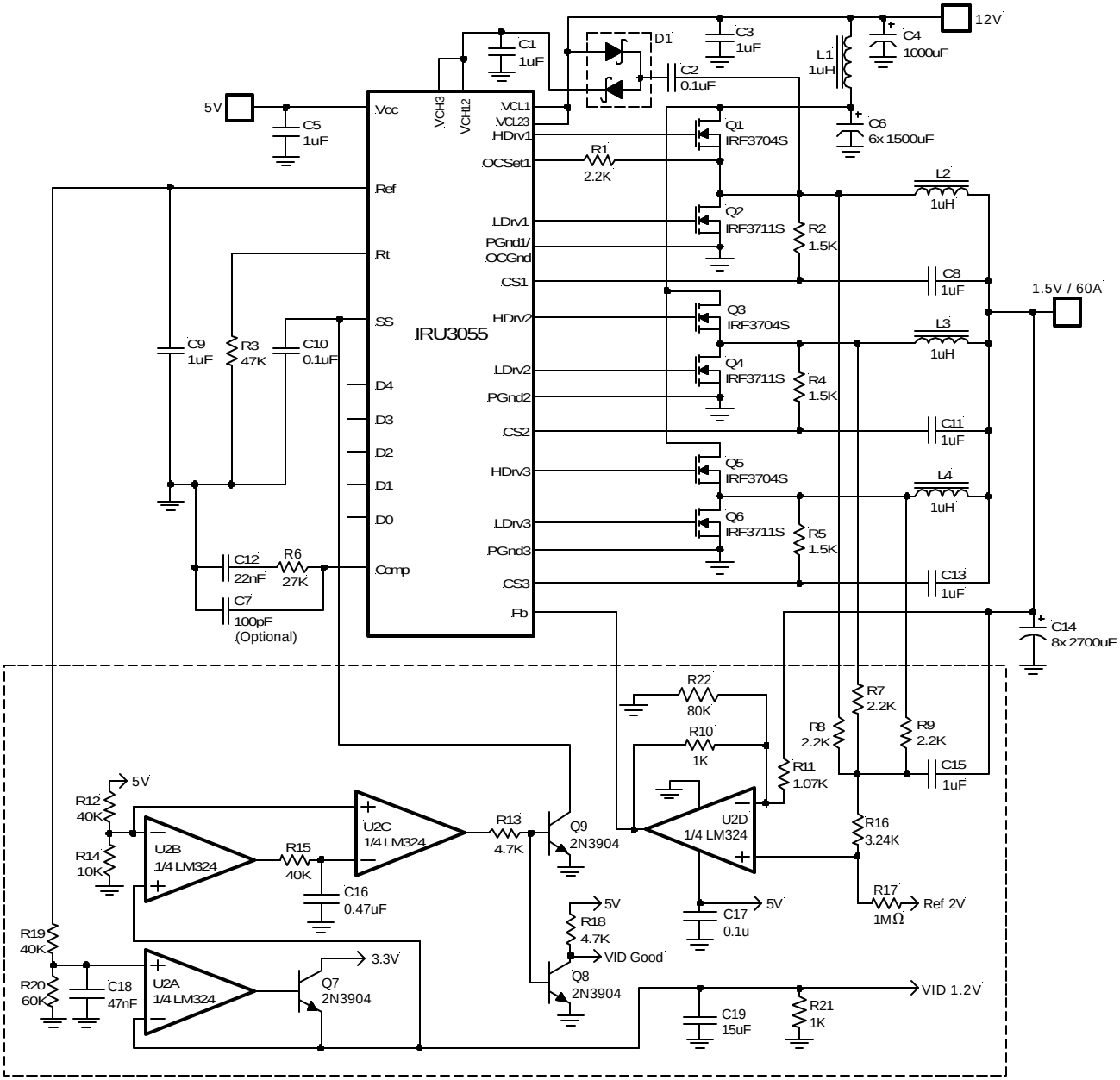


Figure 20 - Application circuit of IRU3055 to implement active voltage droop as well as the 1.2V VID voltage with VccVID Power Good.

PARTS LIST FOR TYPICAL APPLICATION (2)

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1,Q3,Q5	MOSFET	20V, 9mΩ	3	IRF3704S	IR	irf.com
Q2,Q4,Q6	MOSFET	20V, 6mΩ	3	IRF3711S	IR	
U1	Controller	Synchronous PWM	1	IRU3055	IR	
D1	Schottky Diode	In Series	1	BAT54S	IR	
L1	Inductor	1μH	1	Z9479-A	Coilcraft	coilcraft.com
L2,L3,L4	Inductor	1μH	3	T60-18 Core, 6-turns #14 AWG wire		
C1	Cap, Ceramic	1μF, X7R, 25V	1	ECJ-3YB1E105K	Panosonic	maco.panasonic.co.jp
C2,C10	Cap, Ceramic	0.1μF, Y5V, 25V	2	ECJ-2VF1E104Z	Panosonic	
C3,C5,C9, C8,C11,C13	Cap, Ceramic	1μF, Y5V, 16V	6	ECJ-3VF1C105Z	Panosonic	
C4	Cap,Electrolytic	1000μF, 16V	1		Any	
C6	Cap,Electrolytic	1500μF, 16V	6	EEU-FJ1C152U	Panosonic	maco.panasonic.co.jp
C7	Cap (Optional)	100pF, X7R, 50V	1	ECU-V1H101KBN	Panosonic	
C12	Cap, Ceramic	22nF, 50V	1		Panosonic	
C14	Cap,Electrolytic	2700μF,6.3V,13mΩ	8	EEU-FJ0J272U	Panosonic	
R1	Resistor	2.2K, 1%	1		Any	
R2,R4,R5	Resistor	1.5K, 1%	3		Any	
R3	Resistor	47K, 1%	1		Any	
R6	Resistor	27K, 5%	1		Any	

Q7,Q8,Q9	NPN Transistor		3	2N3904	Any	
U2A,B,C,D	OPAMP		1	LM324	Any	
C15	Cap, Ceramic	1μF, X7R, 16V	1	ECJ-2YB1C105K	Panosonic	maco.panasonic.co.jp
C16	Cap, Ceramic	0.47μF, X7R, 16V	1	ECJ-2YB1C474K	Panosonic	
C17	Cap, Ceramic	0.1μF, Y5V, 25V	1	ECJ-2VF1E104Z	Panosonic	
C18	Cap, Ceramic	47nF, X7R, 16V	1	ECJ-2VF1E473K	Panosonic	sanyo.com
C19	Cap, POSCAP	15μF, 6.3V	1		Sanyo	
R7,R8,R9	Resistor	2.2K, 1%	3		Any	
R13,R18	Resistor	4.7K, 5%	2		Any	
R10,R21	Resistor	1K, 1%	2		Any	
R11	Resistor	1.07K, (tuned), 1%	1		Any	
R12,R15, R19	Resistor	40K, 1%	3		Any	
R14	Resistor	10K, 1%	1		Any	
R16	Resistor	3.24K, (tuned), 1%	1		Any	
R17	Resistor	1MΩ, 1%	1		Any	
R20	Resistor	60K, 1%	1		Any	
R22	Resistor	80K, 1%	1		Any	

Introduction to Intel Specification

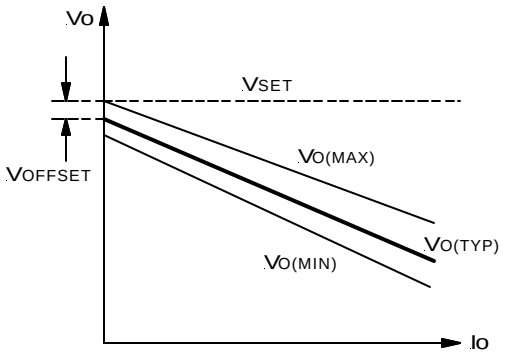


Figure 21 - The Intel specification for the load line.

According to the Intel spec, the output voltage is dependent on the load current. When the current goes up, the voltage goes down. The characteristic can be modeled by the following:

$$Vo = V_{SET} - V_{OFFSET} - K_{LOAD} \times Io \quad ---(10)$$

Where V_{OFFSET} is the offset voltage and K_{LOAD} is the slope of load line.

Rearrangement results in:

$$V_{SET} = Vo + V_{OFFSET} + K_{LOAD} \times Io \quad ---(11)$$

For Intel spec:

V_{OFFSET} = 25mV

K_{LOAD} = 98mV/45A = 2.18mΩ

Implementation of Voltage Droop with IRU3055

With a single single-ended OPAMP, the IRU3055 can achieve voltage droop function as shown in Figure 22. The voltage Vc is a constant voltage such as 2V or 5V. The signal Vo+Rs × Io can be from inductor current sensing. The real application circuit is shown in Figure 20.

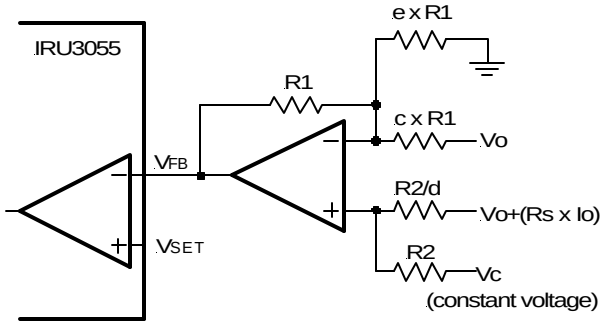


Figure 22 - Implement voltage droop with a single OPAMP.

With this simple circuit, the output voltage will linearly decrease as load current increases. The output voltage will fall in Intel spec. The resistor ratio "c" will determine the slope of the voltage-current load line. The resistor ratios "d" and "e" determine the offset voltage.

In an ideal case, these parameters can be calculated by:

$$c = \frac{Rs}{K_{LOAD} - Rs}$$

$$d = \frac{K_{LOAD}}{Rs} \times \frac{Vc}{V_{OFFSET}}$$

$$e = \frac{Vc}{V_{OFFSET}}$$

Where Rs is equivalent current sensing resistors.

For a 3-phase converter with inductor current sensing:

$$Rs = \frac{R_L}{3}$$

Where R_L is the DC resistance of the inductor.

In practice, the resistor ratios "c" and "d" have to be tuned in order to take some parasitic parameters such as PCB layout trace into account.

Component selection guide

The implementation circuit is shown in Fig.20, Resistor R7, R8, R9 and capacitor C15 configures a inductor current losses sensing network to sense the load current. (Attn: The C15 and R11 must connect directly to the output terminal.) The RC networks that sense the inductor current have to satisfy the following:

$$(R/3) \times C = L/R_L$$

For example, in the application circuit in Figure 20, the inductor is 1μH and the DC resistance is 1.6mΩ. If the filter capacitor C15 is chosen to be 1μF, then the current sensing resistors R7, R8 and R9 are:

$R = 3 \times L/R_L/C$

$R = 3 \times 1\mu H/1.6m\Omega/1\mu F = 1.87K$

Because the given inductor is larger at zero current (it is 1.3μH at 0 current). A large resistor has to be taken.

In the application circuit in Figure 20, R7,R8 and R9=2.2K. Select R17 (referring to R2 in Figure 22) to be 1MΩ if we consider the input bias of OPAMP LM324. Select R10 (referring to R1 in Figure 22) to be 1KΩ.

R10=1K and R17=1MΩ

Connect the voltage Vc to 2V reference voltage shown in Figure 20.

Vc=2V

Calculating R22 (referring to e × R1 in Figure 22) by the provided equation, we get

$$R22 = R17 \times Vc/V_{OFFSET} = 1K \times 2V/25mV = 80K$$

The resistor R11 and R16 (referring to c × R1 and d × R2 in Figure 22) have to be tuned. From the suggested equation, they are in a few KΩ range. Because resistor R11 and R16 function independent, they can be tuned separately. First, connect the board and make the board work first. Put no load in the output. Then replace R16 with a 5K~20K potentiometer and adjust the potentiometer so as the output voltage is about 25mV lower than the DAC output setting. Because the output current is zero, the resistor R11 will not affect the output voltage. The DC offset is only dependent on R16. Select R16 with the tuned potentiometer value.

After R16 is tuned, replace R11 with a potentiometer. Connect the output voltage to certain current load (for example, half of the nominal load, 30A). Adjust the potentiometer so that the output voltage has the same voltage drops as Intel spec requests (for example, 95mV drop comparing with zero current condition). Then select R11 with tuned potentiometer value.

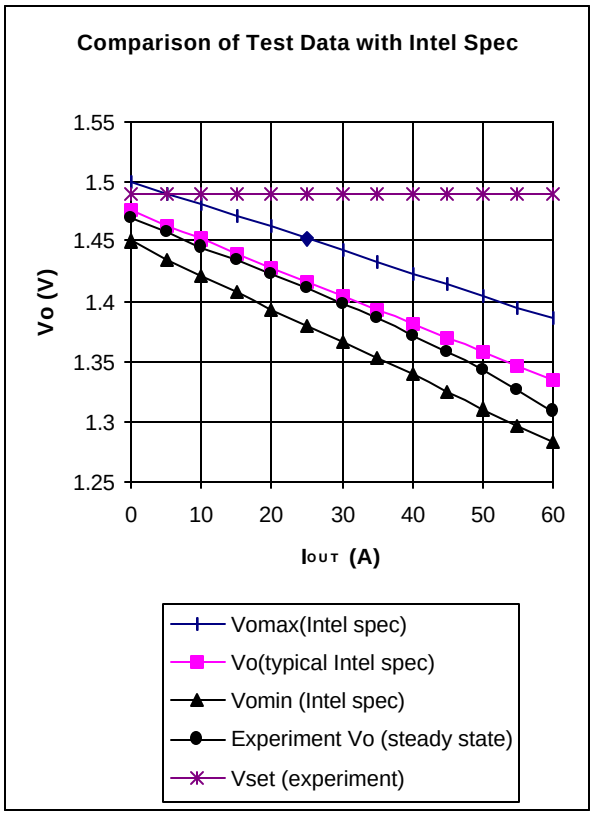


Figure 23 - Test steady state output voltage for the circuit of IRU3055 with active droop.

The test data is displayed in Figure 23. The DAC input is 01110, which refers to output voltage 1.5V. The measured DAC output V_{SET} is 1.490V. The measured output voltage versus load current falls into the Intel specification as shown in Figure 23.

In this figure, at light load, the output voltage almost follows the Intel typical specification. At 40A, 50A and 60A loads, the output voltage is a slight deviation from the typical Intel spec. The reason is because the inductors get hot at high current loads. The resistance increases comparing with low load condition. As a result, there is more voltage droop than the theoretical prediction, because the specification at high current has larger tolerance. The Intel specification can be satisfied easily with the proposed circuit.

Implement the 1.2V VID Regulator

If a Quadra-OPAMP such as LM324 is used, the additional 1.2V VID regulator as well as the power sequence can be implemented. In application circuit Figure 20, one OPAMP and a NPN transistor 2N3904 implement a 1.2V, 30mA VID voltage regulator. The VID voltage is also sent to the minus input of one OPAMP. When the VID voltage reaches 1V, the OPAMP changes to high state and starts to charge up the RC network. The Resistor R15 and the capacitor C16 function as a delay network. 40K and 0.1μF will give about 1ms delay. In the application circuit, C16=0.47μF, which gives about 5ms delay for a better illustration. When the voltage across capacitor C16 reaches 1V, the OPAMP will turn off the two NPN transistors. The soft-start capacitor of IRU3055, C10, starts to be charged up and output voltage, Vo, will smoothly go into steady state.

EXPERIMENT WAVEFORMS FOR TYPICAL APPLICATION (2)

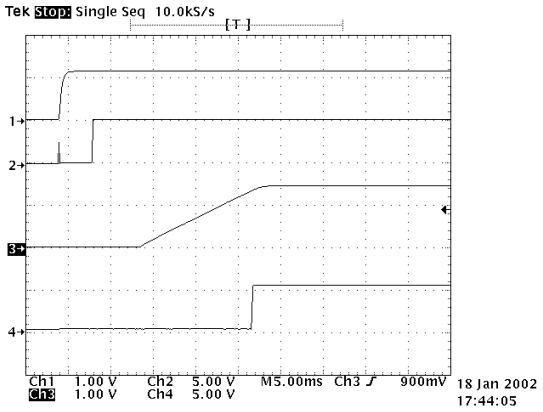


Figure 24 - Soft-start.
Ch1: 1.2V VID. Ch2: VID Good.
Ch3: 1.5V Output. Ch4: PGood.

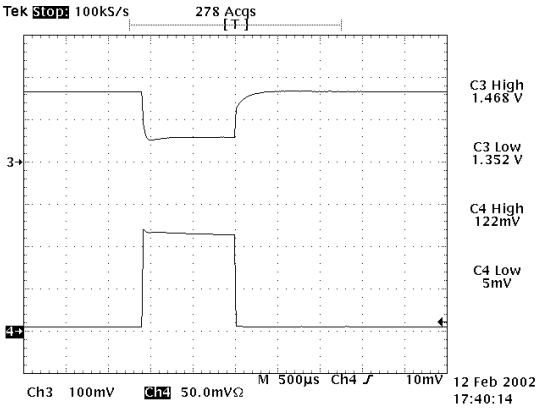


Figure 25 - 60A Load dynamic with 20A/µs slew rate.
Ch4: Output current, sensed through 2mΩ resistor, 25A/div.
Ch3: Ouput voltage, DC offset 1.3V, 100mV/div.

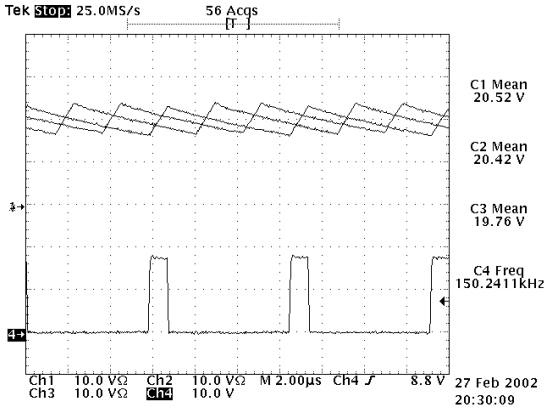


Figure 26 - 3-Phase inductor current at 60A load,
Ch1, Ch2 and Ch3: 10A/div and gate signal.

TYPICAL APPLICATION (3)

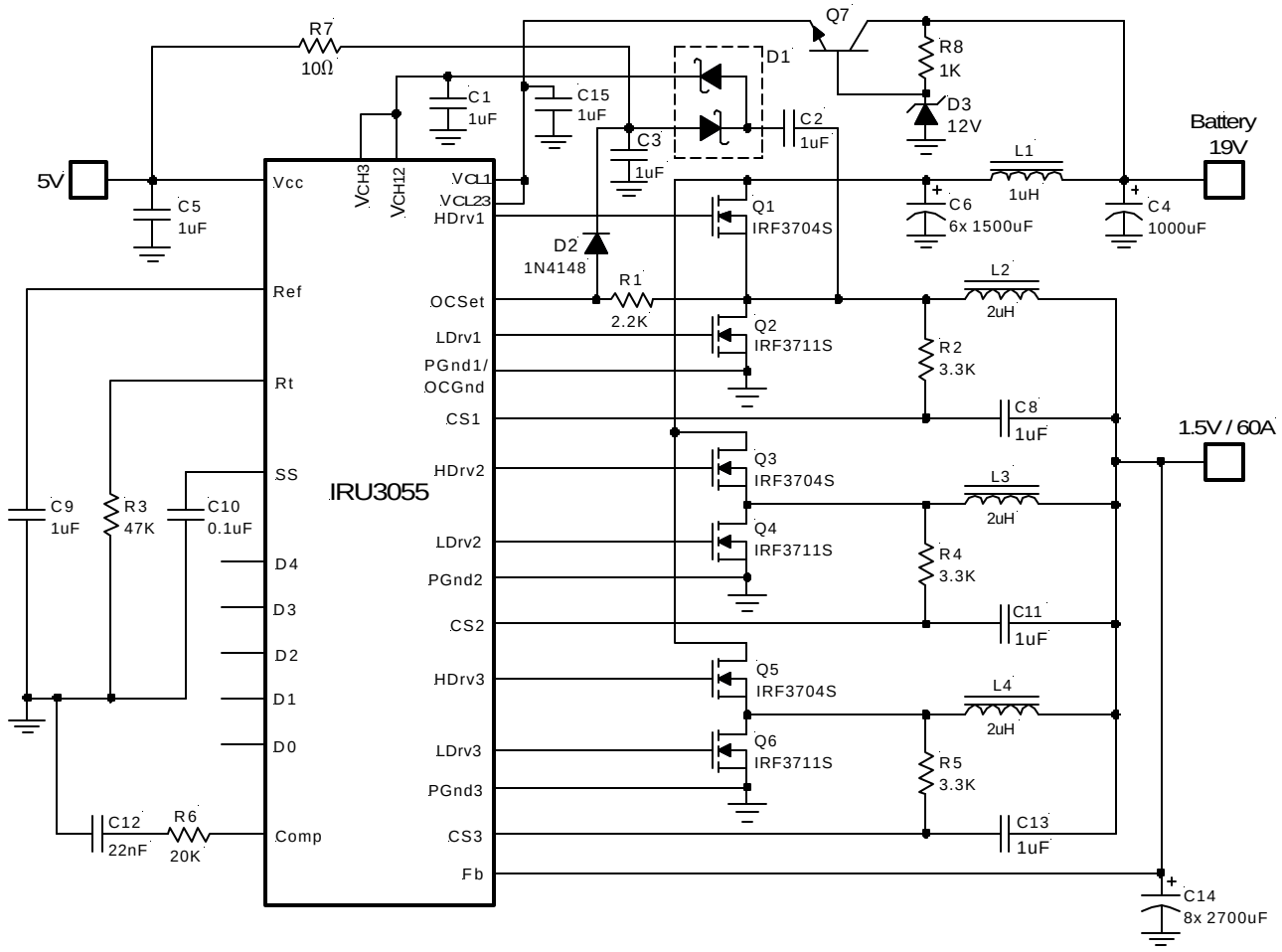


Figure 26 - Typical application of IRU3055 in notebook application.

PARTS LIST FOR TYPICAL APPLICATION (3)

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1, Q3, Q5	MOSFET	20V, 9mΩ	3	IRF3704S	IR	irf.com
Q2, Q4, Q6	MOSFET	20V, 6mΩ	3	IRF3711S	IR	
Q7	NPN Transistor		1	2N3904	Any	
U1	Controller	Synchronous PWM	1	IRU3055	IR	irf.com
D1	Schottky Diode	In Series	1	BAT54S	IR	
D2	Diode		1	1N4148	Any	
D3	Zener Diode		1	1N5242A	Any	
L1	Inductor	1.3μH	1	Z9479-A	Coilcraft	coilcraft.com
L2,L3,L4	Inductor	2μH, 15A	3	T60-18 Core, 6-turns #14 AWG wire		
C1	Cap, Ceramic	1μF, X7R, 25V	1	ECJ-3YB1E105K	Panosonic	maco.panasonic.co.jp
C2, C10	Cap, Ceramic	0.1μF, Y5V, 25V	2	ECJ-2VF1E104Z	Panosonic	
C3,5,8,9, 11,13,15	Cap, Ceramic	1μF, Y5V, 16V	7	ECJ-3VF1C105Z	Panosonic	
C4	Cap,Electrolytic	1000μF, 16V	1		Any	
C6	Cap,Electrolytic	1500μF, 16V	6	EEU-FJ1C152U	Panosonic	maco.panasonic.co.jp
C12	Cap, Ceramic	22nF, X7R, 50V	1	ECU-V1H223KBG	Panosonic	
C14	Cap,Electrolytic	2700μF,6.3V,13mΩ	8	EEU-FJ0J272U	Panosonic	
R1	Resistor	2.2K, 1%	1		Any	
R2,R4,R5	Resistor	3.3K, 1%	3		Any	
R3	Resistor	47K, 1%	1		Any	
R6	Resistor	20K, 1%	1		Any	
R7	Resistor	10Ω, 5%	1		Any	

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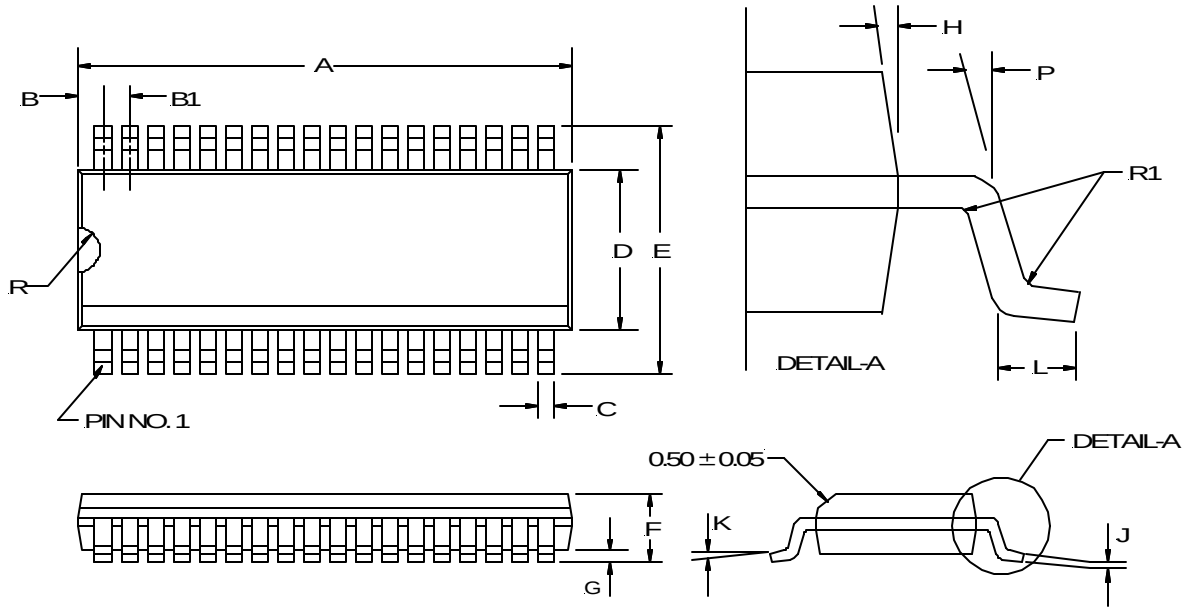
(Q) QSOP Package, Wide Body
36-Pin

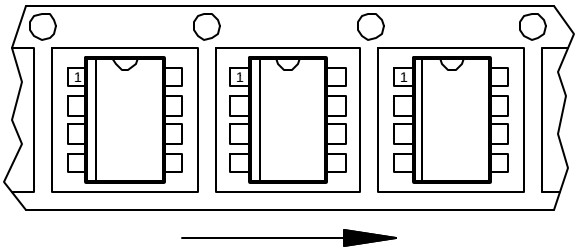


36-PIN		
SYMBOL	**MIN**	**MAX**
A	15.20	15.40
B	0.85	
B1	0.80 REF	
C	0.28	0.51
D	7.40	7.60
E	10.11	10.51
F	2.44	2.64
G	0.10	0.30
H	7° TYP	
J	0.23	0.32
K	0°	8°
L	0.40	1.27
R	0.63	0.89
R1	0.20 ± 0.05	
P	7° ± 3°	

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
Q	QSOP Plastic, Wide Body	36	---	1500	Fig A



Feed Direction
Figure A

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Section 5: Package Information

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig 1
F	TSSOP Plastic	8, 14	100	2500	Fig 2
F	TSSOP Plastic	16	---	2500	Fig 2
F	TSSOP Plastic	20, 24	74	2500	Fig 2
H	MLPM, 3x3	6	---	3000	Fig 7
L3	SOT-23	3	---	3000	Fig 3
L5	SOT-23	5	---	3000	Fig 3
M	TO-263	3, 5, 7	50	750	Fig 4
P	Ultra Thin-Pak™	2, 3, 5, 7	75	2500	Fig 5
Q	QSOP Plastic, Narrow Body	24	---	1500	Fig 2
Q	QSOP Plastic, Wide Body	36	---	1500	Fig 2
S	SOIC, Narrow Body	8	95	2500	Fig 2
S	SOIC, Narrow Body	14	55	2500	Fig 2
S	SOIC, Narrow Body	16	50	2500	Fig 2
T	TO-220	3, 5, 7	50	---	---
W	SOIC, Wide Body	20	38	1000	Fig 2
W	SOIC, Wide Body	24	31	1000	Fig 2
W	SOIC, Wide Body	28	27	1000	Fig 2
Y	SOT-223	3	80	2500	Fig 6

(See Figures on next page)

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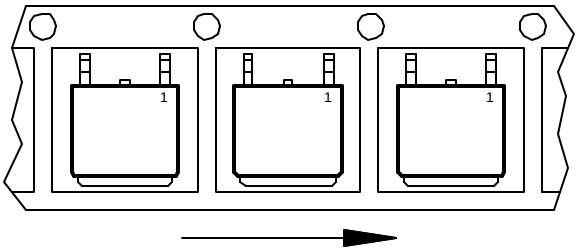
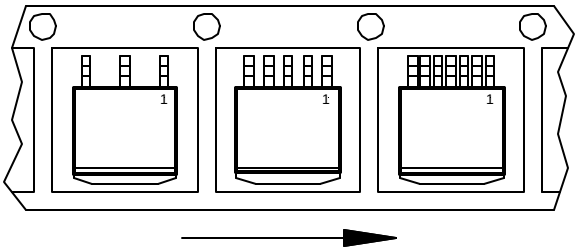
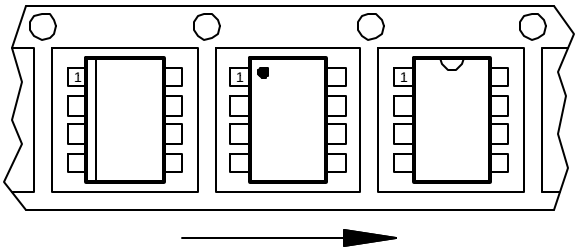
TAPE AND REEL ORIENTATION



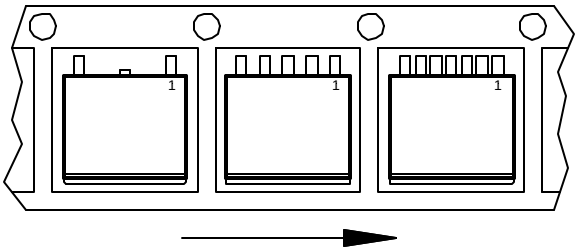
Feed Direction
Figure 1 - TO-252



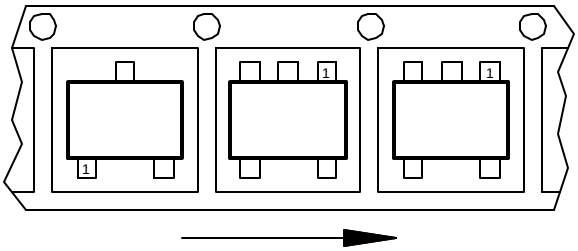
Feed Direction
Figure 4 - TO-263



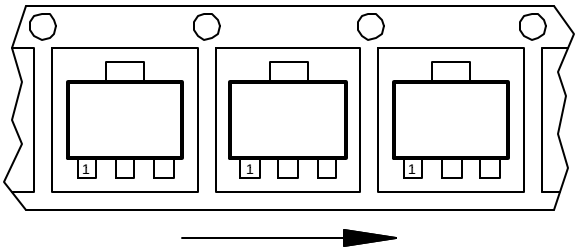
Feed Direction
Figure 2 - TSSOP, QSOP, SOIC



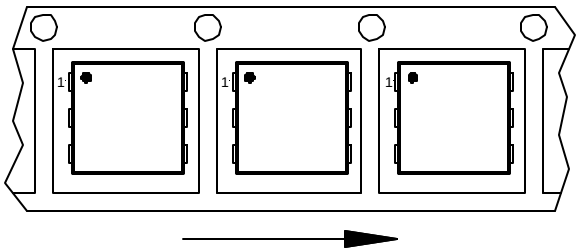
Feed Direction
Figure 5 - Ultra Thin Pak™



Feed Direction
Figure 3 - SOT-23



Feed Direction
Figure 6 - SOT-223



Feed Direction
Figure 7 - MLPM (Live Bug)

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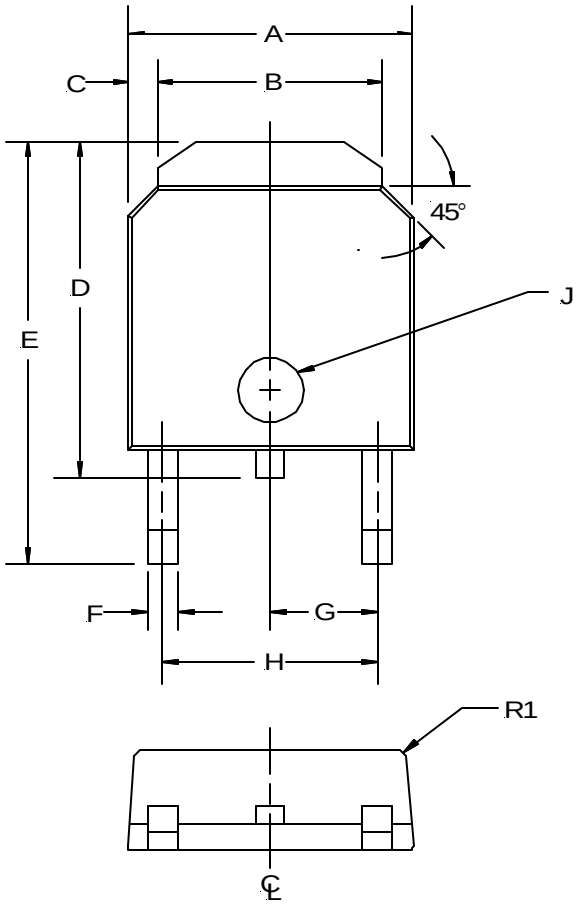
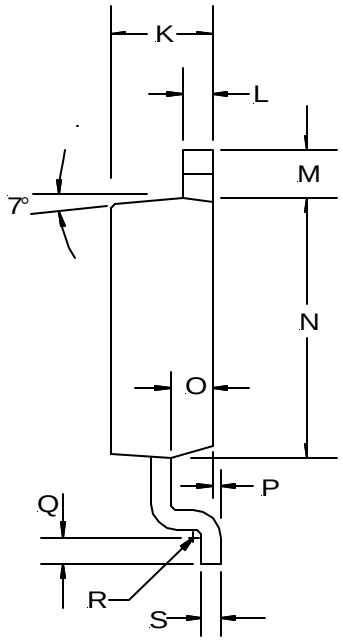
(D) TO-252 Package
2-Pin

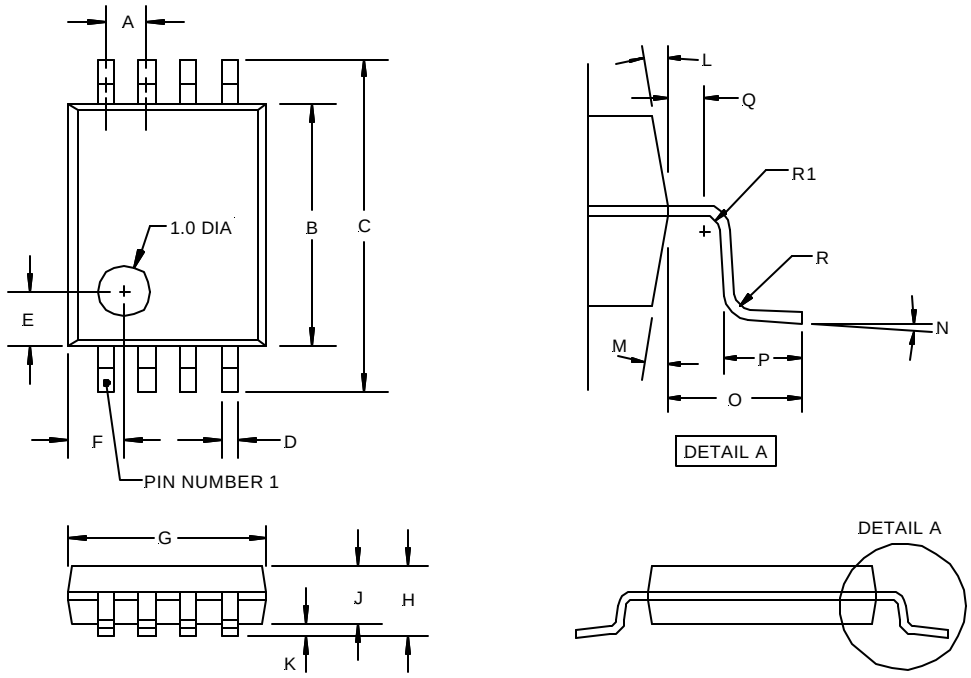




SYMBOL	MIN	MAX
A	6.477	6.731
B	5.004	5.207
C	0.686	0.838
D	7.417	8.179
E	9.703	10.084
F	0.635	0.889
G	2.286 BSC	
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

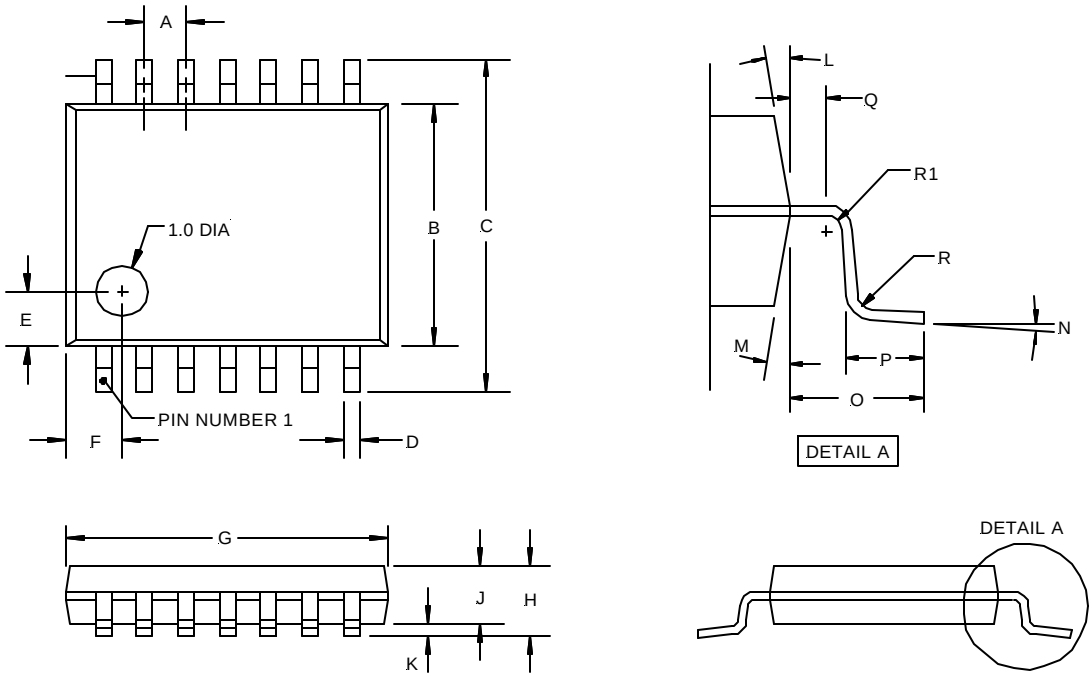
(F) TSSOP Package
8-Pin



SYMBOL	8-PIN		
DESIG	MIN	NOM	MAX
A		0.65 BSC	
B	4.30	4.40	4.50
C		6.40 BSC	
D	0.19	---	0.30
E		1.00	
F		1.00	
G	2.90	3.00	3.10
H	---	---	1.10
J	0.85	0.90	0.95
K	0.05	---	0.15
L		12° REF	
M		12° REF	
N	0°	---	8°
O		1.00 REF	
P	0.50	0.60	0.75
Q		0.20	
R	0.09	---	---
R1	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

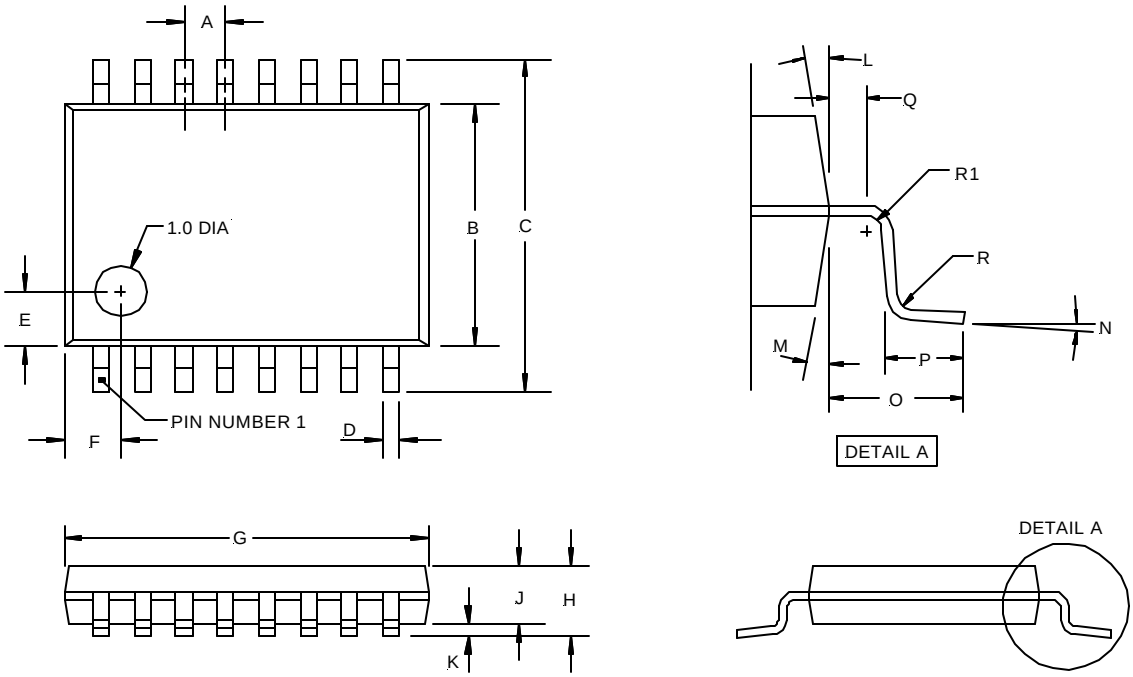
(F) TSSOP Package
14-Pin



SYMBOL	14-PIN		
DESIG	MIN	NOM	MAX
A		0.65 BSC	
B	4.30	4.40	4.50
C		6.40 BSC	
D	0.19	---	0.30
E		1.00	
F		1.00	
G	4.90	5.00	5.10
H	---	---	1.10
J	0.85	0.90	0.95
K	0.05	---	0.15
L		12° REF	
M		12° REF	
N	0°	---	8°
O		1.00 REF	
P	0.50	0.60	0.75
Q		0.20	
R	0.09	---	---
R1	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

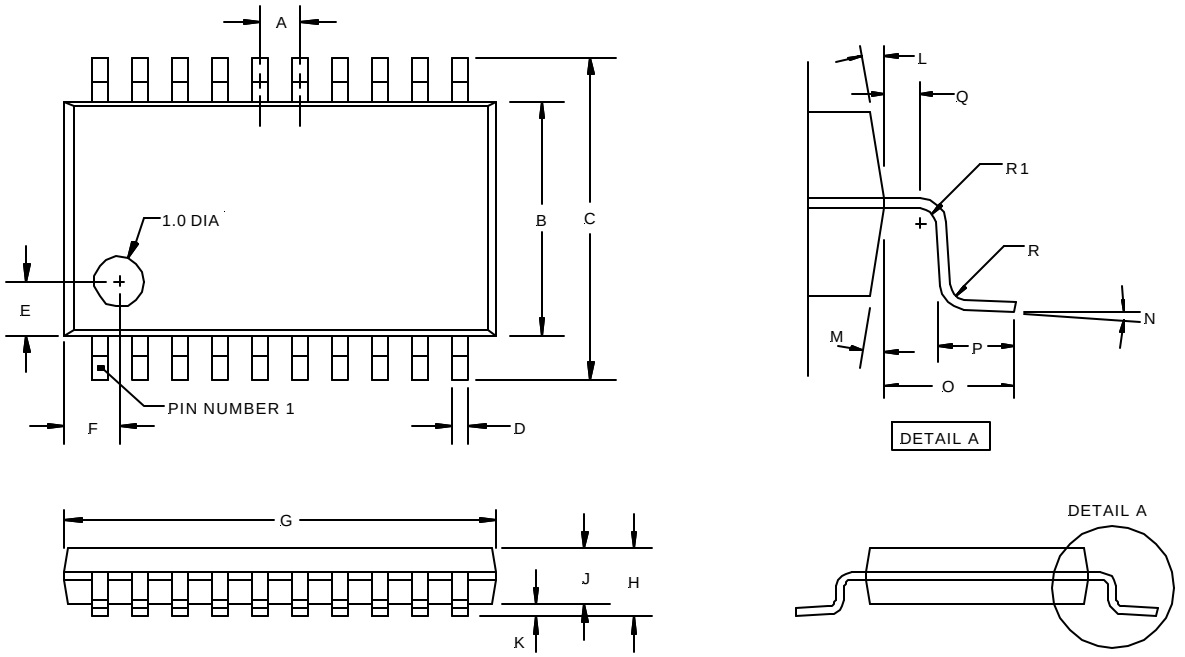
(F) TSSOP Package
16-Pin



SYMBOL	16-PIN		
DESIG	MIN	NOM	MAX
A		0.65 BSC	
B	4.30	4.40	4.50
C		6.40 BSC	
D	0.19	---	0.30
E		1.00	
F		1.00	
G	4.90	5.00	5.10
H	---	---	1.10
J	0.85	0.90	0.95
K	0.05	---	0.15
L		12° REF	
M		12° REF	
N	0°	---	8°
O		1.00 REF	
P	0.50	0.60	0.75
Q		0.20	
R	0.09	---	---
R1	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

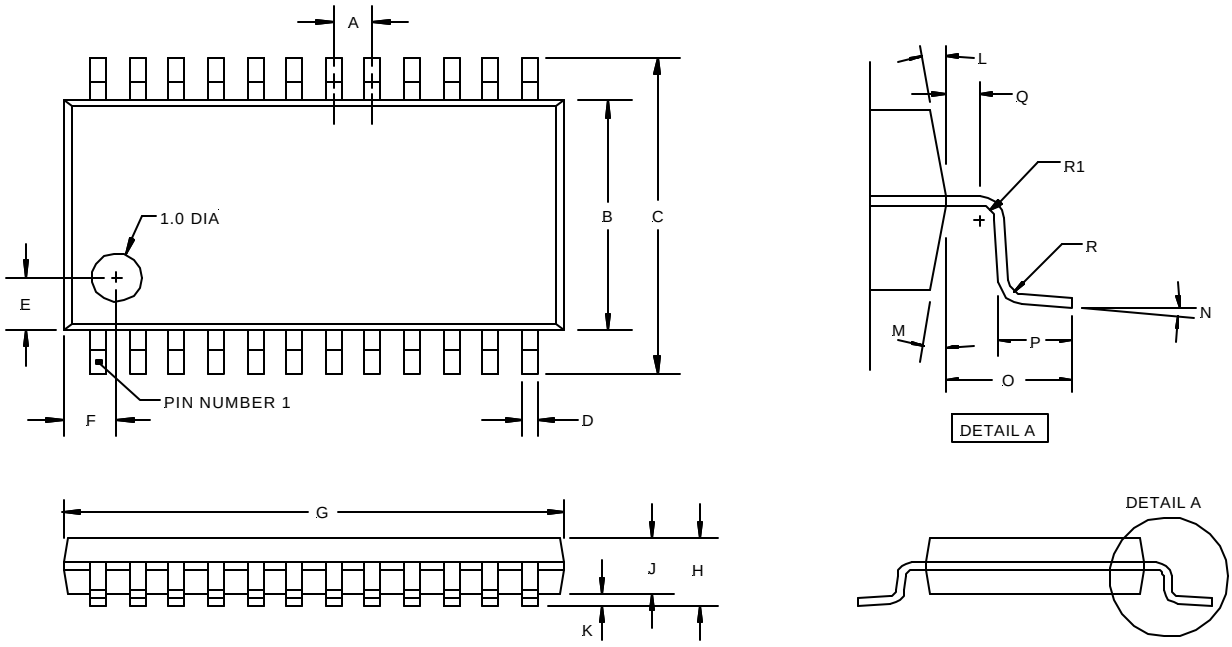
(F) TSSOP Package
20-Pin



SYMBOL	20-PIN		
DESIG	MIN	NOM	MAX
A		0.65 BSC	
B	4.30	4.40	4.50
C		6.40 BSC	
D	0.19	---	0.30
E		1.00	
F		1.00	
G	6.40	6.50	6.60
H	---	---	1.10
J	0.85	0.90	0.95
K	0.05	---	0.15
L		12° REF	
M		12° REF	
N	0°	---	8°
O		1.00 REF	
P	0.50	0.60	0.75
Q		0.20	
R	0.09	---	---
R1	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

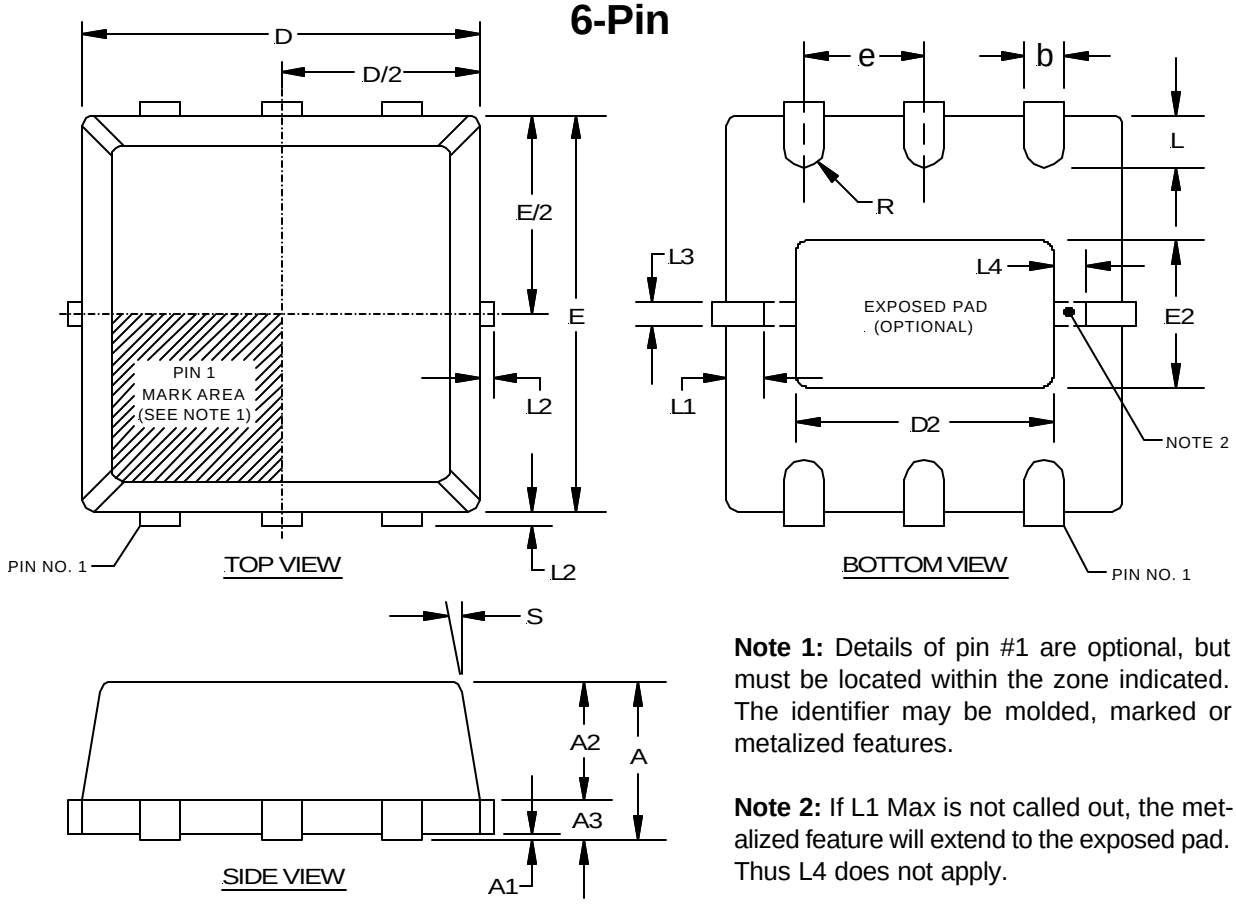
(F) TSSOP Package
24-Pin



SYMBOL DESIG	24-PIN		
	MIN	NOM	MAX
A		0.65 BSC	
B	4.30	4.40	4.50
C		6.40 BSC	
D	0.19	---	0.30
E		1.00	
F		1.00	
G	7.70	7.80	7.90
H	---	---	1.10
J	0.85	0.90	0.95
K	0.05	---	0.15
L		12° REF	
M		12° REF	
N	0°	---	8°
O		1.00 REF	
P	0.50	0.60	0.75
Q		0.20	
R	0.09	---	---
R1	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

(H) MLPM Package
6-Pin



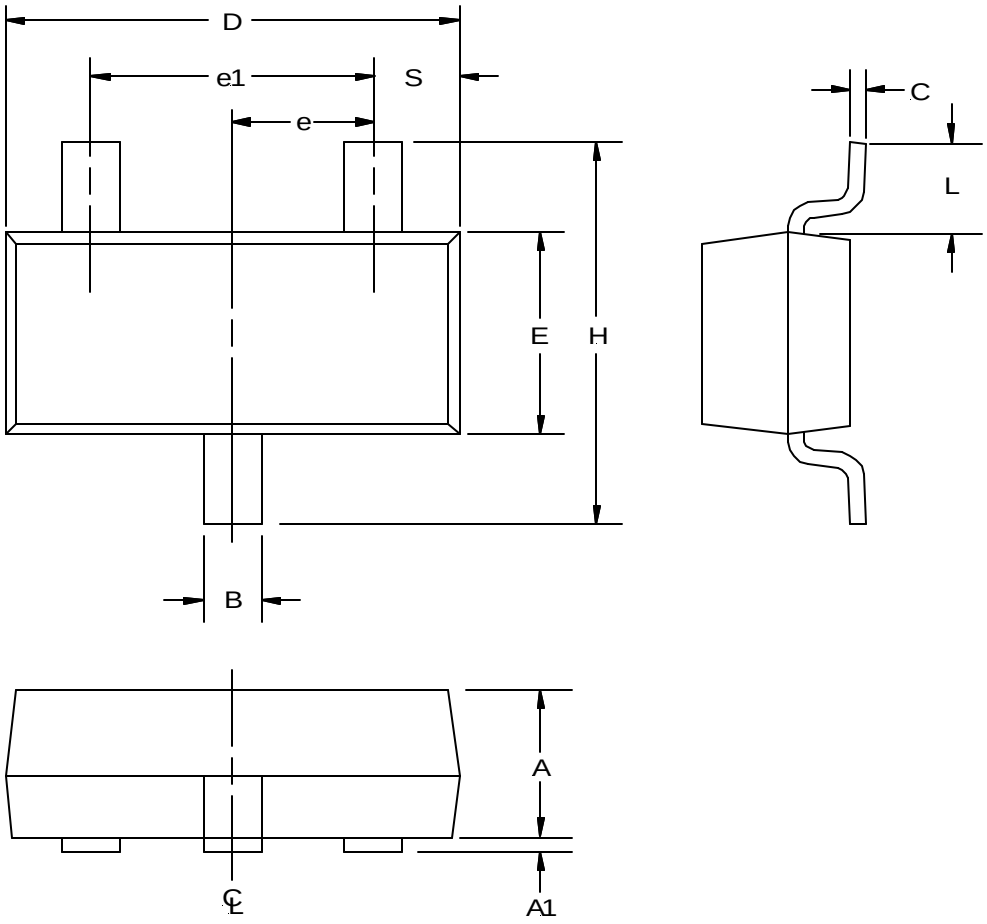
Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, marked or metalized features.

Note 2: If L1 Max is not called out, the metalized feature will extend to the exposed pad. Thus L4 does not apply.

SYMBOL	6-PIN 3x3		
DESIG	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.025	0.05
A2	0.65	0.70	0.75
A3	0.15	0.20	0.25
b	0.33	0.35	0.43
D	3.00 BSC		
D2	1.92	2.02	2.12
E	3.00 BSC		
E2	1.11	1.21	1.31
e	0.95		
L	0.20	0.29	0.45
L1	0.16	0.24	0.40
L2	---	---	0.125
L3	0.17	---	0.30
L4	0.17	---	---
R	0.127 REF		
S	0°	10°	12°

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

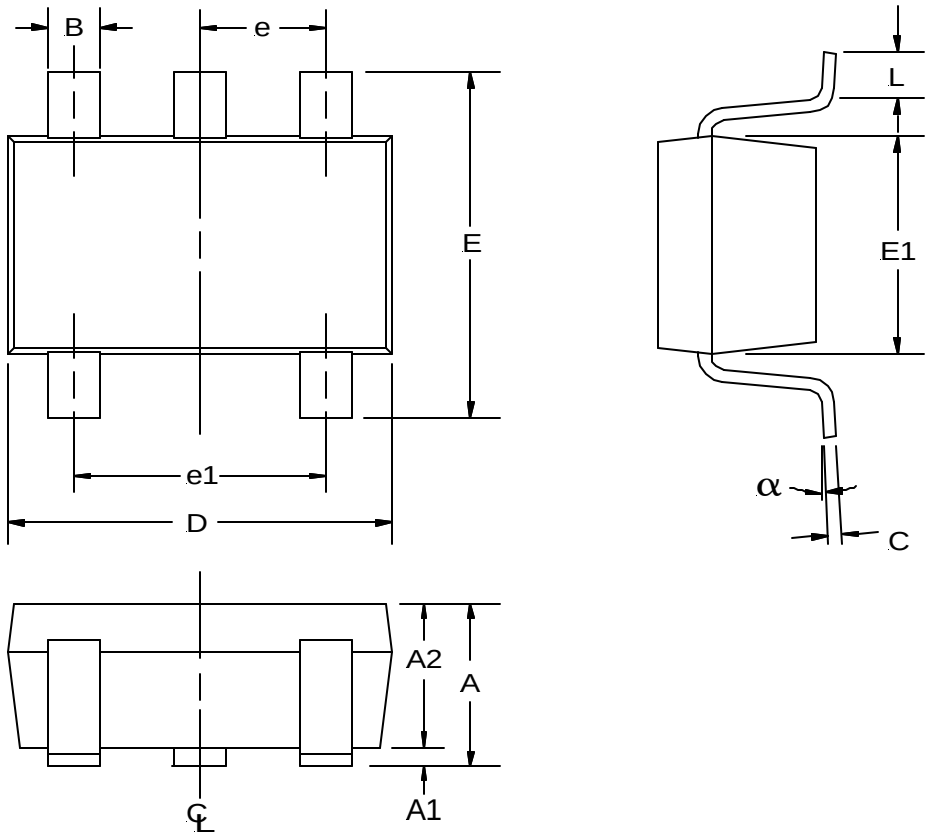
(L3) SOT-23 Package
3-Pin



SYMBOL	MIN	MAX
A	0.890	1.120
A1	0.013	0.100
B	0.370	0.510
C	0.085	0.180
D	2.800	3.040
E	1.200	1.400
e	0.890	1.030
e1	1.780	2.050
H	2.100	2.640
L	0.55 REF	
S	0.450	0.600

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

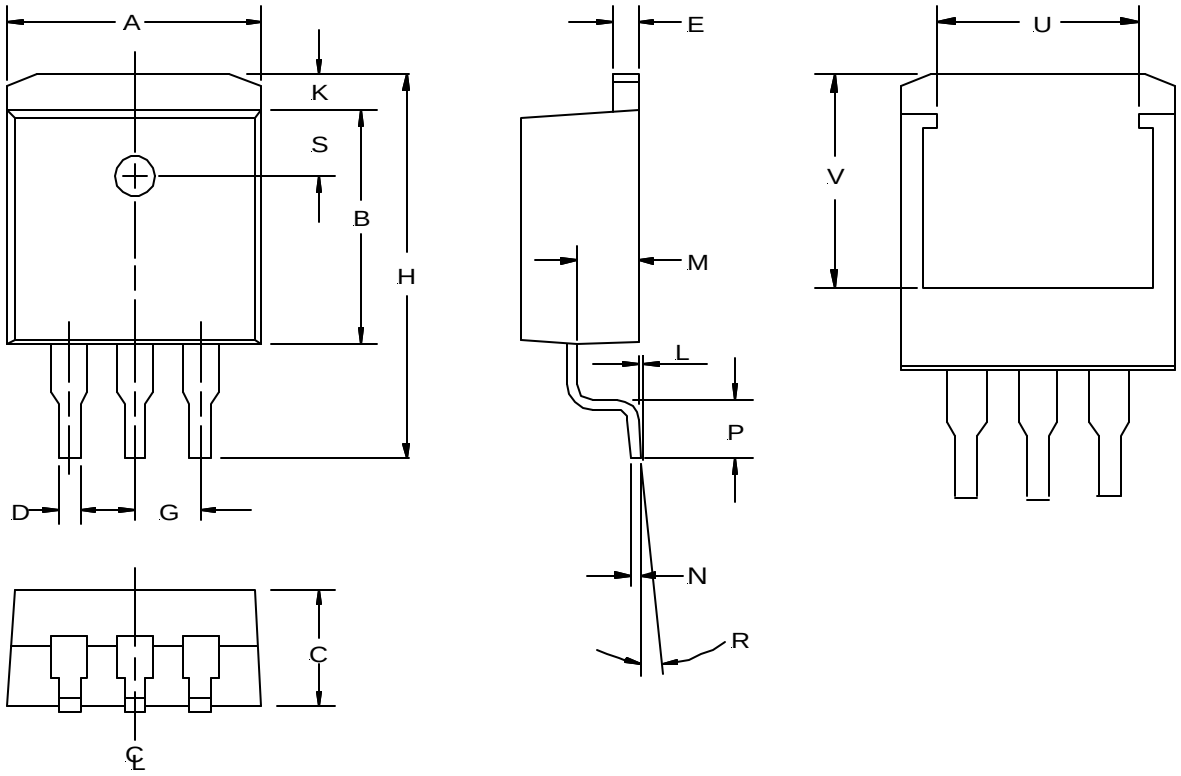
(L5) SOT-23 Package
5-Pin



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.25	0.50
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
e	0.95 REF	
e1	1.90 REF	
L	0.35	0.55
α	0°	10°

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

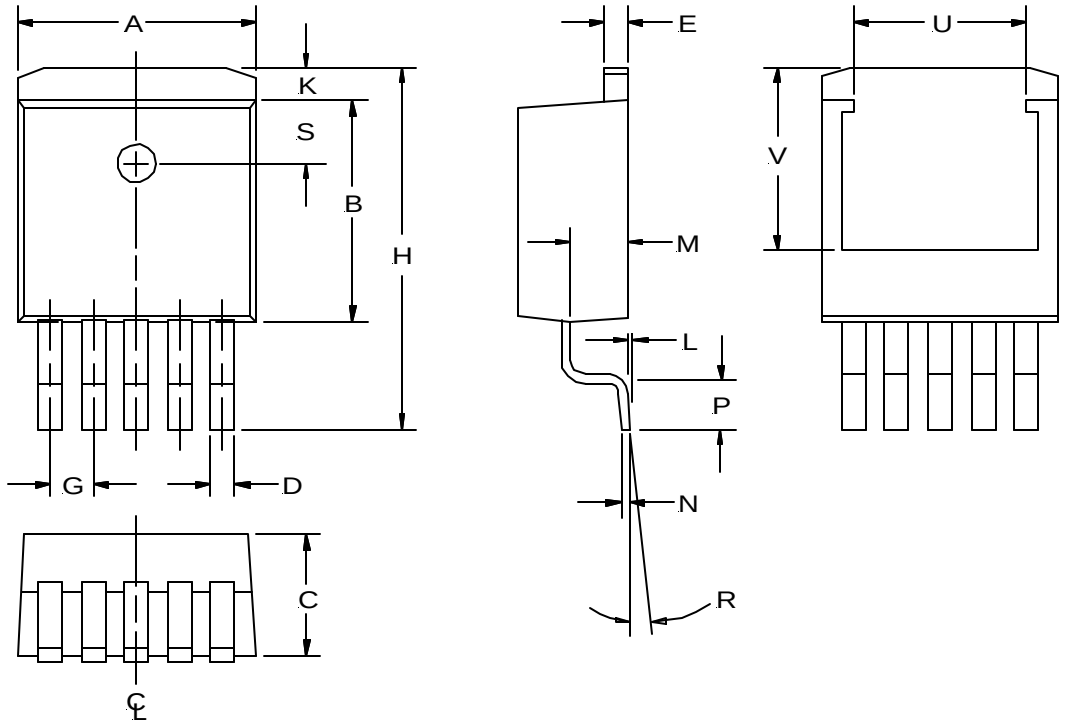
(M) TO-263 Package
3-Pin



SYMBOL	MIN	MAX
A	10.05	10.312
B	8.28	8.763
C	4.31	4.572
D	0.66	0.91
E	1.14	1.40
G	2.54 REF	
H	14.73	15.75
K	1.40	1.68
L	0.00	0.254
M	2.49	2.74
N	0.33	0.58
P	2.286	2.794
R	0°	8°
S	2.41	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

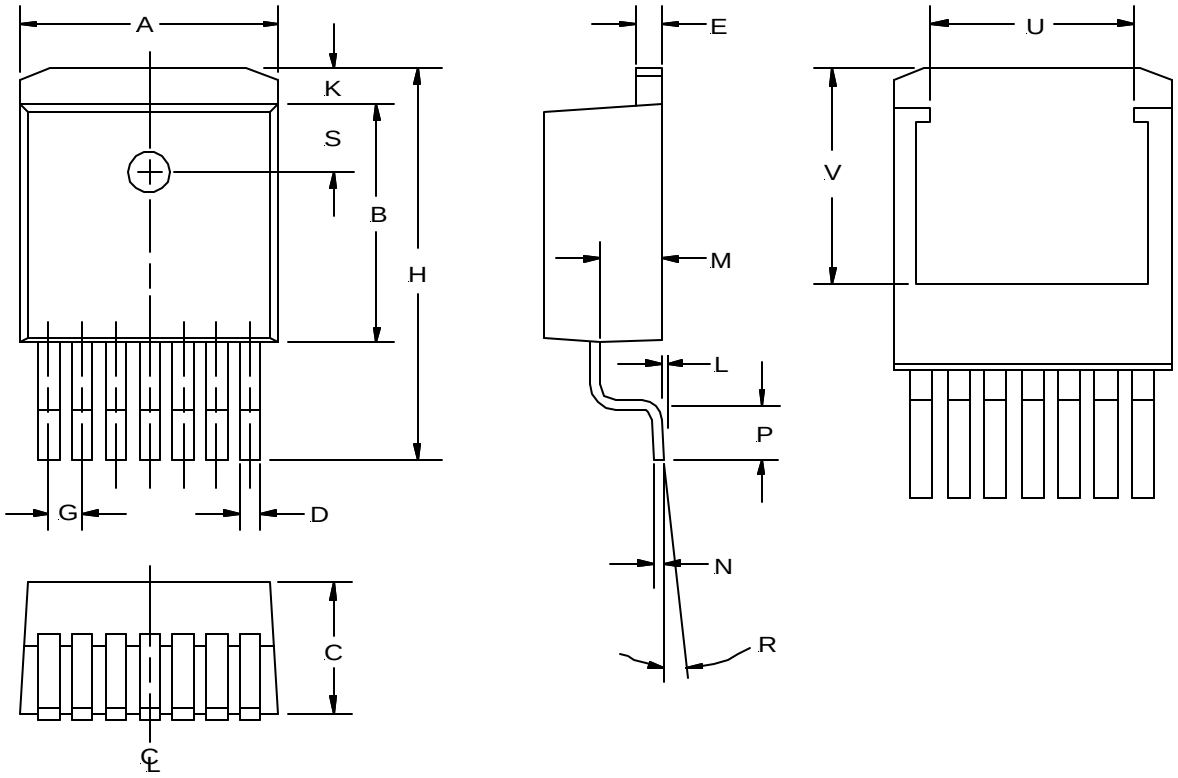
(M) TO-263 Package
5-Pin



SYMBOL	MIN	MAX
A	10.05	10.668
B	8.28	9.169
C	4.31	4.597
D	0.66	0.91
E	1.14	1.40
G	1.575	1.829
H	14.605	15.875
K	1.143	1.68
L	0.00	0.305
M	2.49	2.74
N	0.33	0.58
P	2.286	2.794
R	0°	8°
S	1.143	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

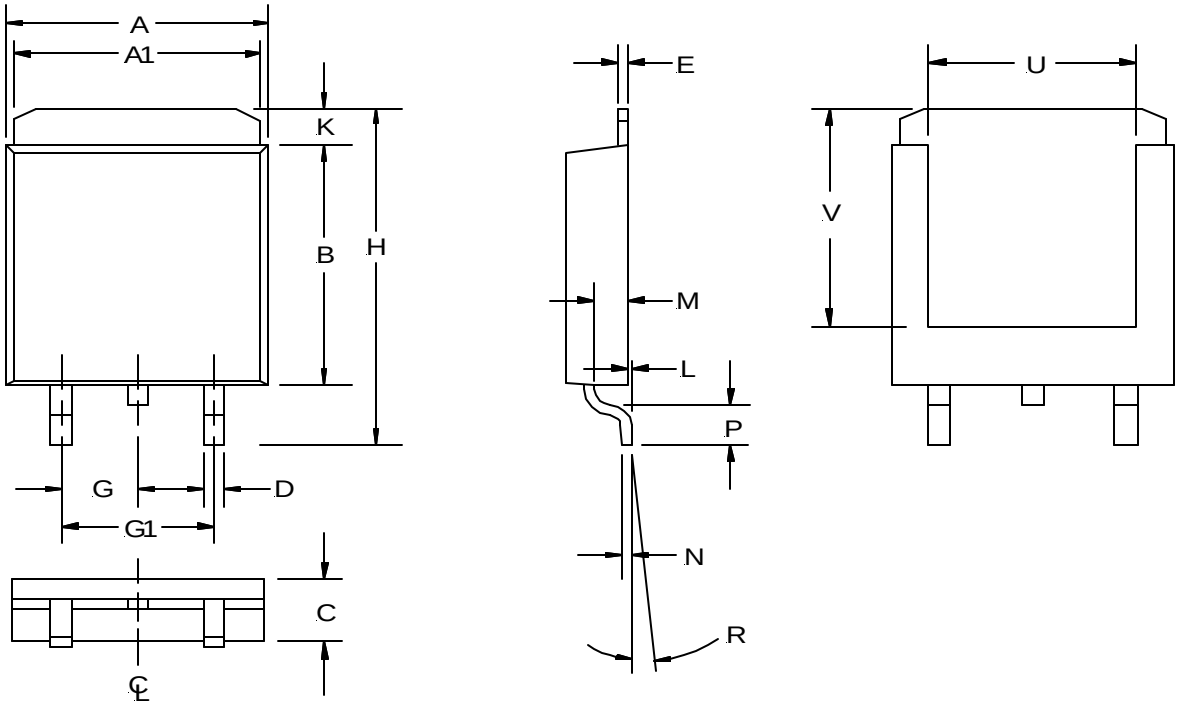
(M) TO-263 Package
7-Pin



SYMBOL	MIN	MAX
A	10.05	10.31
B	8.28	8.53
C	4.31	4.57
D	0.66	0.91
E	1.14	1.40
G	1.27 REF	
H	14.73	15.75
K	1.40	1.68
L	0.00	0.25
M	2.49	2.74
N	0.43	0.58
P	2.29	2.79
R	0°	8°
S	2.41	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(P) Ultra Thin-Pak™
2-Pin

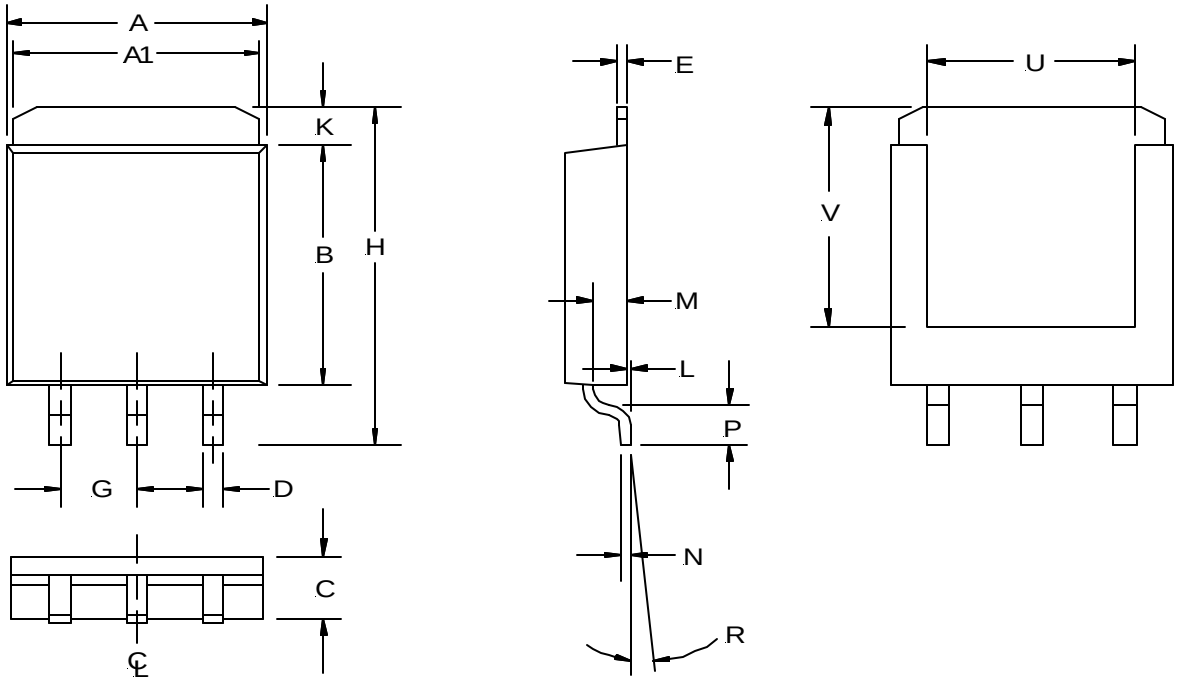


SYMBOL	MIN	MAX
A	5.91	6.17
A1	5.54	5.79
B	6.02	6.27
C	1.70	2.03
D	0.63	0.79
E	0.17	0.33
G	2.16	2.41
G1	4.45	4.70
H	9.42	9.68
K	0.76	1.27
L	0.02	0.13
M	0.89	1.14
N	0.25	0.25
P	0.94	1.19
R	2°	6°
U	2.92	3.30
V	5.08 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

Package Dimensions

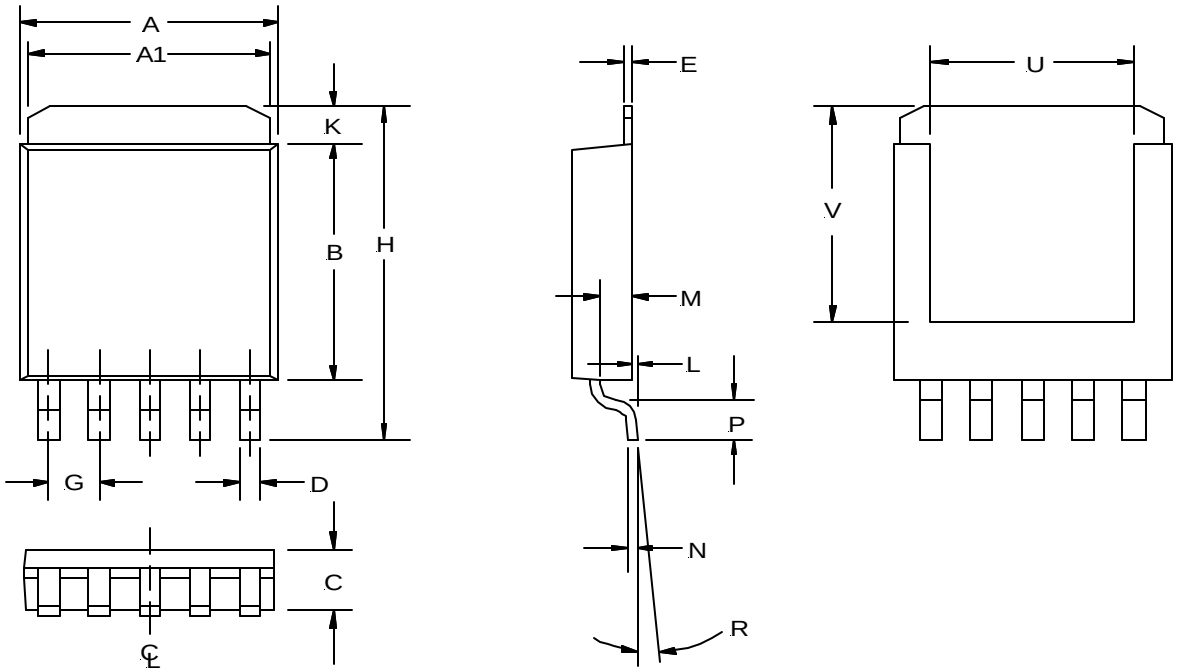
(P) Ultra Thin-Pak™
3-Pin



SYMBOL	MIN	MAX
A	9.27	9.52
A1	8.89	9.14
B	7.87	8.13
C	1.78	2.03
D	0.63	0.79
E	0.25 NOM	
G	2.54	
H	10.41	10.67
K	0.76	1.27
L	0.03	0.13
M	0.89	1.14
N	0.25	
P	0.79	1.04
R	3°	6°
U	5.59 NOM	
V	7.49 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

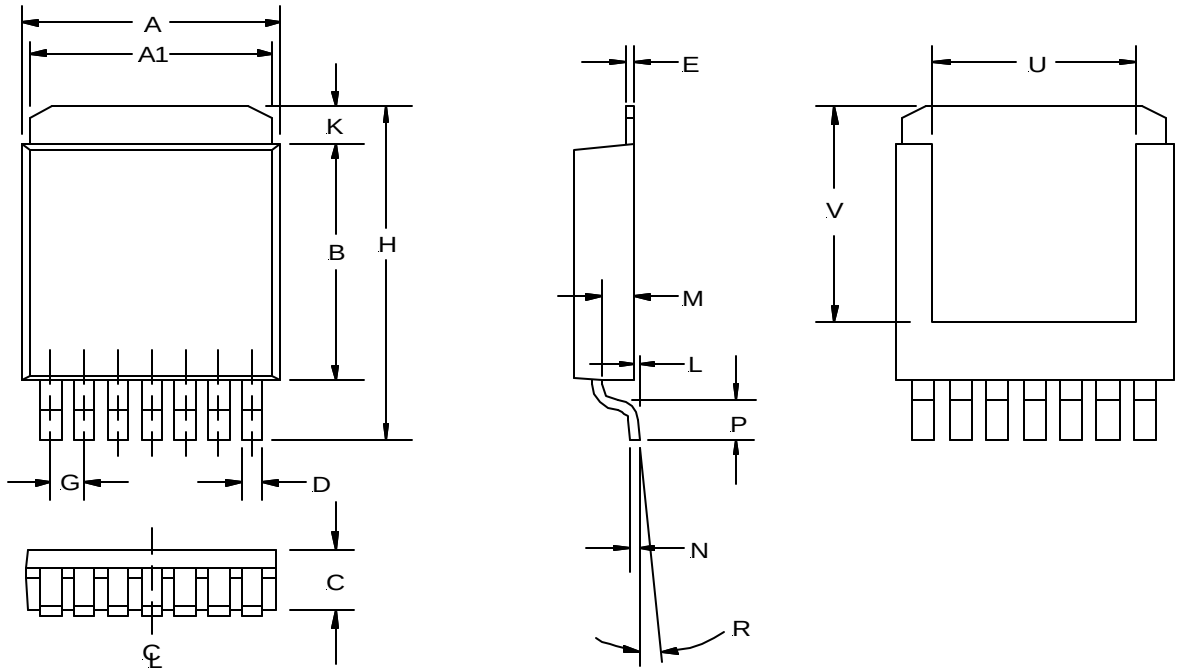
(P) Ultra Thin-Pak™
5-Pin



SYMBOL	MIN	MAX
A	9.27	9.52
A1	8.89	9.14
B	7.87	8.13
C	1.78	2.03
D	0.63	0.79
E	0.25 NOM	
G	1.72	
H	10.41	10.67
K	0.76	1.27
L	0.03	0.13
M	0.89	1.14
N	0.25	
P	0.79	1.04
R	3°	6°
U	5.59 NOM	
V	7.49 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

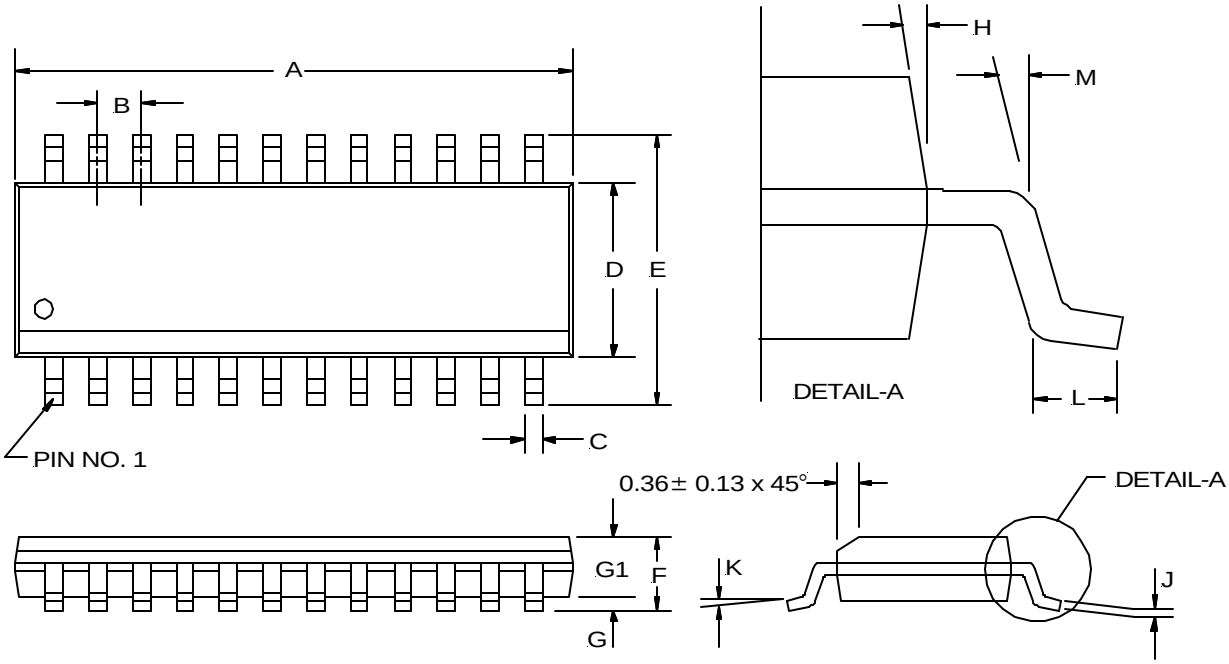
(P) Ultra Thin-Pak™
7-Pin



SYMBOL	MIN	MAX
A	9.27	9.52
A1	8.89	9.14
B	7.87	8.13
C	1.78	2.03
D	0.63	0.79
E	0.25 NOM	
G	1.27	
H	10.41	10.67
K	0.76	1.27
L	0.03	0.13
M	0.89	1.14
N	0.25	
P	0.79	1.04
R	3°	6°
U	5.59 NOM	
V	7.49 NOM	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

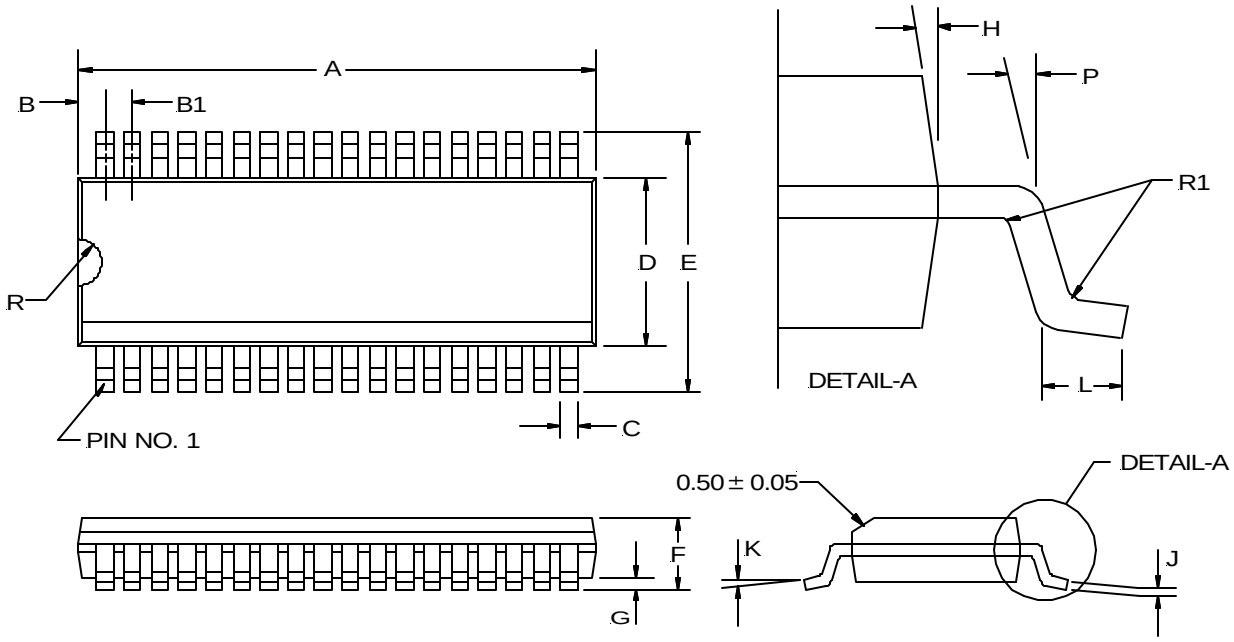
(Q) QSOP Package, Narrow Body
24-Pin



24-PIN		
SYMBOL	**MIN**	**MAX**
A	8.55	8.74
B	0.635 BSC	
C	0.20	0.30
D	3.81	3.99
E	5.79	6.20
F	1.35	1.75
G	0.10	0.25
G1	1.37	1.57
H	9° BSC	
J	0.19	0.25
K	0°	8°
L	0.40	1.27
M	7° ± 3°	

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

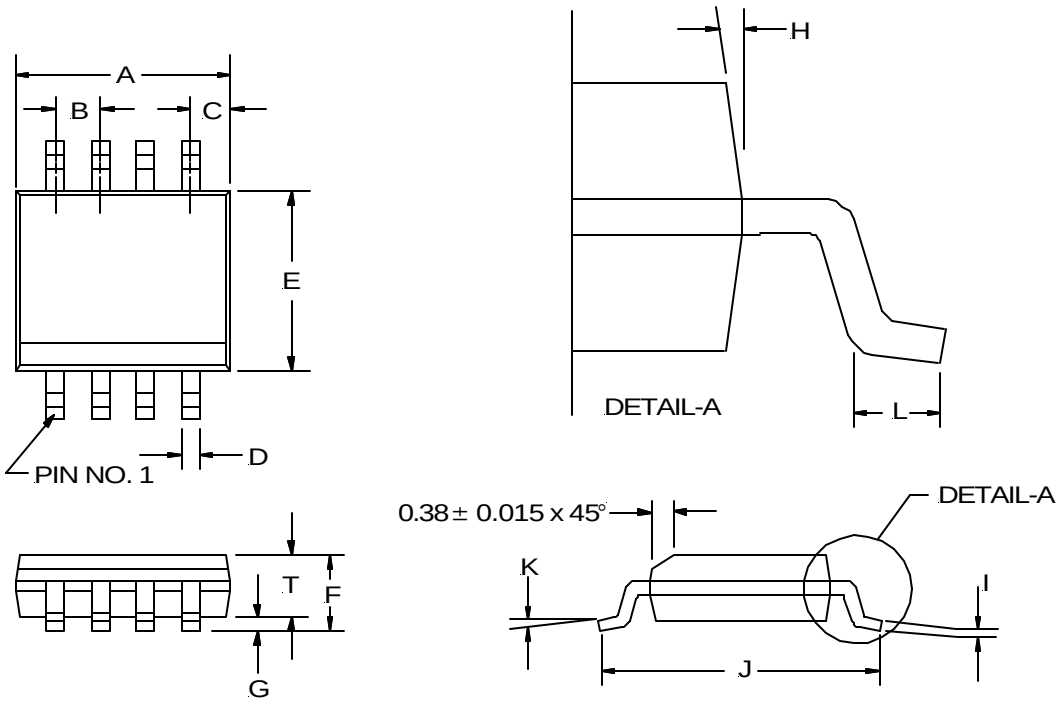
(Q) QSOP Package, Wide Body
36-Pin



36-PIN		
SYMBOL	**MIN**	**MAX**
A	15.20	15.40
B	0.85	
B1	0.80 REF	
C	0.28	0.51
D	7.40	7.60
E	10.11	10.51
F	2.44	2.64
G	0.10	0.30
H	7° TYP	
J	0.23	0.32
K	0°	8°
L	0.40	1.27
R	0.63	0.89
R1	0.20 ± 0.05	
P	7° ± 3°	

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

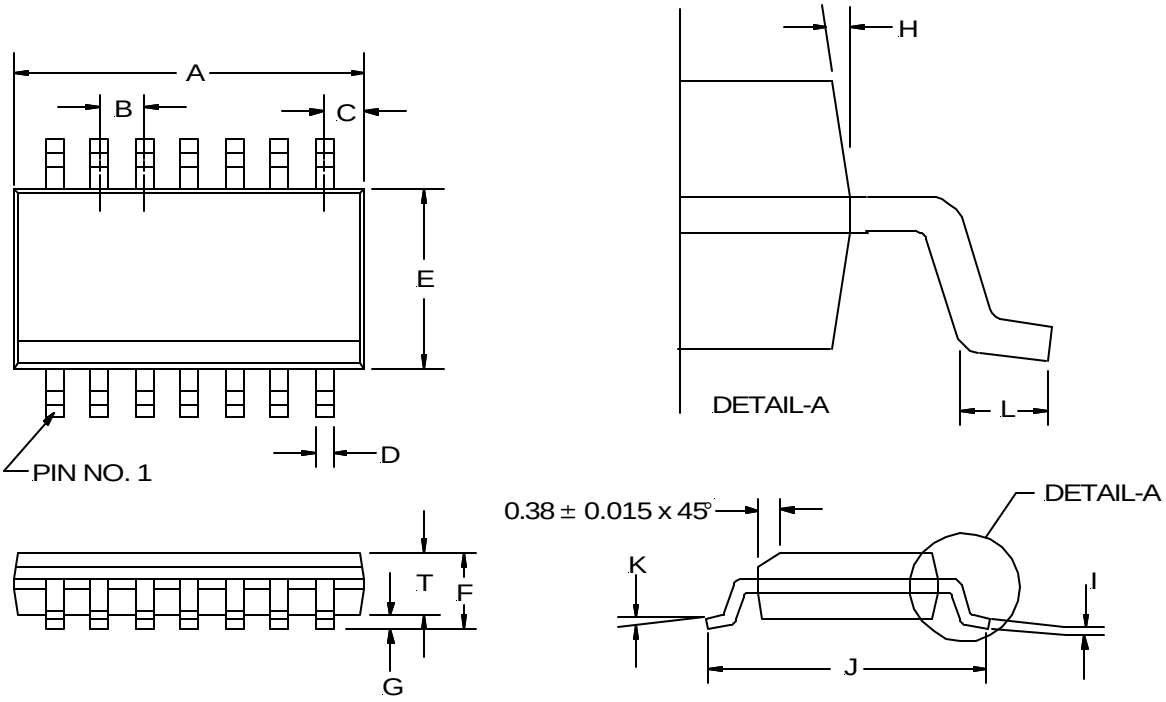
(S) SOIC Package
8-Pin Surface Mount, Narrow Body



8-PIN		
SYMBOL	**MIN**	**MAX**
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

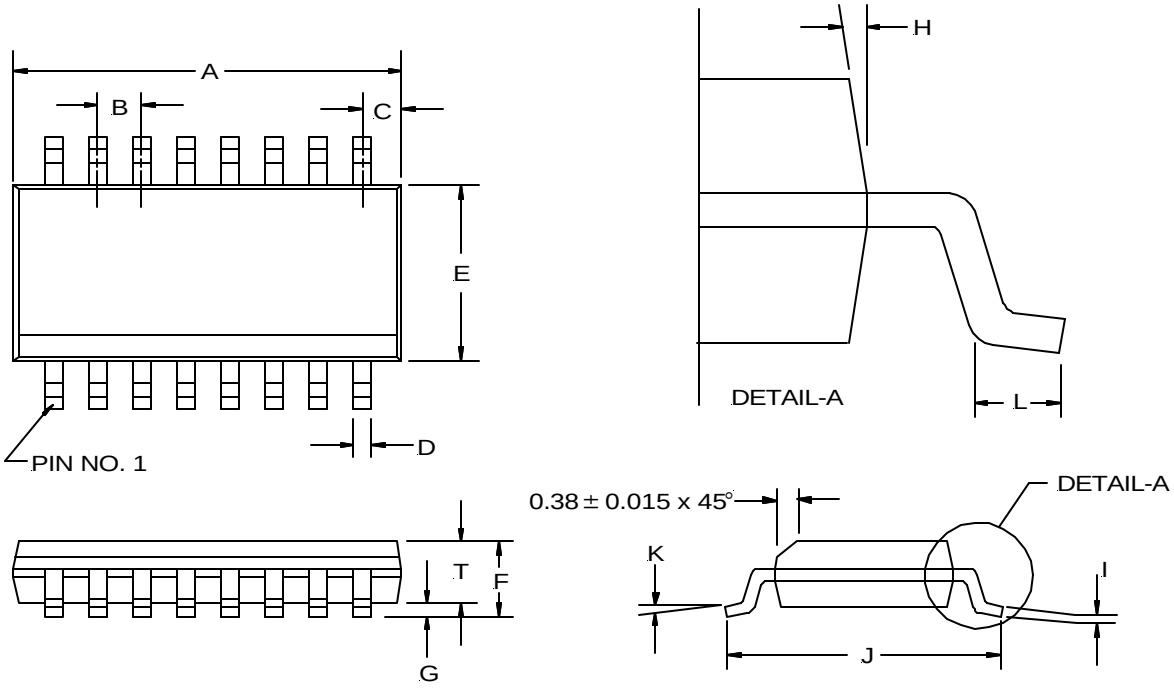
(S) SOIC Package
14-Pin Surface Mount, Narrow Body



14-PIN		
SYMBOL	**MIN**	**MAX**
A	8.56	8.74
B	1.27 BSC	
C	0.51 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

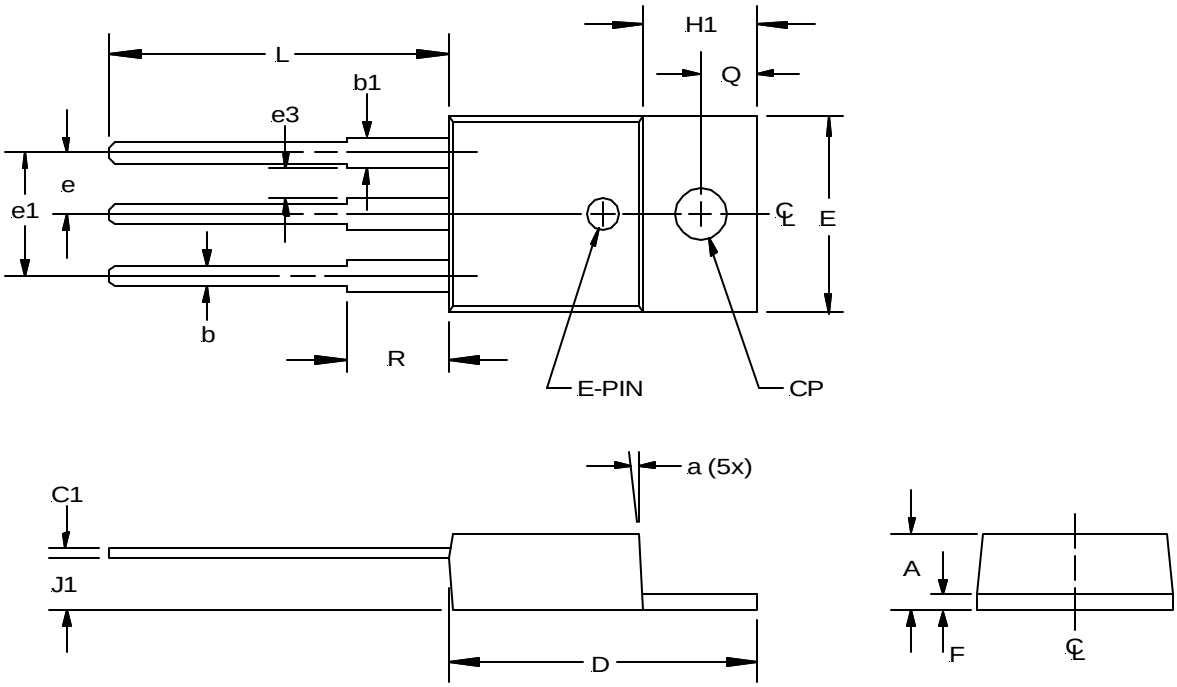
(S) SOIC Package
16-Pin Surface Mount, Narrow Body



16-PIN		
SYMBOL	**MIN**	**MAX**
A	9.80	9.98
B	1.27 BSC	
C	0.51 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

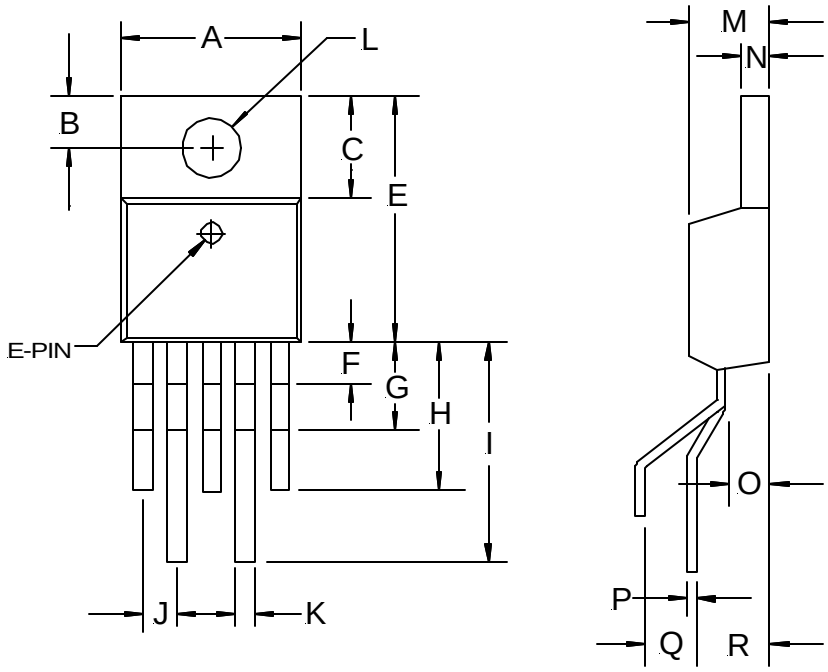
(T) TO-220 Package
3-Pin



SYMBOL	MIN	MAX
A	4.06	4.83
a	3°	7.5°
b	0.63	1.02
b1	1.14	1.52
C1	0.38	0.56
CP	3.71D	3.96D
D	14.22	15.062
E	9.78	10.54
e	2.29	2.79
e1	4.83	5.33
e3	1.14	1.40
F	1.14	1.40
H1	5.94	6.55
J1	2.29	2.92
L	13.716	14.22
Q	2.62	2.87
R	5.588	6.17

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

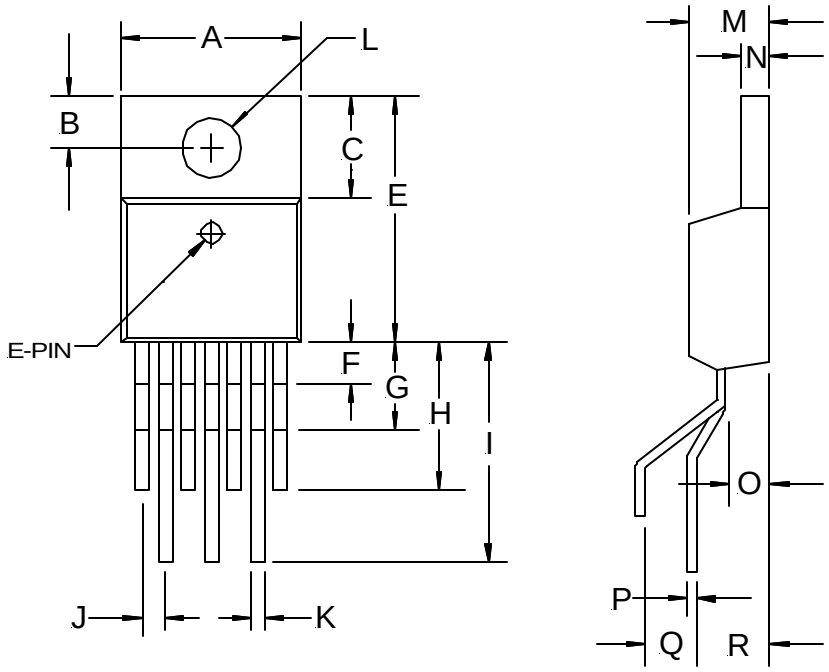
(T) TO-220 Package
5-Pin



SYMBOL	MIN	MAX
A	9.78	10.54
B	2.62	2.87
C	5.94	6.55
E	14.22	14.99
F	3.05	4.07
G	5.79	6.09
H	9.65	11.23
I	12.39	14.22
J	1.57	1.83
K	0.63	1.04
L	3.71D	3.96D
M	4.06	4.83
N	1.14	1.40
O	2.29	2.92
P	0.36	0.56
Q	3.43	4.19
R	3.93	4.95

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

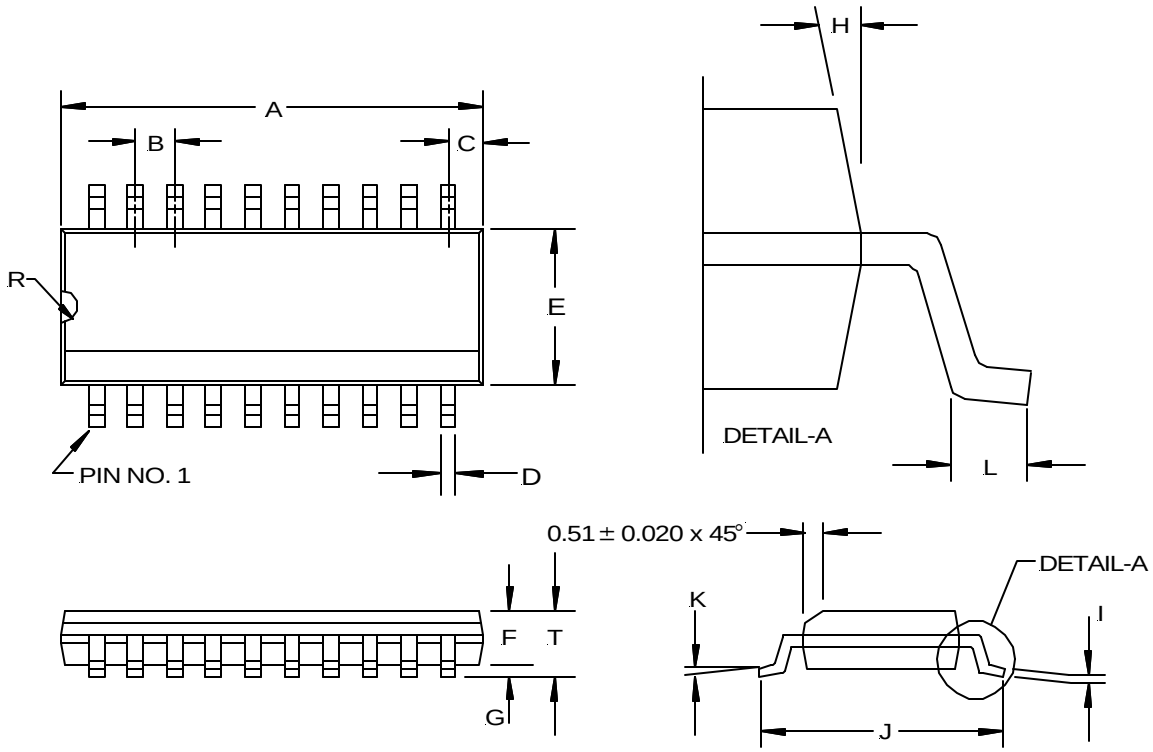
(T) TO-220 Package
7-Pin



SYMBOL	MIN	MAX
A	9.78	10.54
B	2.62	2.87
C	5.94	6.55
E	14.22	14.99
F	3.05	4.07
G	5.79	6.09
H	9.65	11.23
I	12.39	14.22
J	1.14	1.40
K	0.58	1.94
L	3.71D	3.96D
M	4.06	4.83
N	1.14	1.40
O	2.29	2.92
P	0.38	0.56
Q	3.43	4.19
R	3.93	4.95

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

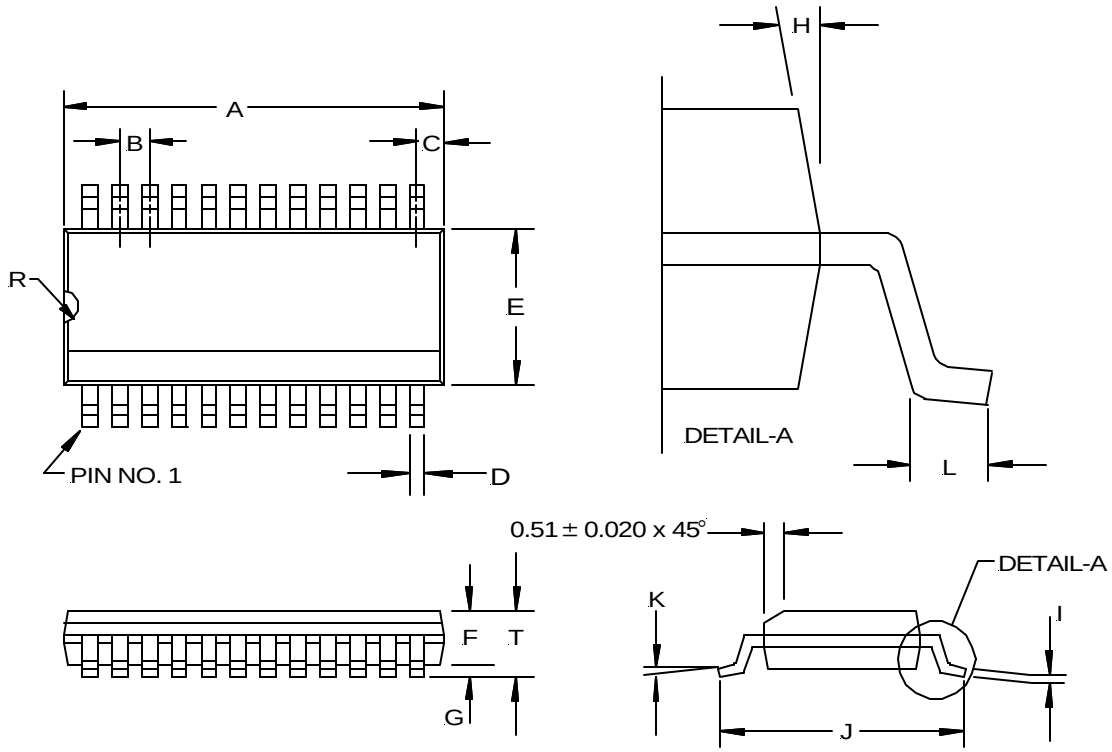
(W) SOIC Package
20-Pin Surface Mount, Wide Body



SYMBOL	20-PIN	
	MIN	MAX
A	12.598	12.979
B	1.018	1.524
C	0.66 REF	
D	0.33	0.508
E	7.40	7.60
F	2.032	2.64
G	0.10	0.30
I	0.229	0.32
J	10.008	10.654
K	0°	8°
L	0.406	1.270
R	0.63	0.89
T	2.337	2.642

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

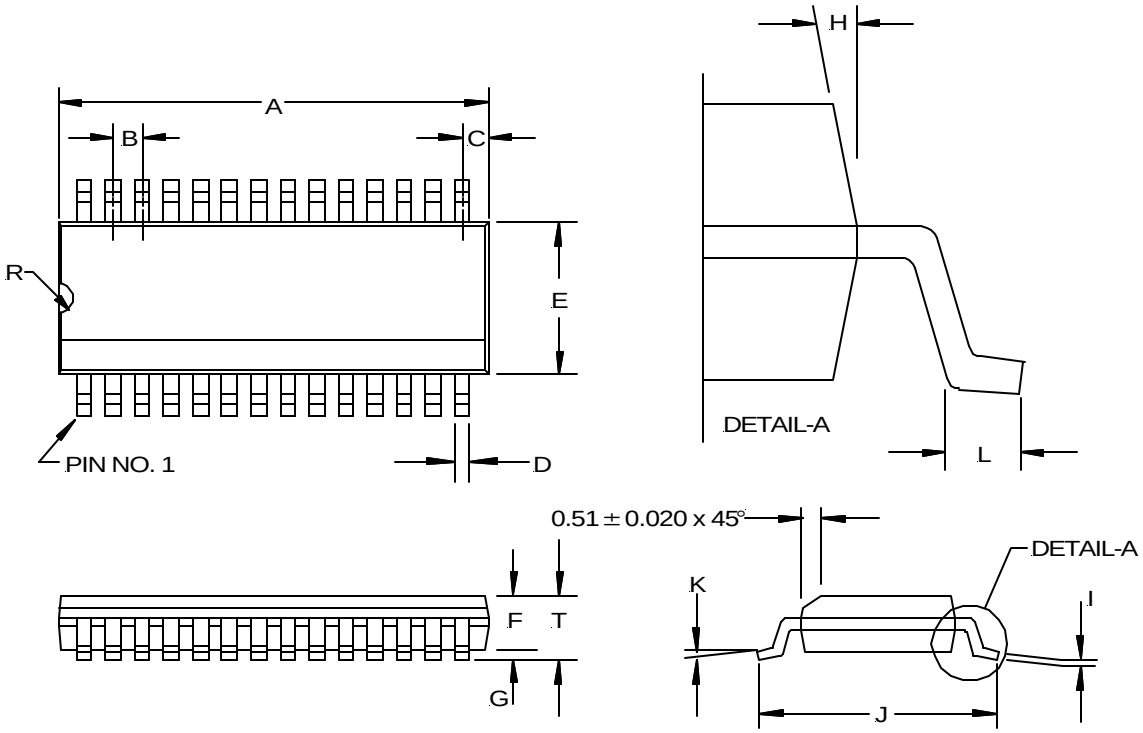
(W) SOIC Package
24-Pin Surface Mount, Wide Body



SYMBOL	24-PIN	
	MIN	MAX
A	15.20	15.40
B	1.27 BSC	
C	0.66 REF	
D	0.36	0.46
E	7.40	7.60
F	2.44	2.64
G	0.10	0.30
I	0.23	0.32
J	10.11	10.51
K	0°	8°
L	0.51	1.01
R	0.63	0.89
T	2.44	2.64

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

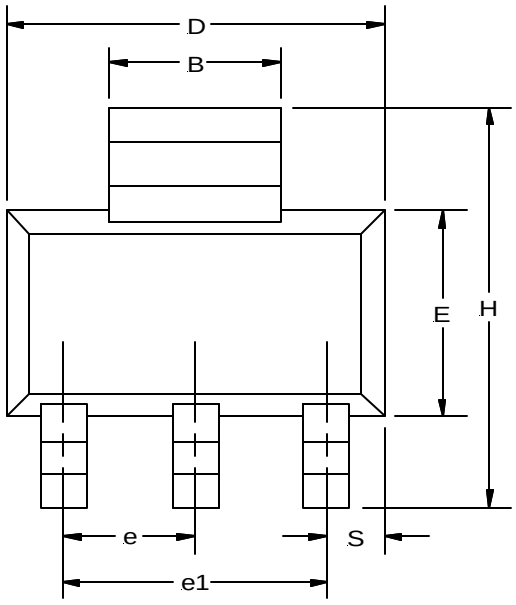
(W) SOIC Package
28-Pin Surface Mount, Wide Body



SYMBOL	28-PIN	
	MIN	MAX
A	17.73	17.93
B	1.27 BSC	
C	0.66 REF	
D	0.36	0.46
E	7.40	7.60
F	2.44	2.64
G	0.10	0.30
I	0.23	0.32
J	10.11	10.51
K	0°	8°
L	0.51	1.01
R	0.63	0.89
T	2.44	2.64

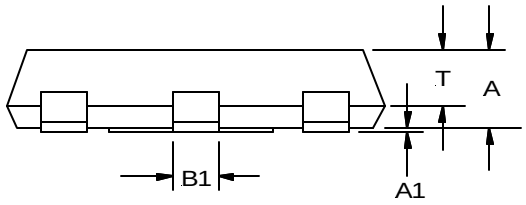
NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

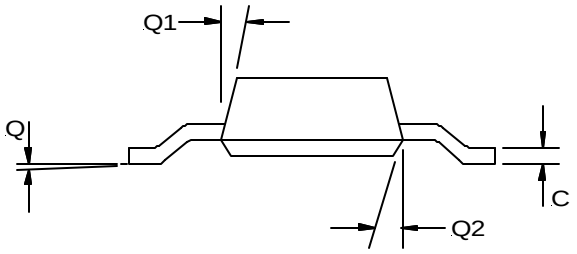
(Y) SOT-223 Package
3-Pin



SYMBOL	MIN	MAX
A	1.498	1.702
A1	0.02	0.11
B	2.895	3.15
B1	0.637	0.85
C	0.239	0.381
D	6.299	6.706
E	3.30	3.708
e	2.209	2.953
e1	4.496	4.699
H	6.70	7.30
Q	0°	10°
Q1	7°	16°
Q2	7°	16°
S	0.838	1.05
T	1.092	1.30

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.





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